SONiX Technology Co., Ltd.

SN8F5000 Family
Instruction Mapping Table

8051-based Microcontroller

1 Overview

SN8F5000 is 8051 Flash Type microcontroller supports comprehensive assembly instructions and which are fully compatible with standard 8051. To reduce the loading of code conversion when replace MCU from 8-Bit Flash/ OTP Type to 8051 Flash Type. This document supplies the information about mapping assembly instructions from 8-Bit Flash/ OTP Type to 8051 Flash Type. It categorizes the assembly instructions into five categories— data transfer operation, arithmetic operation, logic operation, process operation, and program branch.

2 Table of Contents

3 Revision History

Revision	Date	Description
1.0	Nov 2015	First issue

4 Instruction Mapping Table

Symbol description

Symbol	Description
M	Working register R0 - R7, one of 128 internal RAM locations, any Special Function Register or directly/indirectly addressed data
I	8-bit constant (immediate operand)
bit	One of 128 software flags located in internal RAM, or any flag of bit-addressable Special Function Registers
addr16	Destination address for LCALL or LJMP, can be anywhere within the 64-Kbyte page of program memory address space
addr11	Destination address for ACALL or AJMP, within the same 2-Kbyte page of program memory as the first byte of the following instruction
rel	SJMP and all conditional jumps include an 8-bit offset byte. Its range is +127/-128 bytes relative to the first byte of the following instruction
A	Accumulator
ins	One instruction

Data transfer operations

Mnemonic		Description	CY	AC	OV
8-bit Flash Type 8-bit OTP Type	8051 Flash Type				
MOV A, M	MOV A, M	A ← M	-	-	-
MOV M, A	MOV M, A	M ← A	-	-	-
B0MOV A, M	MOV A, M	A ← M (bank 0)	-	-	-
B0MOV M, A	MOV M, A	M (bank 0) ← A	-	-	-
MOV A, I	MOV A, I	A ← I	-	-	-
B0MOV M, I	MOV M, I	M ← I	-	-	-
XCH A, M	XCH A, M	A ←→M	-	-	-
B0XCH A, M	XCH A, M	A ←→M	-	-	-

MOVC	CLR A
	MOV DPTR,#Addr
	MOVC A, @A+DPTR
		A ← ROM [DPTR]	-	-	-

Arithmetic operations

Mnemonic		Description	CY	AC	OV
8-bit Flash Type 8-bit OTP Type	8051 Flash Type				
ADC A, M	ADDC A, M	A ← A + M + C, if occur carry, then CY=1, else CY=0	√	√	√
ADC M, A	ADDC A, M MOV M, A	M ← A + M + C, if occur carry, then CY=1, else CY=0	√	√	√
ADD A, M	ADD A, M	A ← A + M, if occur carry, then CY=1, else CY=0	√	√	√
ADD M, A	ADD A, M MOV M, A	M ← A + M, if occur carry, then CY=1, else CY=0	√	√	√
B0ADD M, A	ADD A, M MOV M, A	M (bank 0) ← M (bank 0) + A, if occur carry, then CY=1, else CY=0	√	√	√
ADD A, I	ADD A, I	A ← A + I, if occur carry, then CY=1, else CY=0	√	√	√
SBC A, M	SUBB A,M	A ← A - M - /CY, if occur borrow, then CY=0, else CY=1	√	√	√
SBC M, A	SUBB A,M MOV M,A	M ← A - M - /CY, if occur borrow, then CY=0, else CY=1	√	√	√

SUB A, M	CLR C SUBB A,M	A ← A - M, if occur borrow, then CY=0, else CY=1	√	√	√

SUB M, A	CLR C
	SUBB A,M
	MOV M,A
		M ← A - M, if occur borrow, then CY=0, else CY=1	√	√	√

SUB A, I	CLR C SUBB A,I	A ← A - I, if occur borrow, then CY=0, else CY=1	√	√	√
DAA	DA A	To adjust ACC's data format from HEX to DEC	√	–	–
MUL A, M	MUL A,B	B, A ← A * B, The LB of product stored in Acc and HB stored in B register. The carry flag is always cleared.	√	–	√

Logic operations

Mnemonic		Description	CY	AC	OV
8-bit Flash Type 8-bit OTP Type	8051 Flash Type				
AND A,M	ANL A, M	A ← A and M	–	–	–
AND M,A	ANL M, A	M ← A and M. M only support directly addressed location.	–	–	–
AND A,I	ANL A, I	A ← A and I	–	–	–
OR A,M	ORL A, M	A ← A or M	–	–	–
OR M,A	ORL A, M	M ← A or M, M only support directly addressed location	–	–	–
OR A,I	ORL A, I	A ← A or I	–	–	–
XOR A,M	XRL A, M	A ← A xor M	–	–	–
XOR M,A	XRL M, A	M ← A xor M, M only support directly addressed location	–	–	–
XOR A,I	XRL A, I	A ← A xor I	–	–	–
COM M	MOV A, M CPL A	A ← M (1's complement)	–	–	–

COMM M	MOV A, M
	CPL A
	MOV M, A
		M ← M (1's complement)	–	–	–

Process operations

Mnemonic		Description	CY	AC	OV
8-bit Flash Type 8-bit OTP Type	8051 Flash Type				
SWAP M	MOV A, M SWAP A	A (b3~b0, b7~b4) ←M(b7~b4, b3~b0)	–	–	–

SWAPM M	MOV A, M
	SWAP A
	MOV M, A
		M(b3~b0, b7~b4) ← M(b7~b4, b3~b0)	–	–	–

RRC M	MOV A, M RRC A	A ← RRC M	√	–	–

RRCM M	MOV A, M
	RRC A
	MOV M, A
		M ← RRC M	√	–	–

RLC M	MOV A, M RLC A	A ← RLC M	√	–	–

RLCM M	MOV A, M
	RLC A
	MOV M, A
		M ← RLC M	√	–	–

CLR M	MOV M, #00H	M ← 0	–	–	–
BCLR M.b	CLR bit	bit ← 0, only support directly addresses bit	–	–	–
	CLR C	CY← 0, only support carry flag	√	–	–
BSET M.b	SETB bit	bit ← 1, only support directly addresses bit	–	–	–
	SETB C	CY← 1, only support carry flag	√	–	–
B0BCLR M.b	CLR bit	bit ← 0, only support directly addresses bit	–	–	–
	CLR C	CY← 0, only support carry flag.	√	–	–
B0BSET M.b	SETB bit	bit ← 1, only support directly addresses bit	–	–	–
	SETB C	CY← 1, only support carry flag	√	–	–

Branch operations

Mnemonic		Description	CY	AC	OV
8-bit Flash Type 8-bit OTP Type	8051 Flash Type				
CMPRS A,I	SUBB A, I JZ rel ins	C ← A - I, if A = I, then skip next instruction	√	√	√

	rel: ins				
CMPRS A,M	SUBB A,M JZ rel ins rel: ins	C ← A – M, if A = M, then skip next instruction	√	√	√
INCS M	MOV A, M INC A JZ rel ins rel: ins	A ← M + 1, if A = 0, then skip next instruction	–	–	–
INCMS M	INC M MOV A, M JZ rel ins rel: ins	M ← M + 1, if M = 0, then skip next instruction	–	–	–
INC M	MOV A, M INC A	A ← M + 1	–	–	–
INCM M	INC M	M ← M + 1	–	–	–
DECS M	MOV A, M DEC A JZ rel ins rel: ins	A ← M - 1, if A = 0, then skip next instruction	–	–	–
DECMS M	DEC M MOV A, M JZ rel ins rel: ins	M ← M - 1, if M = 0, then skip next instruction.	–	–	–
DEC M	MOV A, M DEC A	A ← M – 1	–	–	–
DECM M	DEC M	M ← M – 1	–	–	–
BTS0 M.b	JB bit, rel	If bit = 0, then skip next instruction. Only	–	–	–

	ins rel: ins	support directly address bit			
BTS1 M.b	JNB bit, rel ins rel: ins	If bit = 1, then skip next instruction. Only support directly address bit	–	–	–
B0BTS0 M.b	JB bit, rel ins rel: ins	If bit = 0, then skip next instruction. Only support directly address bit	–	–	–
B0BTS1 M.b	JNB bit, rel ins rel: ins	If bit = 1, then skip next instruction. Only support directly address bit	–	–	–
TS0M M	–	If M = 0, Z = 1. Else Z = 0	–	–	–
JMP d	AJMP addr11	Absolute jump	–	–	–
	LJMP addr16	Long jump	–	–	–
	SJMP rel	Short jump (relative address).	–	–	–
CALL d	ACALL addr11	Absolute subroutine call	–	–	–
	LCALL addr16	Long subroutine call	–	–	–
CALLHL	ACALL addr11	Absolute subroutine call	–	–	–
	LCALL addr16	Long subroutine call	–	–	–
CALLYZ	ACALL addr11	Absolute subroutine call	–	–	–
	LCALL addr16	Long subroutine call	–	–	–

Branch operations

Mnemonic		Description	CY	AC	OV
8-bit Flash Type 8-bit OTP Type	8051 Flash Type				
RET	RET	PC ← Stack	–	–	–
RETI	RETI	PC ← Stack, and to enable global interrupt	–	–	–
RETLW I	RET MOV A, I	PC ← Stack, and load I to ACC	–	–	–
NOP	NOP	No operation	–	–	–

SN8F5000 Family Instruction Mapping Table

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