1 GENERAL DESCRIPTION

The SNC85F E/A/D 24MHz 16-bit RISC controller series is embedded Flash controller with multi-channel 2/8~24 hardware Voice/MIDI Wave Processing Unit (WPU). In addition to having multi-channel hardware channels, two software high quality voice channels with SONiX HQDPCM/Audio32 algorithm is provided.

Key peripherals include a single high quality 13bit DPWM audio output, Max.31-channel comparator for cap sensing touch, three external interrupts, Max. 31ch PWMIOs, serial peripheral interface (SPI0&SPI1),IIC TX/RX, UART TX/RX, and three 12-bit timers. The device features provide idle mode for real-time clock (RTC) applications and sleep mode for power savings.

The SNC85F contains a Low Voltage Detector (LVD) for power management usage. The status of internal or external power can be detected and reported to the management software. There is a Low Voltage Reset (LVR) function provided to keep the whole system from losing data when voltage drops to a low level.

1.1. Features

■ CPU

- Operating voltage: 1.8V ~ 5.5V
- System clock: 24.576MHz
- System clock source:
  - High clock:
    Internal ROSC 24.576 MHz +-0.5%
    external 24.576 MHz crystal.(by body)
  - Low clock:
    Internal ILRC 32.768K
    External 32.768KHz crystal(by body)
- Programmable System Clock:
  24MHz(12MIPS), 12MHz(6MIPS),
  6MHz(3MIPS), 3MHz(1.5MIPS)
- Flash:
  - Embedded Flash 8Mbit for program and data storage.
  - ISP (In-system program) is provided
  - Typical 10,000 erase/program cycles
- RAM Size:
  - 3K words
- Provides Idle and Sleep mode to reduce power consumption
- General-Purpose I/O ports:
  - 31programmable I/Os
- Timer/Counter
  - Three12-bit TimerA & TimerB & TimerC Counter
  - Timer1 (1ms, 4ms)
  - RTC Timer can be programmable: 62.5ms ~ 64sec
  - WDT Timer 0.25sec
  - One 16-bit TimerD with Capture Timer Function
- 3 External interrupt Sources: INT0, INT1, INT2
- 31 Hardware PWMIOs with 256-level brightness control (by body)
- IR function provided
- Low Voltage Reset (LVR 1.70V)
- Low Voltage Detector (LVD)
  - 8 levels (2.0V/2.2V/2.4V/2.6V/2.8V/ 3.0/3.2V/3.4V)

  - Detect internal VDD or external voltage input
- Provide regulator LDO33 for SPI Flash
- 31-channel comparator for Cap sensing applications(by body)
- Two Serial Peripheral Interface (SPI0&SPI1)
  - SPI0 support master and slave mode.
  - SPI1 support master mode only.(by body)
- I2C TX/RX
- UART TX/RX
- 12bit SAR ADC (by body)
- Package
  - SOP8/SOP16/SSOP24/LQFP48

■ WPU

- Two software channels with noise filter to play high quality sound
  - 3/4/5-bit HQDPCM(SW channel)
  - 1.0/1.5/2.0-bit Audio32,low bit rate algorithm
- Maximum 24 independent voice/MIDI Hardware channels with noise filter
- Single 13-bit DPWM audio output for direct drive speaker
- Hardware channels with three playing modes by Wave Processing Unit:
  - 4-bit HQDPCM(HW channel)
  - 5-bit HQDPCM(HW channel)
  - 6-bit HQDPCM(HW channel)
- Event Mark function is supported

1.2. Applications

- Electronic Piano
- High end toy controller
- General Music synthesizer
- General purpose controller

Table of Contents

2 REVISION HISTORY

Version	Date	Description
Rev. 1.0	July 22, 2020	First release
Rev 1.1	November 18,2020	Update Part. No.
Rev 1.2	December 30,2020	Update Package type
Rev 1.3	May 6,2021	Update ELECTRICAL CHARACTERISTICS
Rev1.4	May 13,2021	Modify SNC85F100E/ SNC85F150E/ SNC85F150A SRAM SPEC
Rev 1.5	May 27,2021	1. modify PRODUCT SELECTION GUIDE 2. modify SOP8 part number
Rev 1.6	June 21, 2021	1. Modify APPLICATION CIRCUIT,Add C3/C4/C5/R5 for system ESD protection 2. Modify standby current spec.
Rev1.7	January 18, 2022	Modify PRODUCT SELECTION GUIDE
Rev 1.8	September 02, 2022	1. Modify APPLICATION CIRCUIT, delete R5/C5 component. 2. Add SNC85F240D IC body
Rev 1.9	December 22, 2022	Add SNC85F240A/SNC85F320A IC body
Rev2.0	March 9, 2023	Modify product selection guide
Rev2.1	August 29, 2023	Modify product selection guide
Rev2.2	September 08, 2023	1. Modify APPLICATION CIRCUIT C3/C4= 10nF as C3/C4 = 1nF.
Rev2.3	October 31,2023	Modify APPLICATION CIRCUIT C3/C4 = 1nF & connect to GND_PWM
Rev2.4	April 11,2024	Add PCB Layout guide.
Rev2.5	June 20, 2024	modify idle mode current
Rev2.6	October 07,2024	Modify Multi-Function of I/Os
Rev 2.7	January 09,2025	Modify PCB layout guide
Rev 2.8	February 13,2025	Modify PCB layout guide of English part.

3 PRODUCT SELECTION GUIDE

SNC85FxxxE series (2+2ch speech/MIDI, Audio32)

Part No.	Embedded Flash	Audio32 12Kbps (8K S.R.)	HQ (6K S.R.)	Audio32/HQ Speech Channel	H/W Voice/MIDI Channel	RAM	I/O	Cap-Touch Key/PWMIO	12bit SAR ADC	LDO33	OSC
SNC85F240E	192K*16	240sec	156sec	2	2	3072*16	31	31/31	None	V	ROSC/Xtal
SNC85F320E	256K*16	328sec	208sec	2	2	3072*16	31	31/31	None	V	ROSC/Xtal
SNC85F500E	384K*16	502sec	313sec	2	2	3072*16	31	31/31	None	V	ROSC/Xtal
SNC85F670E	512K*16	677sec	417sec	2	2	3072*16	31	31/31	None	V	ROSC/Xtal

SNC85FxxxA series (8~24+2ch speech/MIDI, Audio32)

Part No.	Embedded Flash	Audio32 12Kbps (8K S.R.)	HQ (6K S.R.)	Audio32/HQ Speech Channel	H/W Voice/MIDI Channel	RAM	I/O	Cap-Touch Key/PWMIO	12bit SAR ADC	LDO33	OSC
SNC85F240A	192K*16	240sec	156sec	2	8~24	3072*16	31	31/31	None	V	ROSC/Xtal
SNC85F320A	256K*16	328sec	208sec	2	8~24	3072*16	31	31/31	None	V	ROSC/Xtal
SNC85F500A	384K*16	502sec	313sec	2	8~24	3072*16	31	31/31	None	V	ROSC/Xtal
SNC85F670A	512K*16	677sec	417sec	2	8~24	3072*16	31	31/31	None	V	ROSC/Xtal

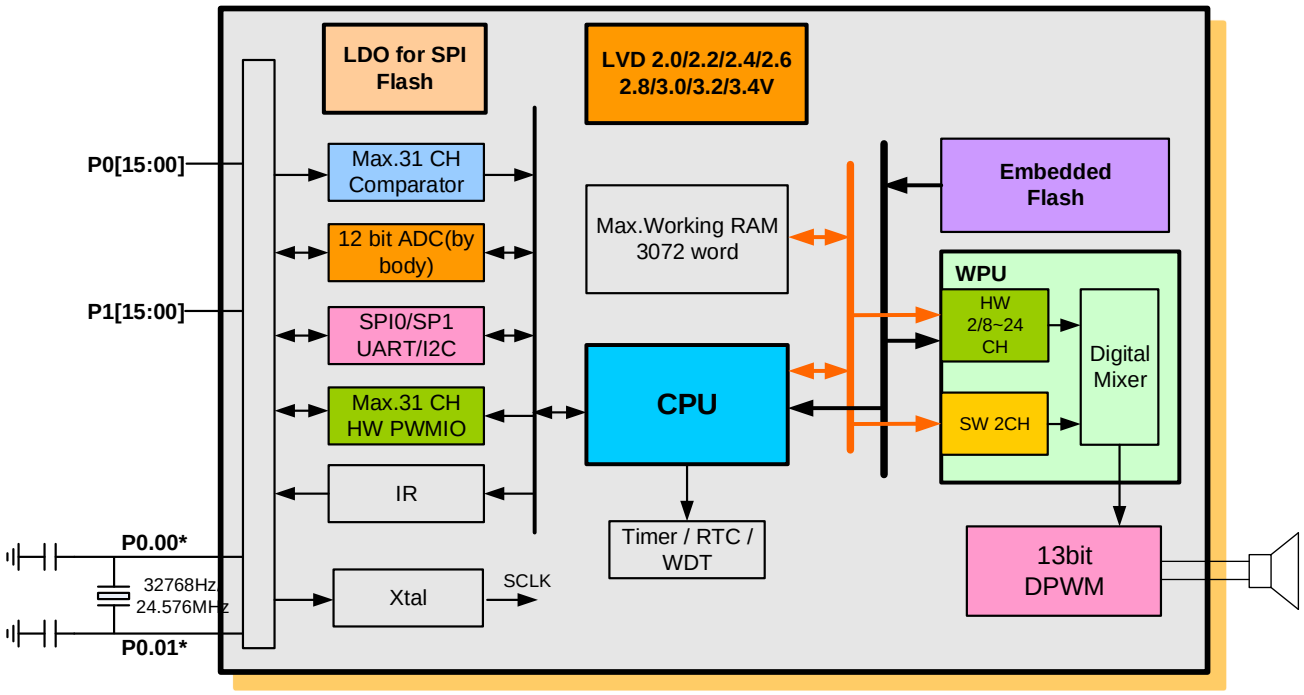
SNC85FxxxD series (8~24+2ch speech/MIDI, Audio32, ADC)

Part No.	Embedded Flash	Audio32 12Kbps (8K S.R.)	HQ (6K S.R.)	Audio32/HQ Speech Channel	H/W Voice/MIDI Channel	RAM	I/O	Cap-Touch Key/PWMIO	12bit SAR ADC	LDO33	OSC
SNC85F240D	192K*16	240sec	156sec	2	8~24	3072*16	31	31/31	**V**	V	ROSC/Xtal
SNC85F320D	256K*16	328sec	208sec	2	8~24	3072*16	31	31/31	**V**	V	ROSC/Xtal
SNC85F670D	512K*16	677sec	417sec	2	8~24	3072*16	31	31/31	**V**	V	ROSC/Xtal

The difference between SNC85F and SNC86P

	SNC85F(Flash based)	SNC86P(OTP based)
VDD	1.8V~5.5V	2.2V~5.5V
CPU cycle	12.288Mhz	6.144Mhz
RAM	3072*16	1520*16
Hardware channel	2/8~24 ch 4/5/6 bit HQDPCM	2/8/16/24ch 5/6/8 bit ADPCM
Midi Instrument	Musical Instrument store in external SPI flash or internal Flash	Only internal OTP
Software channel	2ch	1ch
Audio32(low bit rate algorithm)	2ch	Only 1 ch
PWMIO	16/31	12
Input Pull-low Resistance	1MΩ@5V or100KΩ@5V	600KΩ@5V
ISP(In system program)	V	None
ADC	V(SNC85F320D/ SNC85F670D)/SNC85F240D	None
SPI0,Master/Slave mode	V	None
SPI1,Master only	V	V
I2C	V	None
UART	V	None
Operating Current	3.0mA@12MIPS 2.0mA@6MIPS	6mA@6MIPS
External reset pin	High reset	Low reset

4 Functional Block Diagram



*Note. P0.00 & P0.01 is share pin

*Note: (1) Number of Comparator channels by body is 31 CH
(2) Number of Hardware PWMIOs by body is 31 CH
(3) Number of GPIOs by body is 31IO.

5 PIN ASSIGNMENT

31IO body:
SNC85F500E/SNC85F670E/SNC85F500A/SNC85F670A
SNC85F320D/SNC85F670D/SNC85F240D
SNC85F240A/SNC85F320A/SNC85F240E/SNC85F320E

Pad Name	I/O	Function Description
P0.00 ~ P0.15	I/O	Bit00 ~ Bit15 of I/O port 0 P0.11: ICP_CLK/GPIO P0.10: ICP_DATA0/GPIO P0.06: ICP_DATA1/RST/GPIO
P1.00 ~ P1.08	I/O	Bit00 ~ Bit08 of I/O port 1
P1.10 ~ P1.15	I/O	Bit10 ~ Bit15 of I/O port 1 P1.15 ICE mode: ICE_CSB free run:GPIO
RST	I	Reset Pin: High reset
VDD_PWM	P	Positive power supply for PWM audio output
GND_PWM	P	Negative power supply for PWM audio output
BUO1	O	PWM audio output1
BUO2	O	PWM audio output2
VDDIO	P	Positive power supply for I/O
GNDIO	P	Negative power supply for I/O
VDDSPI	P	Positive power supply for SPI interface
REGOUT33	P	Regulator(LDO33) output for external SPI flash
REGOUT16	P	Regulator(LDO16) output for core power
VDDREG	P	Positive power supply for Regulator circuit
GNDREG	P	Negative power supply for Regulator circuit

6 PACKAGE FORM

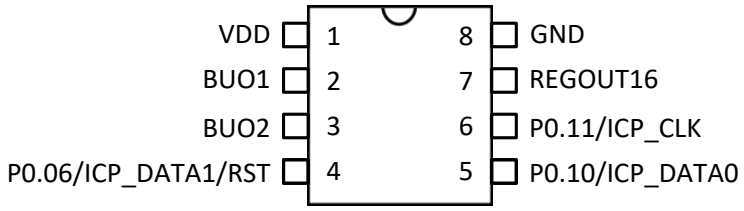
6.1. SOP8

SNC85F240~SNC85F670
Part Number: SNC85FxxxYSG

SOP8

Support 3IO :

P0.06/P0.10/P0.11

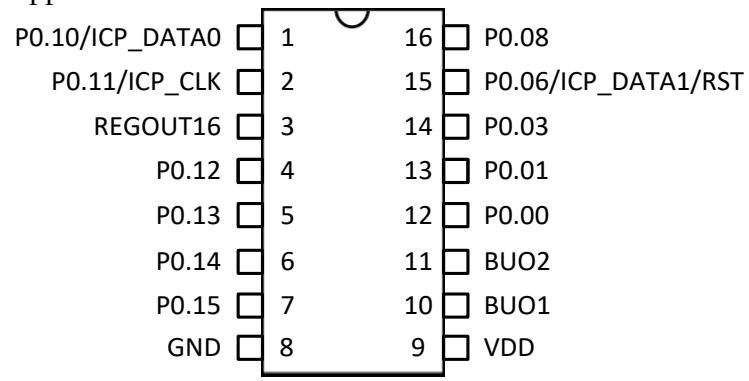


6.2. SOP16

SNC85F240~SNC85F670
Part Number: SNC85FxxxFSG

SOP16

Support 11IO:

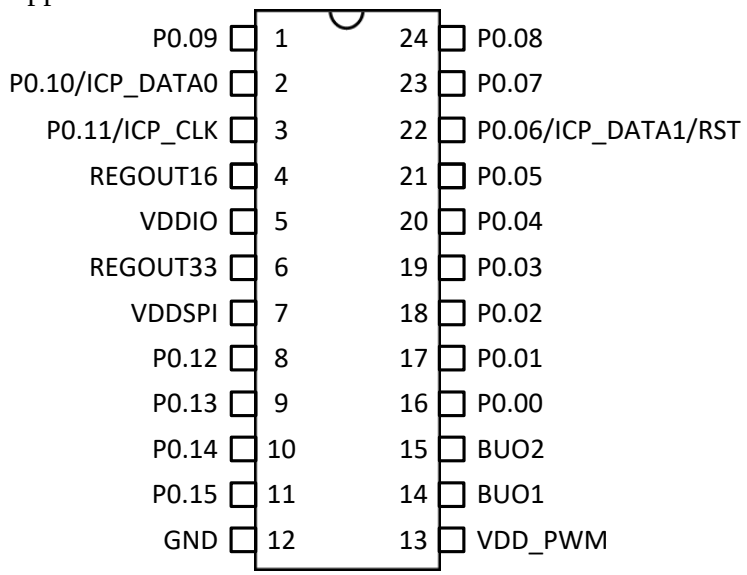


6.3. SSOP24

SNC85F240~SNC85F670
Part Number: SNC85FxxxKXG

SSOP24

Support 16IO:

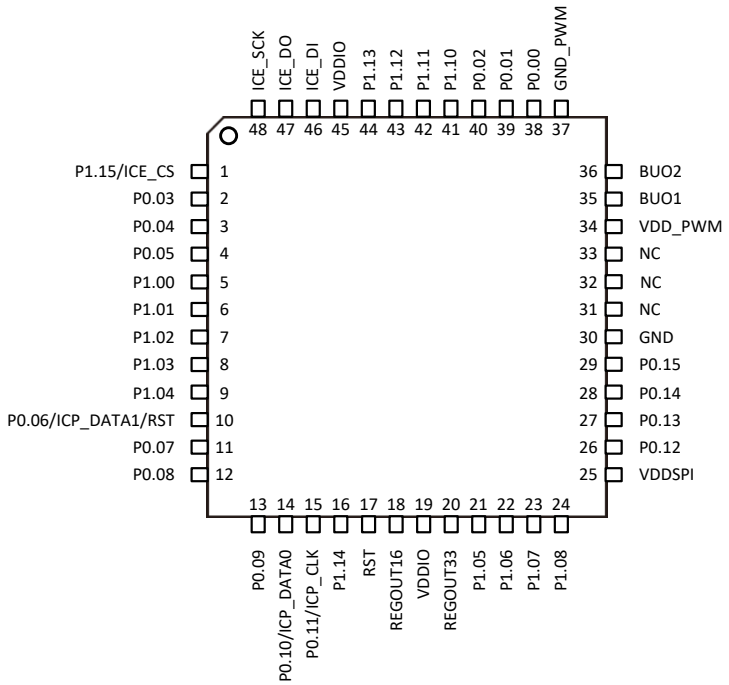


6.4. LQFP48

SNC85F240~SNC85F670
Part Number: SNC85FxxxTFG

LQFP48

Support 31 IO:



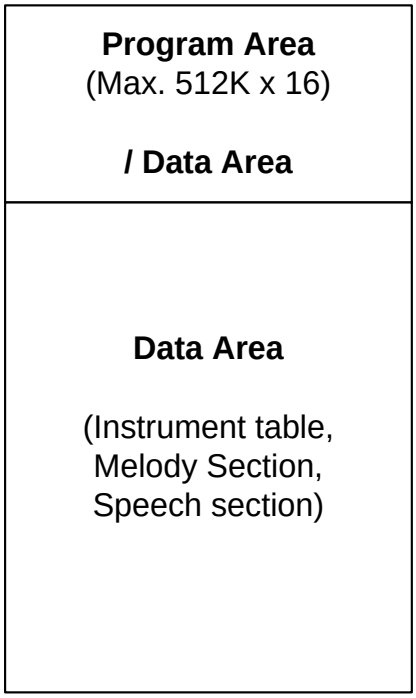
7 FUNCTIONAL DESCRIPTIONS

7.1. CPU Architecture Description

The SNC85F family CPU is a 16-bit RISC architecture that provides powerful instructions and enhances RAM access to reduce instruction and execution cycles. The CPU is based on 24MHz clock system and contains RAM, Flash, Stack, I/Os, Timer, ALU and interrupt functions.

7.2. Flash

The SNC85F family contains a substantial amount of internal Flash that is shared by program and resource data. Program data cannot exceed 512K words. The architecture of Flash is shown as follows:



Architecture of Flash

7.3. RAM

The SNC85F RAM is separated into several banks. Each RAM bank contains 256 words where the appropriate bank number must be set before access. The RAM is subdivided into 12 banks where each bank contains 256 words. The address table of the RAM banks is shown below.

SNC85F320D/SNC85F670D/SNC85F240D

Bank Num	Address Range	Description	Total Size (word)
0	0x000~0x05F	Special Registers	
	0x060~0x067	Bit Operation for C/User RAM	8
	0x068~0x06D	Reserved for C	6
	0x06E~0x0FF	User RAM	146
1	0x100~0x1FF	SW CH0/User RAM	256
2	0x200~0x23B	WPU RAM/User RAM	60
	0x23C~0x2DF	User RAM	164
	0x2E0~0x2FF	Stack buffer	32
3	0x300~0x3FF	SW CH1/User RAM	256
4	0x400~0x4FF	ADC RAM/User RAM	256
5	0x500~0x5FF	ADC RAM/User RAM	256
6	0x600~0x6FF	ADC RAM/User RAM	256
7	0x700~0x7FF	ADC RAM/User RAM	256
8	0x800~0x8FF	User RAM	256
9	0x900~0x9FF	User RAM	256
10	0xA00~0xAFF	User RAM	256
11	0xB00~0xBFF	User RAM	256
12	0xC00~0xC03	WPU Channel RAM 00/User RAM/PERAM	4
	0xC04~0xC07	WPU Channel RAM 01/User RAM/PERAM	4
	---		36
	0xC2C~0xC2F	WPU Channel RAM 11/User RAM/PERAM	4
	0xC30~0xC7F	User RAM/PERAM	80
	0xC80~0xC87	WPU Channel RAM 00/User RAM/PERAM	8
	0xC88~0xC8F	WPU Channel RAM 01/User RAM/PERAM	8
	---		72
	0xCD8~0xCDF	WPU Channel RAM 11/User RAM/PERAM	8
	0xCE0~0xCFF	User RAM/PERAM	32
13	0xD00~0xD7F	User RAM	128

	0xD80~0xDFF	Un-define	

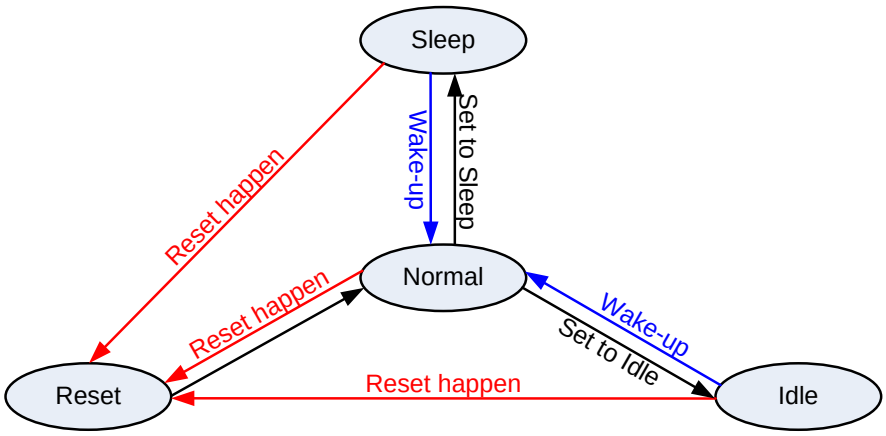
SNC85F500E/SNC85F670E/SNC85F500A/SNC85F670A
SNC85F240A/SNC85F320A/ SNC85F240E/SNC85F320E

Bank Num	Address Range	Description	Total Size (word)
0	0x000~0x05F	Special Registers	
	0x060~0x067	Bit Operation for C/User RAM	8
	0x068~0x06D	Reserved for C	6
	0x06E~0x0FF	User RAM	146
1	0x100~0x1FF	SW CH0/User RAM	256
2	0x200~0x23B	WPU RAM/User RAM	60
	0x23C~0x2DF	User RAM	164
	0x2E0~0x2FF	Stack buffer	32
3	0x300~0x3FF	SW CH1/User RAM	256
4	0x400~0x4FF	User RAM	256
5	0x500~0x5FF	User RAM	256
6	0x600~0x6FF	User RAM	256
7	0x700~0x7FF	User RAM	256
8	0x800~0x8FF	User RAM	256
9	0x900~0x9FF	User RAM	256
10	0xA00~0xAFF	User RAM	256
11	0xB00~0xBFF	User RAM	256
12	0xC00~0xC03	WPU Channel RAM 00/User RAM/PERAM	4
	0xC04~0xC07	WPU Channel RAM 01/User RAM/PERAM	4
	---		36
	0xC2C~0xC2F	WPU Channel RAM 11/User RAM/PERAM	4
	0xC30~0xC7F	User RAM/PERAM	80
	0xC80~0xC87	WPU Channel RAM 00/User RAM/PERAM	8
	0xC88~0xC8F	WPU Channel RAM 01/User RAM/PERAM	8
	---		72
	0xCD8~0xCDF	WPU Channel RAM 11/User RAM/PERAM	8
	0xCE0~0xCFF	User RAM/PERAM	32
13	0xD00~0xD7F	User RAM	128
	0xD80~0xDFF	Un-define	

7.4. Operation Modes

The SNC85F operates in three modes for different clock rates and power saving purposes. There is one active mode as well as two software selectable low-power modes of operation. GPIO or RTC event can wake up the device from any of the two low-power modes.
The following three operating modes are configured by software:

- **Normal Mode：**
  - All clocks are active
  - System clock rate can selectable from 24MHz to 3MHz
- **Idle Mode：**
  - CPU is disabled
  - Only Low-speed clock is turn on
  - RTC Mode
- **Sleep Mode：**
  - CPU is disabled
  - High and Low speed clock is turn off



Operating Mode Control Block

SNC85F function status in all Operating Modes:

Mode / Device	Sleep	Idle	Normal
IHRC(High CLK)	X	X	O
ILRC(32768Hz)	X	O	O
X'tal(32768Hz)	X	O	O
CPU	X	X	O
Interrupt	X	X	O
WPU	X	X	O
SPI	X	X	O
PWMIO	X	X	O
IR	X	X	O
Comparator	X	X	O
DPWM	X	X	O
Timer	X	X	O
RTC	X	O	O
LVD	X	X	O
LVR	O	O	O

Note: In normal mode, software is used to change operation to sleep, idle, or normal modes.

7.5. Interrupts

Interrupts are an important part of any microcontroller system. The SNC85F provides 16 interrupt sources. When the CPU enters an interrupt service routine, the GIE bit (in INTEN) will be cleared to "0". Any other interrupt requests will not be granted at this time. Instead, these requests will be queued in INTRQ.*IRQ, and will be served once GIE is restored to "1" The GIE will be restored to 1 once the CPU exits an ISR.

Interrupt vectors table:

Interrupt Source	Priority	Entry Location	Descriptions
TimerA	1	0X10	TimerA interrupt
UART RX	2	0x14	UART RX interrupt
TimerB	3	0x18	TimerB interrupt
INT0	4	0x1C	External INT0
INT1	5	0x20	External INT1
PWMIO	6	0x24	PWMIO Counter
TimerC	7	0x28	TimerC interrupt
INT2	8	0x2C	External INT2
Timer1	9	0x30	Timer1 interrupt
UART TX	10	0x34	UART TX interrupt
CMP	11	0x38	Comparator edge trigger
TimerD	12	0x3C	Timer D interrupt for Cap sensing
SPI0	13	0x40	SPI0 interrupt
I2C	14	0x44	I2C interrupt
RTC	15	0x48	RTC interrupt
Stack overflow	16	0x4C	Stack overflow

7.6. In-system programming (ISP)

SNC85F provides In-System Program for convenient, upgradeable code storage. The flash memory may be programmed via the ISP or application code for maximum flexibility. SNC85F also provides write protection options to prevent data programmed or erased.

- The CPU is stalled during ISP program and erase operations, other peripherals (Timers, WDT, UART, SPI, etc.) remain active.
- After the operation of ISP, FW need to execute “NOP” instruction for three times.
- Watch dog should be cleared before ISP program or erase operations.
- The erase operation sets all the bits in the flash to logic 1.
- HW will hold system clock and automatically move out data from RAM and do programming, after programming finished, HW will release system clock and let CPU execute the next instruction.
- Setting the sector erase before executing the page program.

7.6.1 Program/Erase

The ISP program/erase operation requires different length and time. The definition is shown as below.

- Sector erase: 256 words (512bytes) :2.5ms
- Page program: 128 words (256 bytes) :1.3ms
- Word program: 1 word (2 bytes) : 36.2us

7.6.2 ISP Commands

The ISP provides different commands for program/erase. The command set is shown as below.

- Page program PECMD = 0x5A
- Word program PECMD = 0x1E
- Sector erase PECMD = 0x96

7.6.3 ISP Control Flow

These configurations must be setup completely before ISP operation. ISP is configured using the following steps, use page program as example.

1. Save program data into PERAM.
2. Set the start address to PERAM [7:0].
3. Set the start address of updated area to PEROM [18:0]. (By PEROMH/PEROML registers)
4. Write 1 to Write_En bit of PECMD [15] to enable ISP program/erase.
5. Write ‘0x96’ to PECMD [7:0] to trigger ISP erase function.
6. Write ‘NOP’ instruction for three times.
7. Write ‘0x5A’ to PECMD [7:0] to trigger ISP program function.
8. Write ‘NOP’ instruction for three times.

7.6.4 Write Protection

SNC85F provides write protect function for ISP. The write protection use (CMP, BP4, BP3, BP2, BP1 and BP0) bits to allow part of memory to be protected as read only. The protected area is shown as below with different flash size. The protected areas are more flexible which may protect various area by setting CMP, BP0-BP4 bits.

Flash=512K*16						Memory Content(1 block=16KWord)			
CMP	BP4	BP3	BP2	BP1	BP0	Blocks	Address	Density	Portion
0	X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	0	1	31	0x7_C000 - 0x7_FFFF	16KWord	Upper 1/32
0	0	0	0	1	0	30 to 31	0x7_8000 - 0x7_FFFF	32KWord	Upper 1/16
0	0	0	0	1	1	28 to 31	0x7_0000 – 0x7_FFFF	64KWord	Upper 1/8
0	0	0	1	0	0	24 to 31	0x6_0000 – 0x7_FFFF	128KWord	Upper 1/4
0	0	0	1	0	1	16 to 31	0x4_0000 – 0x7_FFFF	256KWord	Upper 1/2
0	0	1	0	0	1	0	0x0_0000 – 0x0_3FFF	16KWord	Lower 1/32
0	0	1	0	1	0	0 to 1	0x0_0000 – 0x0_7FFF	32KWord	Lower 1/16
0	0	1	0	1	1	0 to 3	0x0_0000 – 0x0_FFFF	64KWord	Lower 1/8
0	0	1	1	0	0	0 to 7	0x0_0000 – 01_FFFF	128KWord	Lower1/4
0	0	1	1	0	1	0 to 15	0x0_0000 – 0x3_FFFF	256KWord	Lower 1/2
0	X	X	1	1	X	0 to 31	0x0_0000 – 0x7_FFFF	512KWord	ALL
0	1	0	0	0	1	31	0x7_FE00– 0x7_FFFF	0.5KWord	Top Block
0	1	0	0	1	0	31	0x7_FC00– 0x7_FFFF	1KWord	Top Block
0	1	0	0	1	1	31	0x7_F800– 0x7_FFFF	2KWord	Top Block
0	1	0	1	0	0	31	0x7_F000– 0x7_FFFF	4KWord	Top Block
0	1	1	0	0	1	0	0x0_0000 –0x0_0200	0.5KWord	Bottom Block
0	1	1	0	1	0	0	0x0_0000 –0x0_0400	1KWord	Bottom Block
0	1	1	0	1	1	0	0x0_0000 –0x0_0800	2KWord	Bottom Block
0	1	1	1	0	0	0	0x0_0000 –0x0_1000	4KWord	Bottom Block
1	X	X	0	0	0	0 to 31	0x0_0000 – 0x7_FFFF	512KWord	ALL
1	0	0	0	0	1	0 to 30	0x0_0000 - 0x7_BFFF	496KWord	Lower 31/32
1	0	0	0	1	0	0 to 29	0x0_0000 - 0x7_7FFF	480KWord	Lower 15/16
1	0	0	0	1	1	0 to 27	0x0_0000 - 0x6_FFFF	448KWord	Lower 7/8
1	0	0	1	0	0	0 to 23	0x0_0000 - 0x5_FFFF	384KWord	Lower 3/4
1	0	0	1	0	1	0 to 15	0x0_0000 - 0x3_FFFF	256KWord	Lower 1/2
1	0	1	0	0	1	1 to 31	0x0_4000 – 0x7_FFFF	496KWord	Upper 31/32
1	0	1	0	1	0	2 to 31	0x0_8000 – 0x7_FFFF	480KWord	Upper 15/16

1	0	1	0	1	1	4 to 31	0x1_0000 – 0x7_FFFF	448KWord	Upper 7/8
1	0	1	1	0	0	8 to 31	0x2_0000 – 0x7_FFFF	384KWord	Upper 3/4
1	0	1	1	0	1	16 to 31	0x4_0000 – 0x7_FFFF	256KWord	Upper 1/2
1	X	X	1	1	X	NONE	NONE	NONE	NONE
1	1	0	0	0	1	0 to 31	0x0_0000 - 0x7_FE00	511.5KWord	L-0.5KW
1	1	0	0	1	0	0 to 31	0x0_0000 - 0x7_FC00	511KWord	L-1KW
1	1	0	0	1	1	0 to 31	0x0_0000 - 0x7_F800	510KWord	L-2KW
1	1	0	1	0	0	0 to 31	0x0_0000 - 0x7_F000	508KWord	L-4KW
1	1	1	0	0	1	0 to 31	0x0_0200– 0x7_FFFF	511.5KWord	U-0.5KW
1	1	1	0	1	0	0 to 31	0x0_0400– 0x7_FFFF	511KWord	U-1KW
1	1	1	0	1	1	0 to 31	0x0_0800– 0x7_FFFF	510KWord	U-2KW
1	1	1	1	0	0	0 to 31	0x0_1000– 0x7_FFFF	508KWord	U-4KW

Flash=384K*16						Memory Content (1 block=16KWord)			
CMP	BP4	BP3	BP2	BP1	BP0	Blocks	Address	Density	Portion
0	X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	0	1	23	0x5_C000 - 0x5_FFFF	16KWord	Upper 1/24
0	0	0	0	1	0	22 to 23	0x5_8000 - 0x5_FFFF	32KWord	Upper 1/12
0	0	0	0	1	1	20 to 23	0x5_0000 – 0x5_FFFF	64KWord	Upper 1/6
0	0	0	1	0	0	16 to 23	0x4_0000 – 0x5_FFFF	128KWord	Upper 1/3
0	0	0	1	0	1	8 to 23	0x2_0000 – 0x5_FFFF	256KWord	Upper 2/3
0	0	1	0	0	1	0	0x0_0000 – 0x0_3FFF	16KWord	Lower 1/24
0	0	1	0	1	0	0 to 1	0x0_0000 – 0x0_7FFF	32KWord	Lower 1/12
0	0	1	0	1	1	0 to 3	0x0_0000 – 0x0_FFFF	64KWord	Lower 1/6
0	0	1	1	0	0	0 to 7	0x0_0000 – 01_FFFF	128KWord	Lower1/3
0	0	1	1	0	1	0 to 15	0x0_0000 – 0x3_FFFF	256KWord	Lower 2/3
0	X	X	1	1	X	0 to 23	0x0_0000 – 0x7_FFFF	384KWord	ALL
0	1	0	0	0	1	23	0x5_FE00– 0x5_FFFF	0.5KWord	Top Block
0	1	0	0	1	0	23	0x5_FC00– 0x5_FFFF	1KWord	Top Block
0	1	0	0	1	1	23	0x5_F800– 0x5_FFFF	2KWord	Top Block
0	1	0	1	0	0	23	0x5_F000– 0x5_FFFF	4KWord	Top Block
0	1	1	0	0	1	0	0x0_0000 –0x0_0200	0.5KWord	Bottom Block
0	1	1	0	1	0	0	0x0_0000 –0x0_0400	1KWord	Bottom Block
0	1	1	0	1	1	0	0x0_0000 –0x0_0800	2KWord	Bottom Block
0	1	1	1	0	0	0	0x0_0000 –0x0_1000	4KWord	Bottom Block
1	X	X	0	0	0	0 to 23	0x0_0000 – 0x5_FFFF	384KWord	ALL

1	0	0	0	0	1	0 to 22	0x0_0000 - 0x5_BFFF	368KWord	Lower 23/24
1	0	0	0	1	0	0 to 21	0x0_0000 - 0x5_7FFF	352KWord	Lower 11/12
1	0	0	0	1	1	0 to 19	0x0_0000 - 0x4_FFFF	320KWord	Lower 5/6
1	0	0	1	0	0	0 to 15	0x0_0000 - 0x3_FFFF	256KWord	Lower 2/3
1	0	0	1	0	1	0 to 7	0x0_0000 - 0x1_FFFF	128KWord	Lower 1/3
1	0	1	0	0	1	1 to 23	0x0_4000 – 0x5_FFFF	368KWord	Upper 23/24
1	0	1	0	1	0	2 to 31	0x0_8000 – 0x5_FFFF	352KWord	Upper 11/12
1	0	1	0	1	1	4 to 31	0x1_0000 – 0x5_FFFF	320KWord	Upper 5/6
1	0	1	1	0	0	8 to 31	0x2_0000 – 0x5_FFFF	256KWord	Upper 2/3
1	0	1	1	0	1	16 to 31	0x4_0000 – 0x5_FFFF	128KWord	Upper 1/3
1	X	X	1	1	X	NONE	NONE	NONE	NONE
1	1	0	0	0	1	0 to 23	0x0_0000 - 0x5_FE00	383.5KWord	L-0.5KW
1	1	0	0	1	0	0 to 23	0x0_0000 - 0x5_FC00	383KWord	L-1KW
1	1	0	0	1	1	0 to 23	0x0_0000 - 0x5_F800	382KWord	L-2KW
1	1	0	1	0	0	0 to 23	0x0_0000 - 0x5_F000	380KWord	L-4KW
1	1	1	0	0	1	0 to 23	0x0_0200– 0x5_FFFF	383.5KWord	U-0.5KW
1	1	1	0	1	0	0 to 23	0x0_0400– 0x5_FFFF	383KWord	U-1KW
1	1	1	0	1	1	0 to 23	0x0_0800– 0x5_FFFF	382KWord	U-2KW
1	1	1	1	0	0	0 to 23	0x0_1000– 0x5_FFFF	380KWord	U-4KW

7.6.5 ISP Registers

PERAM Registers

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PERAM (0x20)	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	-
default	-	-	-	-	-	-	-	-
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PERAM[7:0]							
R/W	R/W							
default	0							

BIT	Description
PERAM	PERAM Start address from 0xC00 for program ROM. Note: For page program, F/W set PERAM = 0x00 For word program, F/W set PERAM = 0x00~0xFF

Bank Num	Address Range	Description	Total Size (word)
12	0xC00~0xC03	WPU Channel RAM 00/User RAM/PERAM	4
	0xC04~0xC07	WPU Channel RAM 01/User RAM/PERAM	4
	---		84
	0xC5C~0xC5F	WPU Channel RAM 23/User RAM/PERAM	4
	0xC60~0xC7F	User RAM/PERAM	32
	0xC80~0xC87	WPU Channel RAM 00/User RAM/PERAM	8
	0xC88~0xC8F	WPU Channel RAM 01/User RAM/PERAM	8
	---		104
	0xCF8~0xCFF	WPU Channel RAM 15/User RAM/PERAM	8

PEROMH Registers

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PEROMH (0x21)	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	-
default	-	-	-	-	-	-	-	-
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	-	-	-	-	-	PEROM[18:16]		
R/W	-	-	-	-	-	R/W		
default	-	-	-	-	-	0		

BIT	Description
PEROM	Set up ISP flash address[18:16]

PEROML Registers

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PEROML (0x22)	PEROM[15:8]							
R/W	R/W							
default	0							
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PEROM[7:0]							
R/W	R/W							
default	0							

BIT	Description
PEROM	Set up ISP flash address[15:0]

PECMD Registers

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PECMD (0x23)	Write_En	CMP	BP4	BP3	BP2	BP1	BP0	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
default	0	0	0	0	0	0	0	-
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PECMD[7:0]							
R/W	W							
default	-							

BIT	Description
Write_En	Write Enable control bit 0: Flash Program/Erase disable 1: Flash Program/Erase enable
CMP/BP4/BP3/BP2/BP1/BP0	Write protect area Please refer to write protection
PECMD	ISP command set Page program PECMD = 0x5A Word program PECMD = 0x1E Sector erase PECMD = 0x96 Note: After write the command, F/W need to execute “NOP” instruction for three times During the program & erase process, CPU will hold clock until process is done.

```
…

/* Page Program Example */
#pragma data_address 0xC00
unsigned int data_buffer[0x80];

void SYS_Set_DataBuffer(unsigned int address, unsigned int data)
{
```

```
    data_buffer[address] = data;
}

Void SYS_ISP_Page_Start(unsigned int pageAddress)
{
   ISP_Page_Pro(pageAddress, &data_buffer[0]);                    // Page Program
}
```

7.7. Wave Processing Unit

The SNC85F provides two ways to play voice/sound. The first way is by 2/8~24 channel hardware channel and the second by 14-bit software channel.

The hardware channel is built-in the Wave Processing Unit. It is a high-performance multi-channel music synthesizer to provide high-quality wave-table melody playback. Many events of the standard MIDI file format are supported by a MIDI to Melody converter software tool.

The major function of wave synthesizer is to synthesis wave data from Flash area into voice. It is equipped with sampling rate counter, auto repetition function, and envelope control for each individual channel. With the help of the wave synthesizer, playing multi-channel music can be realized with little software effort.

The voice/sound algorithms support 4-bit HQDPCM, 5-bit HQDPCM, and 6-bit HQDPCM.

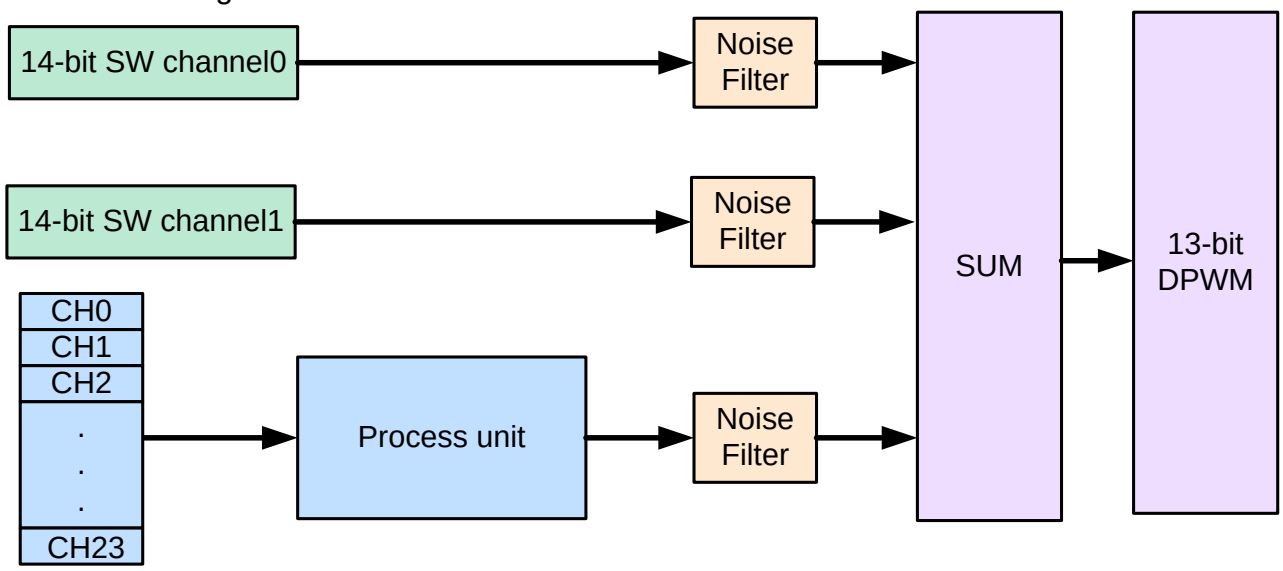
Wave Mark to trigger event in program is also supported.

The 14-bit software channel with SONiX HQDPCM algorithm is provided for high-quality sound and supports 3-bit HQDPCM, 4-bit HQDPCM, and 5-bit HQDPCM.

For better sound quality, the hardware channel and 14-bit high-quality software channel both include a noise filter.

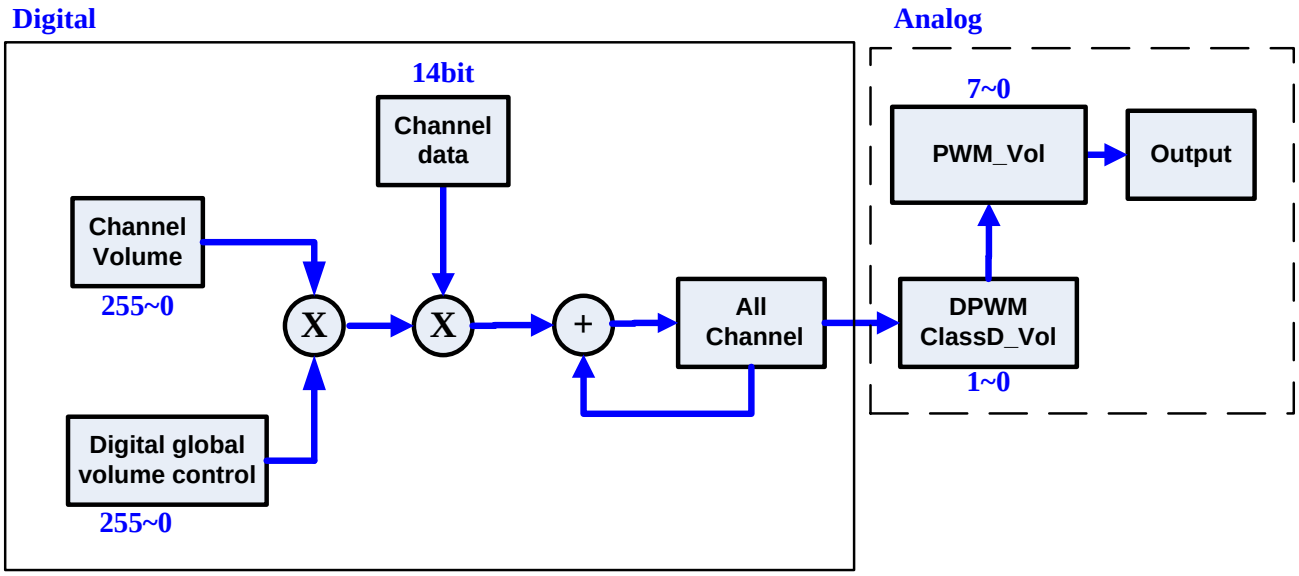
WPU	Channel Number (Max.)	Storage	Encode Type	Up-Sampling Filter	Sample Rate (Max).	Application
SNC85FxxxE Hardware CH	2	Internal Flash	4,5,6 bit HQDPCM	1,2,4X	64khz	Speech/Midi
SNC85FxxxE Hardware CH	2	**External SPI Flash**	4,5,6 bit HQDPCM	1,2,4X	32khz	Speech/Midi
SNC85FxxxA SNC85FxxxD Hardware CH	24	Internal Flash	4,5,6 bit HQDPCM	1,2,4X	64khz	speech/Midi
SNC85FxxxA SNC85FxxxD Hardware CH	8	**External SPI Flash**	4,5,6 bit HQDPCM	1,2,4X	28khz	speech/Midi
Software CH	2	Both	3,4,5bit HQDPCM	1,2,4X	24khz	Speech
	2	Both	Audio32	1,2,4X	16khz	Speech

Wave Processing Unit structure.



7.8. Volume control

There are four ways to control volume of SNC85F which are **channel volume, digital global volume, analog class D volume and analog PWM volume.**



ClassD_VOL	ClassD output
ClassD_VOL=1	6dB
ClassD_VOL=0	0db

PWM Volume control	AMP output
PWM_VOL=7	(Max output)*16/16
PWM_VOL=6	(Max output)*12/16
PWM_VOL=5	(Max output)*8/16
PWM_VOL=4	(Max output)*6/16
PWM_VOL=3	(Max output)*4/16
PWM_VOL=2	(Max output)*3/16
PWM_VOL=1	(Max output)*2/16
PWM_VOL=0	(Max output)*1/16

7.9. Input / Output Ports

The SNC85F offers considerable flexibility on the I/O ports. With the input or output designation of every pin fully under program control, pull-low 1MΩ@5V/ pull-low 100KΩ@5V/ floating options for all ports and provide wake-up function on all pins, the SNC85F has an I/O structure to meet the needs of a wide range of application possibilities.

Depending upon which device or package is chosen, the SNC85F provides from 16 to 31 bidirectional input/output lines labeled with port names P0, P1 etc. All of these I/O ports can be independently used for input and output operations and functions. Part of the I/O port provides high drive/sink currents that can directly drive an LED without requiring any external components.

I/O port supports four configurations for all GPIO:

PxMH	PxML	Port Mode
PxMH[n] = 0	PxML[n] = 0	Px.n as Input pull low 1MΩ(default)@5V
PxMH[n] = 0	PxML[n] = 1	Px.n as Input pull low 100KΩ@5V
PxMH[n] = 1	PxML[n] = 0	Px.n as Output
PxMH[n] = 1	PxML[n] = 1	Px.n as Input floating

7.9.1 Multi-Function of I/Os

The flexibility of the microcontroller range is greatly enhanced by the use of pins that have more than one function. Limited numbers of pins can force serious design constraints on designers however by supplying pins with multiple functions, many of these difficulties can be overcome. For some pins, the chosen function of the multi-function I/O pins is set by configuration options while for others, the function is set by application program control.
A summary of I/O multi-function is shown below.

SNC85F320D/SNC85F670D/SNC85F240D

	ICP_ Serial	RST	Xtal	ADC _ch	LVD_ Ext	INT	PWMA/B	SPI0	SPI1	I2C	UART	PWMIO	Touch key	CMP
P0.00			Xtal_ Xin								UART_RxD #1	PWMIO 00	Touch key00	
P0.01			Xtal_ Xout								UART_TxD #1	PWMIO 01	Touch key01	
P0.02							PWMAEn1 #0				UART_RxD #0	PWMIO 02	Touch key02	
P0.03				Ch0/ Vref		INT0 #1	PWMBEn1 #0				UART_TxD #0	PWMIO 03	Touch key03	
P0.04				Ch1						I2C_data #1		PWMIO 04	Touch key04	CMP +
P0.05				Ch2						I2C_clcok #1		PWMIO 05	Touch key05	CMP O
P0.06	ICP_ Data1	RST		Ch8								PWMIO 06	Touch key06	
P0.07				Ch9		INT1						PWMIO 07	Touch key07	
P0.08				Ch10	LVD_ Ext							PWMIO 08	Touch key08	
P0.09				Ch11		INT2						PWMIO 09	Touch key09	
P0.10	ICP_ Data0			Ch12			PWMAEn0 #0			I2C_data #0		PWMIO 10	Touch key10	
P0.11	ICP_ Clock			Ch13		INT0 #0	PWMBEn0 #0			I2C_clcok #0		PWMIO 11	Touch key11	
P0.12								MISO0 #0	MISO1 #1			PWMIO 12	Touch key12	
P0.13								CS0 #0	CS1 #1			PWMIO 13	Touch key13	
P0.14								SCK0 #0	SCK1 #1			PWMIO 14	Touch key14	
P0.15								MOSI0 #0	MOSI1 #1			PWMIO 15	Touch key15	
P1.00				Ch3				MISO0 #1	MISO1 #0			PWMIO 16	Touch key16	
P1.01				Ch4				CS0 #1	CS1 #0			PWMIO 17	Touch key17	
P1.02				Ch5				SCK0 #1	SCK1 #0			PWMIO 18	Touch key18	
P1.03				Ch6				MOSI0 #1	MOSI1 #0			PWMIO 19	Touch key19	
P1.04				Ch7								PWMIO 20	Touch key20	
P1.05							PWMBEn0 #1					PWMIO 21	Touch key21	
P1.06							PWMBEn1 #1					PWMIO 22	Touch key22	
P1.07							PWMAEn0 #1					PWMIO 23	Touch key23	
P1.08							PWMAEn1 #1					PWMIO 24	Touch key24	
P1.10												PWMIO 26	Touch key26	

P1.11												PWMIO 27	Touch key27	
P1.12												PWMIO 28	Touch key28	
P1.13												PWMIO 29	Touch key29	
P1.14												PWMIO 30	Touch key30	
P1.15 /ICE_ CSB												PWMIO 31	Touch key31	

SNC85F500E/SNC85F670E/SNC85F500A/SNC85F670E/SNC85F240A/SNC85F320A SNC85F240E/SNC85F320E

	ICP_ Serial	RST	Xtal	LVD_ Ext	INT	PWMA/B	SPI0	SPI1	I2C	UART	PWMIO	Touch key	CMP
P0.00			Xtal_ Xin							UART_RxD #1	PWMIO 00	Touch key00	
P0.01			Xtal_ Xout							UART_TxD #1	PWMIO 01	Touch key01	
P0.02						PWMAEn1 #0				UART_RxD #0	PWMIO 02	Touch key02	
P0.03					INT0 #1	PWMBEn1 #0				UART_TxD #0	PWMIO 03	Touch key03	
P0.04									I2C_data #1		PWMIO 04	Touch key04	CMP +
P0.05									I2C_clcok #1		PWMIO 05	Touch key05	CMP O
P0.06	ICP_ Data1	RST									PWMIO 06	Touch key06	
P0.07					INT1						PWMIO 07	Touch key07	
P0.08				LVD_ Ext							PWMIO 08	Touch key08	
P0.09					INT2						PWMIO 09	Touch key09	
P0.10	ICP_ Data0					PWMAEn0 #0			I2C_data #0		PWMIO 10	Touch key10	
P0.11	ICP_ Clock				INT0 #0	PWMBEn0 #0			I2C_clcok #0		PWMIO 11	Touch key11	
P0.12							MISO0 #0	MISO1 #1			PWMIO 12	Touch key12	
P0.13							CS0 #0	CS1 #1			PWMIO 13	Touch key13	
P0.14							SCK0 #0	SCK1 #1			PWMIO 14	Touch key14	
P0.15							MOSI0 #0	MOSI1 #1			PWMIO 15	Touch key15	
P1.00							MISO0 #1	MISO1 #0			PWMIO 16	Touch key16	
P1.01							CS0 #1	CS1 #0			PWMIO 17	Touch key17	
P1.02							SCK0 #1	SCK1 #0			PWMIO 18	Touch key18	
P1.03							MOSI0 #1	MOSI1 #0			PWMIO 19	Touch key19	
P1.04											PWMIO 20	Touch key20	
P1.05						PWMBEn0 #1					PWMIO 21	Touch key21	
P1.06						PWMBEn1 #1					PWMIO 22	Touch key22	
P1.07						PWMAEn0 #1					PWMIO 23	Touch key23	
P1.08						PWMAEn1 #1					PWMIO 24	Touch key24	
P1.10											PWMIO 26	Touch key26	
P1.11											PWMIO 27	Touch key27	

P1.12											PWMIO 28	Touch key28	
P1.13											PWMIO 29	Touch key29	
P1.14											PWMIO 30	Touch key30	
P1.15 /ICE_ CSB											PWMIO 31	Touch key31	

BIT	15	14	13	12	11	10	9	8
Timer1_IOSWAP	T1CLR	T1TO	T1TOS					
R/W	C1	R/C0	R/W					
default	**0**	**0**	0					
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
		IO_ PWMBEn	IO_ PWMAEn	IO_I2C	IO_SPI1	IO_SPI0	IO_UART	IO_INT0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W
default		0	0	0	0	0	0	0

IO_INT0:

IO_INT0 =0 =>INT0=P0.11

IO_INT0 =1 => INT0=P0.03

IO_UART

IO_INT0 =0 => UART_RxD=P0.02 UART_TXD=P0.03

IO_UART =1 =>UART_RxD=P0.00 UART_TXD=P0.01

IO_SPI0:

IO_SPI0=0 => MISO0=P0.12 CS0=P0.13 SCK0=P0.14 MOSI0=P0.15

IO_SPI0=1 => MISO0=P1.00 CS0=P1.01 SCK0=P1.02 MOSI0=P1.03

IO_SPI1:

IO_SPI1=0 => MISO1=P1.00 CS1=P1.01 SCK1=P1.02 MOSI1=P1.03

IO_SPI1=1 => MISO1=P0.12 CS0=P1.13 SCK1=P0.14 MOSI1=P0.15

IO_I2C:

IO_I2C=0 => I2C_Clock=P0.11 I2C_Data=P0.10

IO_I2C=1 => I2C_Clock=P0.05 I2C_Data=P0.04

IO_ PWMAEn:

IO_ PWMAEn=0 =>PWMAEN0=P0.10 PWMAEN1=P0.02

IO_ PWMAEn=1 =>PWMAEN0=P1.07 PWMAEN1=P1.08

IO_ PWMBEn:

IO_ PWMBEn=0 =>PWMBEN0=P0.11 PWMBEN1=P0.03

IO_ PWMBEn=1 =>PWMBEN0=P1.05 PWMBEN1=P1.06

7.10. Timer

7.10.1 Timer1

Timer1 is a special timer that provides either 4ms or 1ms time out flag. The timer also has its own interrupt service(vector).

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Timer1_IOSWAP (0x4A)	T1CLR	T1TO	T1TOS					
R/W	C1	R/C0	R/W					
default	0	0	0					
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		IO_PWMBEn	IO_PWMAEn	IO_I2C	IO_SPI1	IO_SPI0	IO_UART	IO_INT0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W
default		0	0	0	0	0	0	0

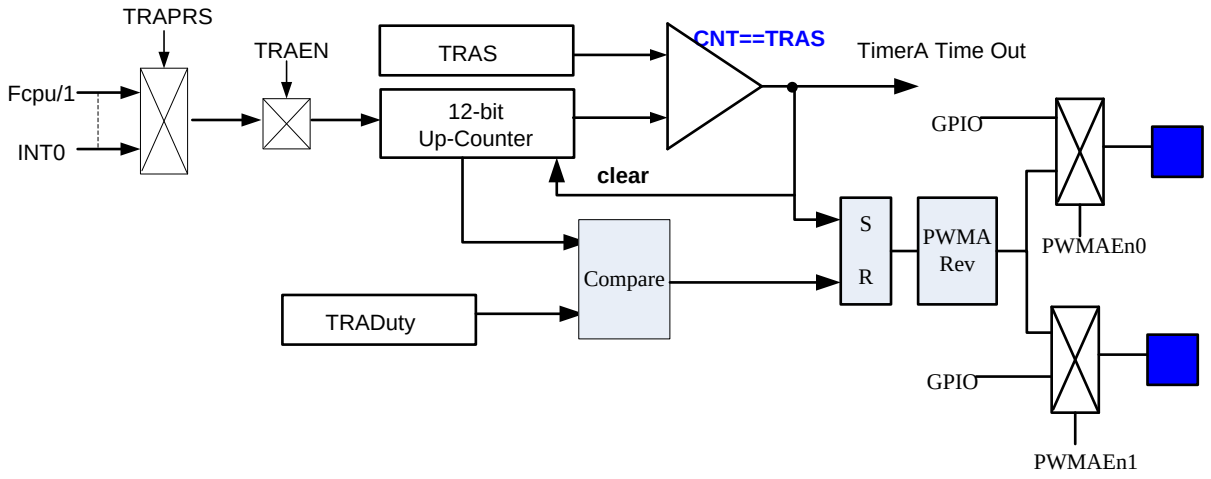
BIT	Description
T1CLR	Clear Timer1 count Write T1Clr with 1 will clear it's counting value. The T1CLR is not readable (the value is always "0")
T1TO	Timer1 timeout flag T1TO=1: Timer 1 time out. Write 0 will clear this time out flag. If user needs to set other bit of this register, please be aware to write 1 into this bit, else, Time out flag might have chance to be clear before recognize.
T1TOS	Timer1 timeout select 0: 1ms 1: 4ms

7.10.2 TimerA 12-bit Timer/Counter

TimerA is a special timer. It is an 12-bit binary up-counting timer with auto-reload function or event counter function, as well as perform IR and PWM output functions. If a successful event occurs (counting value = set value), it will issue a time out signal to TimerA interrupt service and continue counting.

The TimerA features include as below,

1. 12-bit up counter with interrupt function.
2. External interrupt 0 (INT0) counter.
3. IR modulation. Duty cycle can be programmable 1/2, 2/3, 1/3, 1/4.
4. PWMIO output.



TRA: TimerA Control Register

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
TRA (0x3C)	TRAEN	TRAPRS[2:0]			TRAS[11:8]			
R/W	R/W	R/W			R/W			
default	0	000			0000			
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	TRAS[7:0]							
R/W	R/W							
default	0000,0000							

BIT	Description
TRAEN	TimerA enable 0: disable 1: enable
TRAPRS[2:0]	TimerA pre-scale

TRAPRS[2:0]		
000b	Fcpu/1	12288KHz
001b	Fcpu/2	6144KHz
010b	Fcpu/8	192KHz
011b	Fcpu/64	96KHz
100b	Fcpu/256	48KHz
101b	source from external INT0	
110b	Reserve	
111b	Reserve	

TRAS[11:0]	TimerA up-count expect value. Write: setting expect counting limit value Read: up-counting value

The TRAS register records TimerA counter value, which can control time-out time of TimerA. When TRAEN=1, TimerA will start count from 0 to this counting limit value. If a successful event occurs (counting value = limit value), it will restart counting and issue a time out signal (INTRQ). If TRAINTEN=1 and GIE=1, it will enter TimerA interrupt service routine.
Note. Write zero into TRAS[11:0] register is prohibited.

TRAPWM: PWMIO or IR Control Register

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
TRAPWM (0x3C)	PWMAEN1	PWMAEN0	PWMAREV	TRAAR	PWMADUTY[11:8]			
R/W	R/W	R/W	R/W	R/W	R/W			
default	0	0	0	0	0000			
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PWMADUTY[7:0]							
R/W	R/W							
default	0000,0000							

BIT	Description
PWMAEN0	PWMAEN0 or IR enable 0: Disable(Normal GPIO) 1: PWMAEN0 or IR output enable

PWMAEN1	PWMAEN1 or IR enable 0: Disable(Normal GPIO) 1: PWMAEN1 or IR output enable
PWMAREV	PWMA output reverse 0: Normal 1: Output reverse
TRAAR	TimerA audio reload 0: Disable auto reload 1: Enable audo reload
PWMA Duty[11:0]	PWMA duty register

IR Output Setting

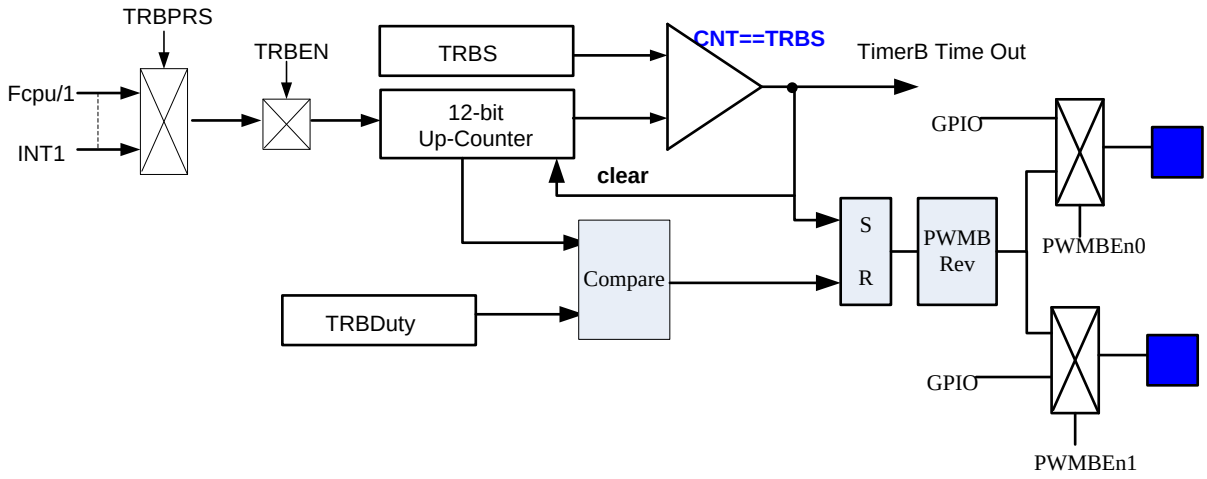
TRAPRS[2:0]	TRAS[7:0]	IR freq	DUTY[11:0]		
			1/2 duty	2/3 duty	1/3 duty
001b (Fcpu/2)	160	38.4KHz	80	106	53

7.10.3 TimerB 12-bit Timer/Counter

TimerB is a general-purpose timer. It is an 12-bit binary up-counting timer with auto-reload function and event counter function. If a successful event occurs (counting value = setting value), it will issue a time out signal to TimerB interrupt service and continue counting. Two clock sources contain CPU clock and external clock can be selected to be timer's clock source.

The TimerB features include as below

1. 12-bit up counter with interrupt function
2. External interrupt (INT1) counter
3. IR module, 1/2 duty, 2/3, 1/3, 1/4 duty
4. PWMBEn0 / PWMBEn1 output to control DC motor



BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
TRB (0x3E)	TRBEN	TRBPRS[1:0]			TRBS[11:8]			
R/W	R/W	R/W			R/W			
default	0	000			0000			
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	TRBS[7:0]							
R/W	R/W							
default	0000,0000							

BIT	Description
TRBEN	TimerB enable 0: disable 1: enable
TRBPRS[2:0]	TimerB pre-scale

TRBPRS[2:0]		
000b	Fcpu/1	12288KHz
001b	Fcpu/2	6144KHz
010b	Fcpu/8	1536KHz
011b	Fcpu/64	192KHz
100b	Fcpu/256	48KHz
101b	source from external INT1	
110b	Reserve	
111b	Reserve	

TRBS[11:0]	TimerB count value Write: setting expect counting limit value Read: up-counting value When counting value = setting value, up-counter will be reset. Maximum is 4095.

The TRBS register records TimerB counter value, which can control time-out time of TimerB. When TRBEN=1, TimerB will start count from 0 to this counting limit value. If a successful event occurs (counting value = limit value), it will restart counting and issue a time out signal (INTRQ). If TRBINTEN=1 and GIE=1, it will enter TimerB interrupt service routine.
Note. Write zero into TRBS[11:0] register is prohibited.

TRBPWM: PWMIO or IR Control Register

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
TRAPWM (0x3C)	PWMBEN1	PWMBEN0	PWMBREV	TRBAR	PWMBDUTY[11:8]			
R/W	R/W	R/W	R/W	R/W	R/W			
default	0	0	0	0	0000			
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PWMBDUTY[7:0]							
R/W	R/W							
default	0000,0000							

BIT	Description
PWMBEN0	PWMBEN0 or IR enable 0: Disable(Normal GPIO) 1: PWMBEN0 or IR output enable
PWMBEN1	PWMBEN1 or IR enable 0: Disable(Normal GPIO) 1: PWMBEN1 or IR output enable

PWMBREV	PWMB output reverse 0: Normal 1: Output reverse
TRBAR	TimerB audio reload 0: Disable auto reload 1: Enable audo reload
PWMB Duty[11:0]	PWMB duty register

IR Output Setting

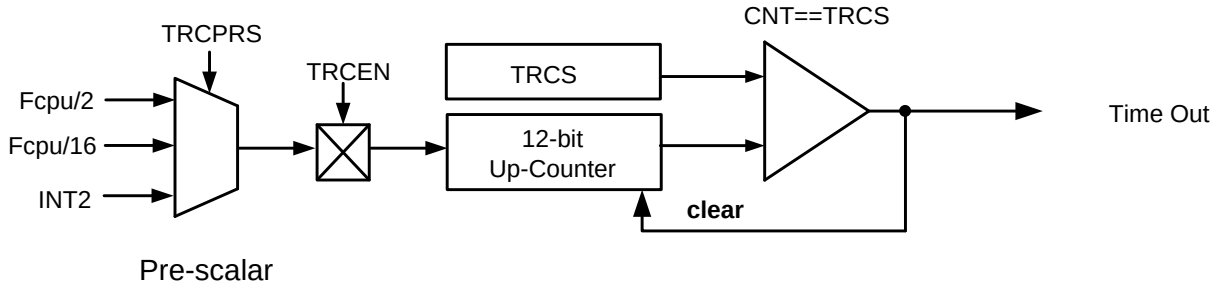
TRBPRS[2:0]	TRBS[7:0]	IR freq	DUTY[11:0]		
			1/2 duty	2/3 duty	1/3 duty
001b (Fcpu/2)	160	38.4KHz	80	106	53

7.10.4 TimerC 12-bit Timer/Counter

TimerC is a general-purpose timer. It is an 12-bit binary up-counting timer with auto-reload function and event counter function. If a successful event occurs (counting value = setting value), it will issue a time out signal to TimerC interrupt service and continue counting. Two clock sources contain CPU clock and external clock can be selected to be timer's clock source.

The TimerC features include as below,

1. 12-bit up counter with interrupt function.
2. External interrupt (INT2) counter.



BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
TRC (0x3F)	TRCEN	TRCAR	TRCPRS[1:0]		TRCS[11:8]			
R/W	R/W	R/W	R/W		R/W			
default	0	0	00		0000			
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	TRCS[7:0]							
R/W	R/W							
default	0000,0000							

BIT	Description
TRCEN	TimerC enable 0: disable 1: enable
TRCAR	TimerC auto reload 0: disable auto reload 1: enable auto reload

<table>
<tr><td>TRCPRS[1:0]</td><td>TimerC pre-scale
<table>
<tr><th>TRCPRS[1:0]</th><th></th><th>IHRC: 24.576MHz</th></tr>
<tr><td>00b</td><td>Fcpu/2</td><td>6144KHz</td></tr>
<tr><td>01b</td><td>Fcpu/16</td><td>768KHz</td></tr>
<tr><td>1Xb</td><td colspan="2">source from external INT2</td></tr>
</table></td></tr>
<tr><td>TRCS[11:0]</td><td>TimerC count value
Write: setting expect counting limit value
Read: up-counting value
When counting value = setting value, up-counter will be reset. Maximum is 4095.</td></tr>
</table>

Note. Write zero into TRCS[11:0] register is prohibited.

7.10.5 WDT timer

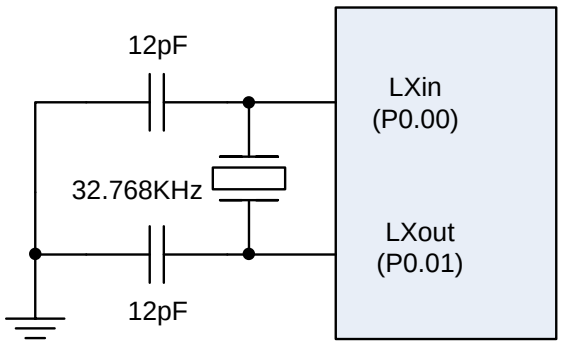
The Watch Dog Timer will reset the chip when watchdog time-out counter is not cleared yet before WDT time-out flag is issued. The duration of WDT time-out time is 0.25s.

User can through Sonix provides library to easy setting function.

Function	Library Name	Input	Return	Function Description
Watch dog timer	**sys_ClrWDT();**			Clear WDT counter
	sys_ClrWDT_TO();			Clear WDT timeout flag
	sys_ChkWDT_TO();		0/1	Get WDT timeout flag Return 0: WDT not timeout Return 1: WDT timeout

7.10.6 Real Time Clock (RTC)

The SNC85F has a built-in 32.768KHz oscillator circuit for Real Time Clock (RTC) function. The RTC timer provides an accurate timer for digital clock use. A 32.768KHz crystal should be connected to XTAL by shared IO inputs P0.00 and P0.01. In IDLE mode, the chip will wake up for a regular interval time by RTC timer set. RTC timer range selections of between 62.5ms to 64sec are supported.

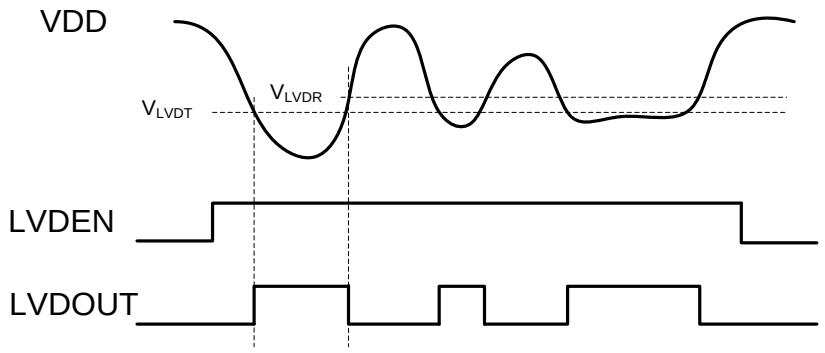


32.768K X'tal circuit

Function	Library Name	Input	Return	Function Description
RTC	**sys_RTC62p5ms();**	CNT		Set RTC Timer timeout = 62.5ms * (CNT+1) CNT: 0 ~ 15
	sys_RTC125ms();	CNT		Set RTC Timer timeout = 125ms * (CNT+1) CNT: 0 ~ 15
	sys_RTC250ms();	CNT		Set RTC Timer timeout = 250ms * (CNT+1) CNT: 0 ~ 15
	sys_RTC500ms();	CNT		Set RTC Timer timeout = 500ms * (CNT+1) CNT: 0 ~ 15
	sys_RTC1sec();	CNT		Set RTC Timer timeout = 1sec * (CNT+1) CNT: 0 ~ 15
	sys_RTC2sec();	CNT		Set RTC Timer timeout = 2sec * (CNT+1) CNT: 0 ~ 15
	sys_RTC4sec();	CNT		Set RTC Timer timeout = 4sec * (CNT+1) CNT: 0 ~ 15
	sys_ChkRTC_TO();		0/1	Check RTC timeout flag Return 0: not timeout Return 1: RTC timeout
	sys_ClrRTC_TO();			Clear RTC timeout flag
	sys_Dis_RTC();			Disable RTC Timer

7.11. Low Voltage Detector (LVD)

The SNC85F has a Low Voltage Detector (LVD) for power management. This feature is favorable to product battery life requirements and can be an effective management of system power. The device provides 8 software programmable voltage levels to detect low voltage events 2.0/2.2/2.4/2.6/2.8/3.0/3.2/3.4V The LVD function compares the power supply voltage VDD, with a pre-specified voltage level stored in the register. When the power supply voltage VDD falls below this pre-determined value, the LVDOUT bit will be set high indicating a low power supply voltage condition. When the device is powered down the low voltage detector will remain active if the LVDEN bit is high.



LVD Operation

Note the LVD detect has a voltage window of about 0.1V. When LVD level = 2.4V, and VDD supply falls lower than 2.4V, the LVD will trigger LVD (V_{LVDT}). When VDD supply rises higher than 2.5V, LVD (V_{LVDR}) will be released. The LVD function does not operate in sleep or idle modes and is recommended to turn off the LVD function in these modes to reduce power consumption.

7.12. External Interrupt (INT0 & INT1 & INT2)

INT0(P0.03/P0.11) & INT1(P0.07) & INT2(P0.09) are external interrupt trigger sources and build in edge trigger Mode. If external interrupt control bit enabled and enable trigger mode and external edge trigger occurs, the external interrupt request flag will be set to “1”. The program counter will jump to the interrupt vector (INT0 → 0x1C, INT1 → 0X20, INT2 → 0X2C) and execute interrupt service routine.

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PWMChINTM (0x41)	-		INT2M		INT1M		INT0M	
R/W	-		R/W		R/W		R/W	
default	xx		00		00		00	
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	-		PWMChNum[5:0]					
R/W	-		R/W					
default	xx		000000					

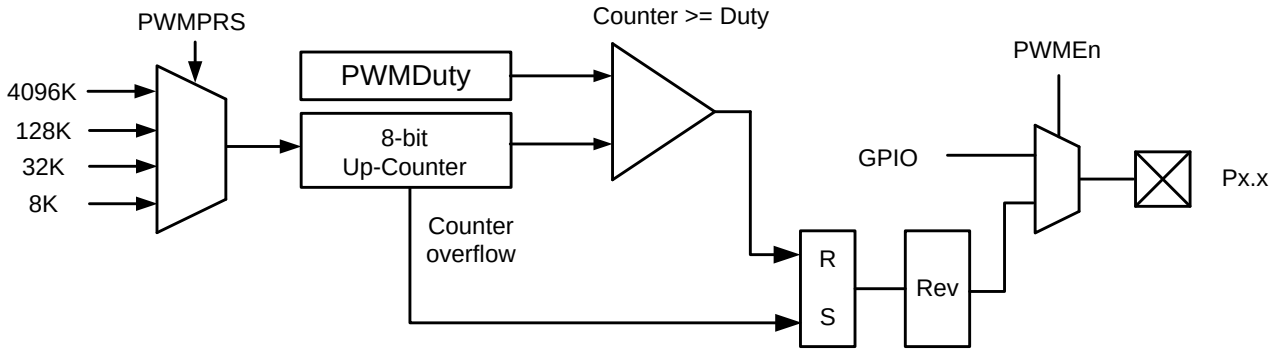
Note. IO can only be triggered when input mode.

BIT	Description
INT0M[1:0]	External0 interrupt mode select 00: P0.03/P0.11 is GPIO. Disable. 01: P0.03/P0.11 is INT0. Trigger when positive edge. 10: P0.03/P0.11 is INT0. Trigger when negative edge. 11: P0.03/P0.11 is INT0. Trigger when both edge. If enable INT0 trigger mode and TimerA’s TRAPRS=5, the INT0 is Event count mode (external clock by P0.03/P0.11)
INT1M[1:0]	External1 interrupt mode select 00: P0.07 is GPIO. Disable. 01: P0.07 is INT1. Trigger when positive edge. 10: P0.07 is INT1. Trigger when negative edge. 11: P0.07 is INT1. Trigger when both edge. If enable INT1 trigger mode and TimerB’s TRBPRS=5, the INT1 is Event count mode (external clock by P0.07)
INT2M[1:0]	External2 interrupt mode select

	00: P0.09 is GPIO. Disable. 01: P0.09 is INT2. Trigger when positive edge. 10: P0.09 is INT2. Trigger when negative edge. 11: P0.09 is INT2. Trigger when both edge. If enable INT2 trigger mode and TimerC's TRAPRS=2, the INT2 is Event count mode (external clock by P0.09)

7.13. Pulse Width Modulation (PWMIO)

The SNC85F supports up to Max.31 PWMIOs. Each I/O has an 8-bit independent duty register. The clock source of PWMIO is selected by PWMPRS[1:0] which provides 4096KHz, 128KHz, 32KHz, or 8KHz frequencies. Each PWMIO provides high drive/sink currents that can directly drive an LED without requiring external components.



BIT	15	14	13	12	11	10	9	8
PWMCR0	**PWMCLR**	**BIT_REV**	**PWMPRS[1:0]**		**PWMEnCLR**			
R/W	**C0**	**R/W**	**R/W**		**C1**			
default	**1**	**0**	**00**		**0**			
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
								PWMIOEn
R/W								**R/W**
default								**0**

BIT	*Description*
PWMIOEn	PWMIO enable/disable control. The PWMIOEn control the PWMIO which is assigned by PWMChNum[5:0]. 0: disable 1: enable Note. It should use BSET/BCLR instruction to set this bit. (Ex: PWMCR0 = BSET.0 PWMCR0)
PWMEnCLR	Clear all PWMIOEn Write 1: Disable all PWMIO Write 0: No operation

PWMPRS***[1:0]***	PWMIO clock pre-scalar **PWMPRS[1:0] / PWMIO Clock Source / PWMIO Cycle** 00b / 0.244us (4096KHz) / 62.5us (16KHz) 01b / 7.8125us (128KHz) / 2ms (500Hz) 10b / 31.25us (32KHz) / 8ms (125Hz) 11b / 125us (8KHz) / 32ms (31.25Hz)
BIT_REV	PWMIO output reverse 0: Normal 1: PWM output reverse Note. Setting BIT_REV must be when PWMIOEN is disabled.
PWMCLR	PWMIO counter clear Write 0 to clear the PWM counter Always read 1

■ **PWMIO Duty Register**

Each PWMIO has an individual register (PWMDutyx) to set the duty. The PWM IO re-loads the data only at counter initialization.

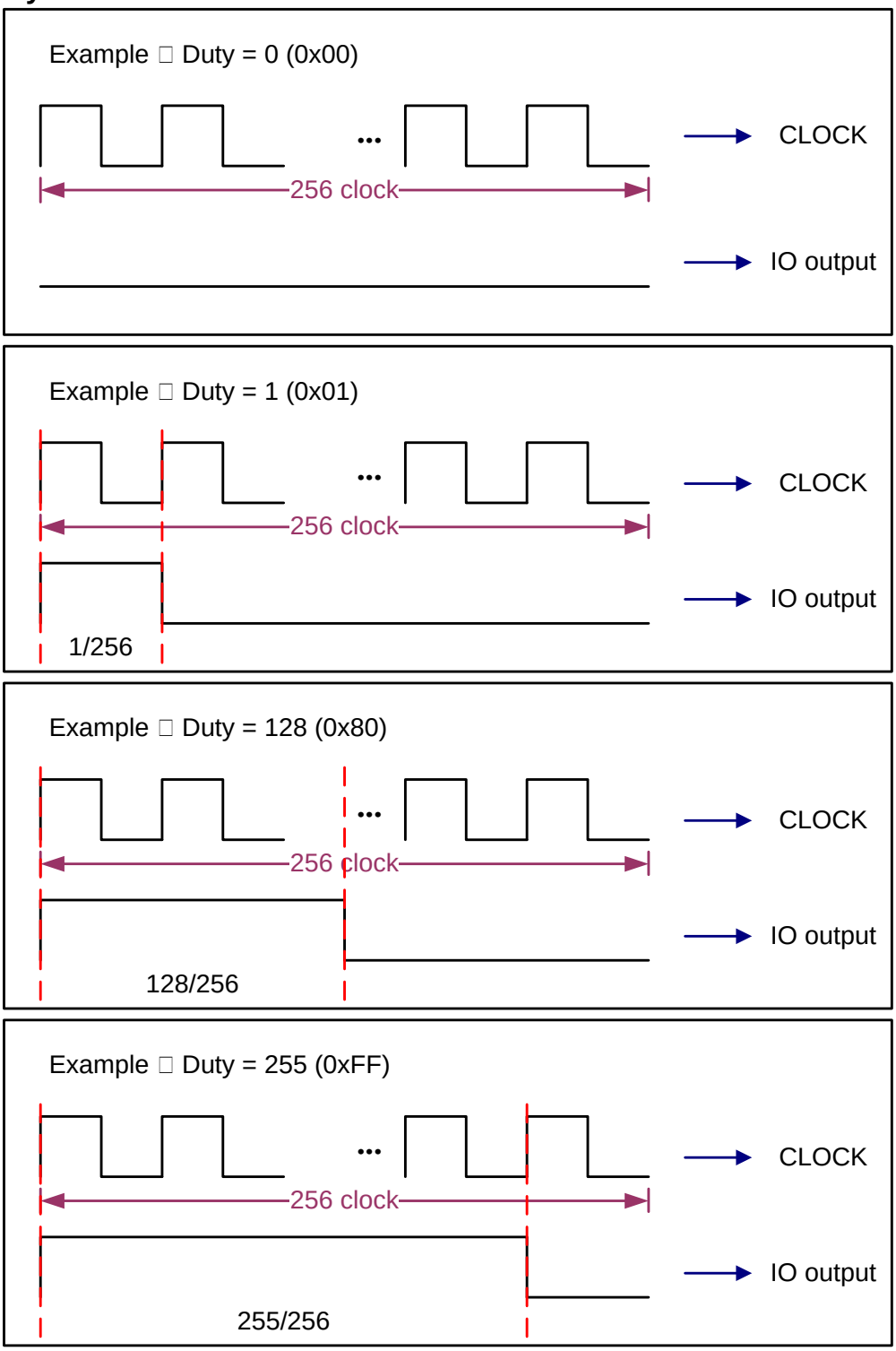
BIT	15	14	13	12	11	10	9	8
PWMCh_INTM			INT2M		INT1M		INT0M	
R/W			R/W		R/W		R/W	
default			00		00		00	

BIT	7	6	5	4	3	2	1	0
			PWMChNum[5:0]					
R/W			**R/W**					
default			**000000**					

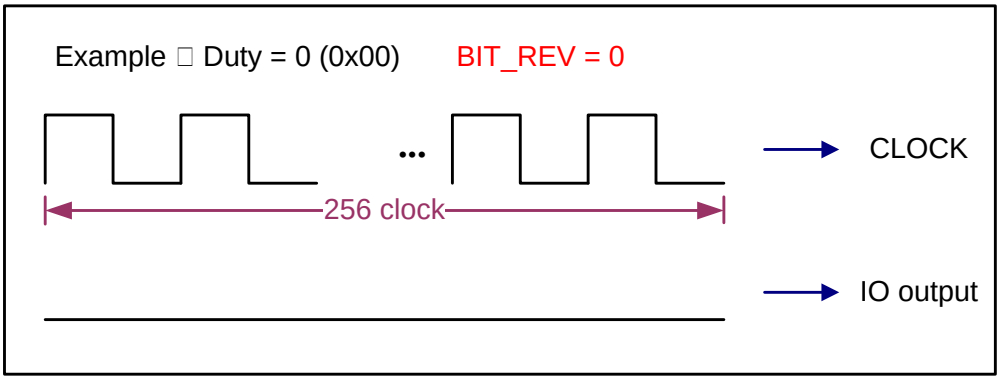
BIT	15	14	13	12	11	10	9	8
PWMDuty	**-**							
R/W	**-**							
default	**-**							

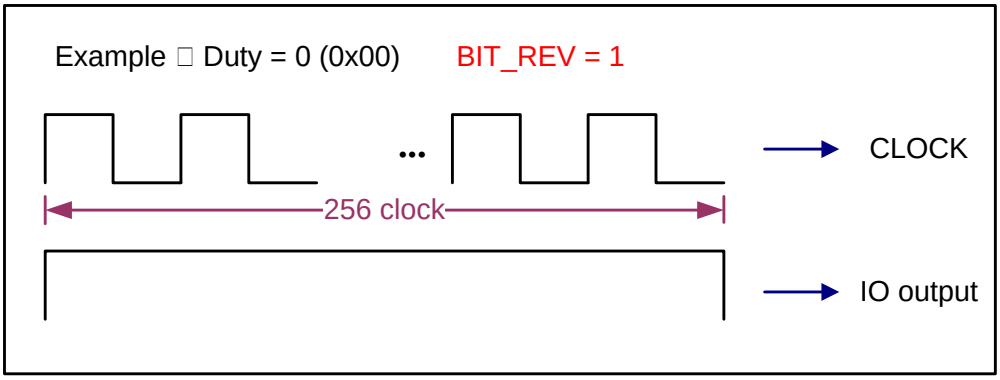
BIT	7	6	5	4	3	2	1	0
	PWMDuty[7:0]							
R/W	**R/W**							
default	**00000000**							

PWMIO Duty control:

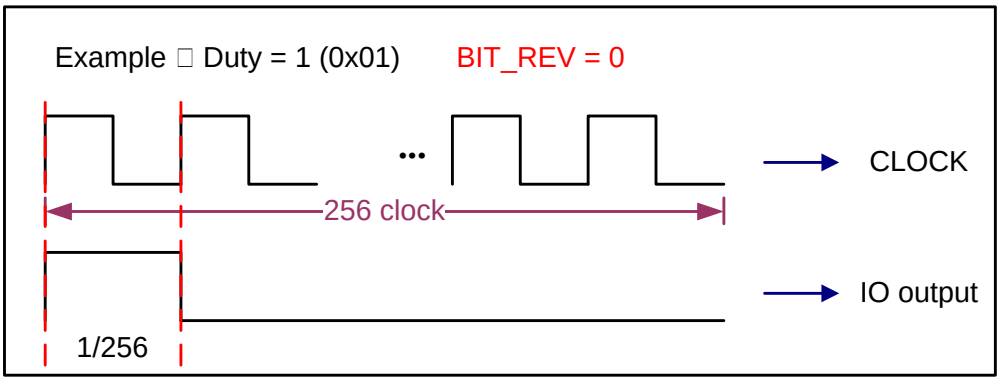


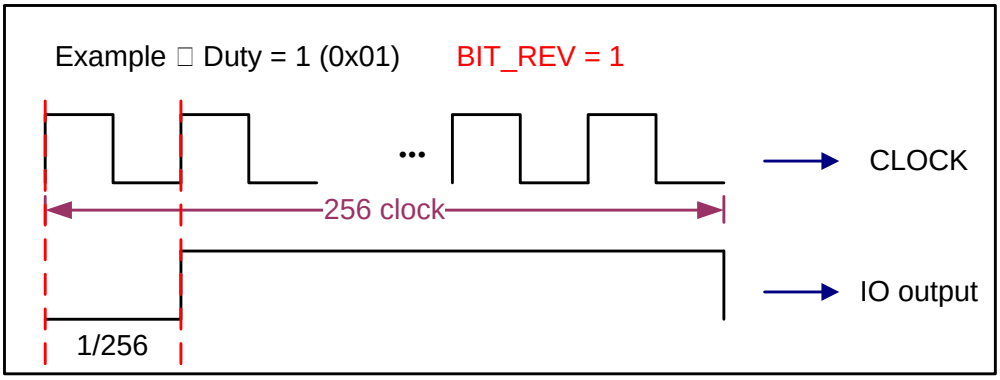
SNC85F have support PWMIO IO output reverse. If use sink mode LED, user can set BIT_REV = 1.

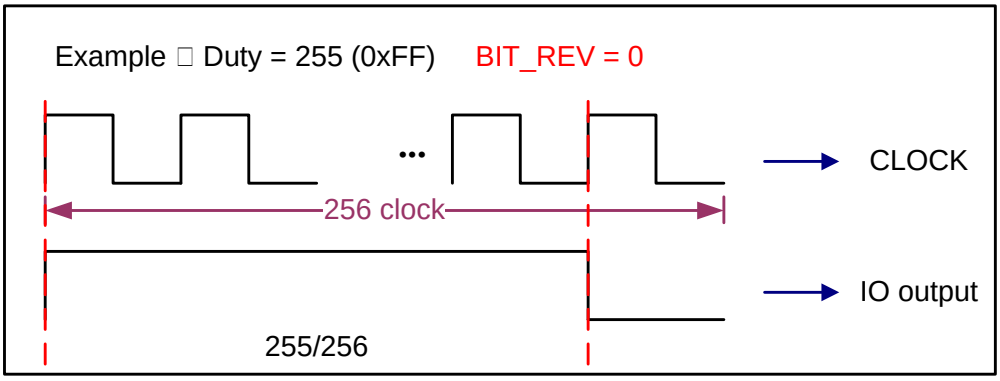


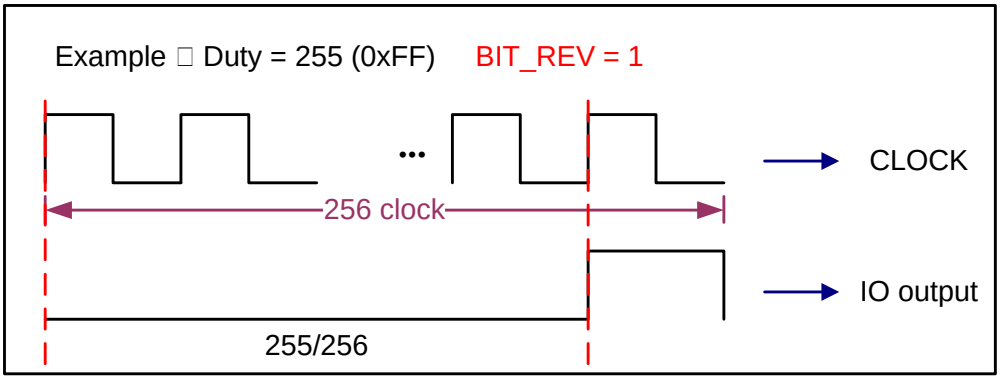


Note. Set BIT_REV = 1 and Duty = 0 to let sink mode LED completely low.






Example □ Duty = 255 (0xFF)
BIT_REV = 0
CLOCK
256 clock
IO output
255/256


Example □ Duty = 255 (0xFF)
BIT_REV = 1
CLOCK
256 clock
IO output
255/256

7.14. Serial Peripheral Interface 0 (SPI0, Master mode/Slave mode)

The SNC85F supports two SPI interface SPI0 and SPI1. SPI0 is dedicated for connecting with an external SPI flash. The other SPI1 is dedicated for module connection such as, G-sensor or 2.4 GHz RF module.

Function comparison between SPI0 and SPI1:

SPI0	SPI1
Master mode & Slave mode	Only Master mode
Transmit FIFO: 8 bytes	Transmit FIFO: 2 bytes
With interrupt function	Without interrupt
Maximum running speed Master mode:12.288Mhz Slave mode:6.144Mhz	Maximum running speed Master mode:12.288Mhz
IO port: IO_SPI0=0 MISO0=P0.12 CS0=P0.13 SCK0=P0.14 MOSI0=P0.15 IO_SPI0=1 MISO0=P1.00 CS0=P1.01 SCK0=P1.02 MOSI0=P1.03	IO port: IO_SPI1=0 MISO1=P1.00 CS1=P1.01 SCK1=P1.02 MOSI1=P1.03 IO_SPI1=1 MISO1=P0.12 CS0=P1.13 SCK1=P0.14 MOSI1=P0.15

The SPI peripheral is a synchronous, 4-wire interface consisting of two data pins (MOSI0 and MISO0), slave select pins (CS0); and a synchronous clock pin (SCK0). The two data pins permit full-duplex and half-duplex operation to other SPI-compatible devices. The SPI also includes programmable baud rates, clock phase (CPHA), and clock polarity (CPOL).

Devices communicate using a master/slave relationship, in which the master initiates the data transfer by writing to transmit data buffer (SPIDATA0~7) and bits to be transfer (SPITRANSFER). When the master generates a clock and selects a slave device, data may be transferred in both directions simultaneously. In the master SPI, bits are sent out of the MOSI0 pin and received in the MISO0 pin. Bits to be shifted out are stored in the SPI internal shift register SPIDATA[0:7] and are sent out most significant bit (bit 7) first . When bit 7 of the master is shifted out through MOSI0 pin, a bit from bit 7 of the slave is being shifted into bit 0 of the master via the MISO0 pin. After 8 clock pulses or shifts, this bit will eventually end up in bit 7 of the master.

7.14.1 SPI Control Register (SPICTRL)

BIT	15	14	13	12	11	10	9	8
	-	MSMode	-	-	-	-	CPHA	CPOL
R/W	-	R/W	-	-	-	-	R/W	R/W
default	-	0	-	-	-	-	0	0
BIT	7	6	5	4	3	2	1	0
	SPIEN	-	-	-	INTNum[2:0]			START
R/W	R/W	-	-	-	R/W			R/W
default	0	-	-	-	000			0

Bit	*Name*	*Description*
14	MSMode	SPI Master/Slave Mode 0: master 1: slave
9	CPHA	Clock phase 0: Data change at clock falling, latch at clock rising when CPOL = 0; Data change at clock rising, latch at clock falling when CPOL = 1. 1: Data change at clock rising, latch at clock falling when CPOL = 0; Data change at clock falling, latch at clock rising when CPOL = 1.
8	CPOL	Clock polarity 0: Clock idles at low 1: Clock idles at high
7	SPIEN	SPI module enable control 0: disable, 1: enable
3:1	INTNum[2:0]	SPI0 occurs interrupt timing INTNum[2:0]=0 transmission/ receive byte==1 occurs SPI0 interrupt INTNum[2:0]=1 transmission/ receive byte==2 occurs SPI0 interrupt INTNum[2:0]=2 transmission/ receive byte==3 occurs SPI0 interrupt .. INTNum[2:0]=7 transmission/ receive byte==8 occurs SPI0 interrupt
0	START	Set this bit to START SPI transfer/received, auto clear after operation finished. 0: STOP, 1: START

7.14.2 SPI Baud Rate Register (SPIBR)

BIT	15	14	13	12	11	10	9	8
	-	-	-	-	-	SPIPRS[2:0]		
R/W	-	-	-	-	-	R/W		
default	-	-	-	-	-	000		
BIT	7	6	5	4	3	2	1	0
	SPIDIV[7:0]							
R/W	R/W							
default	0000,0000							

Bit	*Name*	*Description*
14	MSMode	SPI Master/Slave Mode 0: master 1: slave
10:8	SPIPRS[2:0]	SPIPRS[2:0], SPI0 pre-scalar clock System clock=12.288Mhz SPIPRS[2:0]=0, SPI0 pre-scalar clock=12.288Mhz SPIPRS[2:0]=1, SPI0 pre-scalar clock=6.144Mhz … SPIPRS[2:0]=7, SPI0 pre-scalar clock=48Khz
7:0	SPIDIV[7:0]	SPIDIV[7:0]=0~255 SPI clock = SPI0 pre-scalar clock/ (SPIDIV[7:0]+1) Example System clock=12.288Mhz SPIPRS[2:0]=0, SPI0 pre-scalar clock=12.288Mhz SPIDIV[7:0]=0 SPI clock = SPI0 pre-scalar clock/ (SPIDIV[7:0]+1)=12.288M/(0+1) =12.288Mhz

Note: When the SPI is in Slave mode, the maximum running speed is system clock/2

Example:

System clock=12.288Mhz

Slave mode max. SPI clock= 12.288Mhz/2=6.144Mhz

7.14.3 SPIDATABuf(SPI Transmit and Receive Data Buffer)

SPIDATA0~SPIDATA7 is used for transfer and receive data buffer for SPI. For each operation, all the data in this register will be shifted out to the MOSI0 pin one by one, while at the same time, data will be shifted in from the MISO0 pin. After the operation has finished, the received data can be examined in this register

BIT	15	14	13	12	11	10	9	8
	-	-	-	-	-			
R/W	-	-	-	-	-			
default	-	-	-	-	-			
BIT	7	6	5	4	3	2	1	0
	SPIDATA0[7:0]							
R/W	R/W							
default	0000,0000							

BIT	15	14	13	12	11	10	9	8
	-	-	-	-	-			
R/W	-	-	-	-	-			
default	-	-	-	-	-			
BIT	7	6	5	4	3	2	1	0
	SPIDATA1[7:0]							
R/W	R/W							
default	0000,0000							

…

BIT	15	14	13	12	11	10	9	8
	-	-	-	-	-			
R/W	-	-	-	-	-			
default	-	-	-	-	-			
BIT	7	6	5	4	3	2	1	0
	SPIDATA7[7:0]							
R/W	R/W							
default	0000,0000							

7.14.4 SPI bit Transfer (SPITRANSFER)

This register is used to identify the amounts of bit from data buffer to be transferred.

BIT	15	14	13	12	11	10	9	8
	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	-
default	-	-	-	-	-	-	-	-
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	-	TF[6:0]						
R/W	-	R/W						
default	-	000,0000						

Example:

TF[6:0]=64, there are 64-bits (8 bytes) will be transfer.

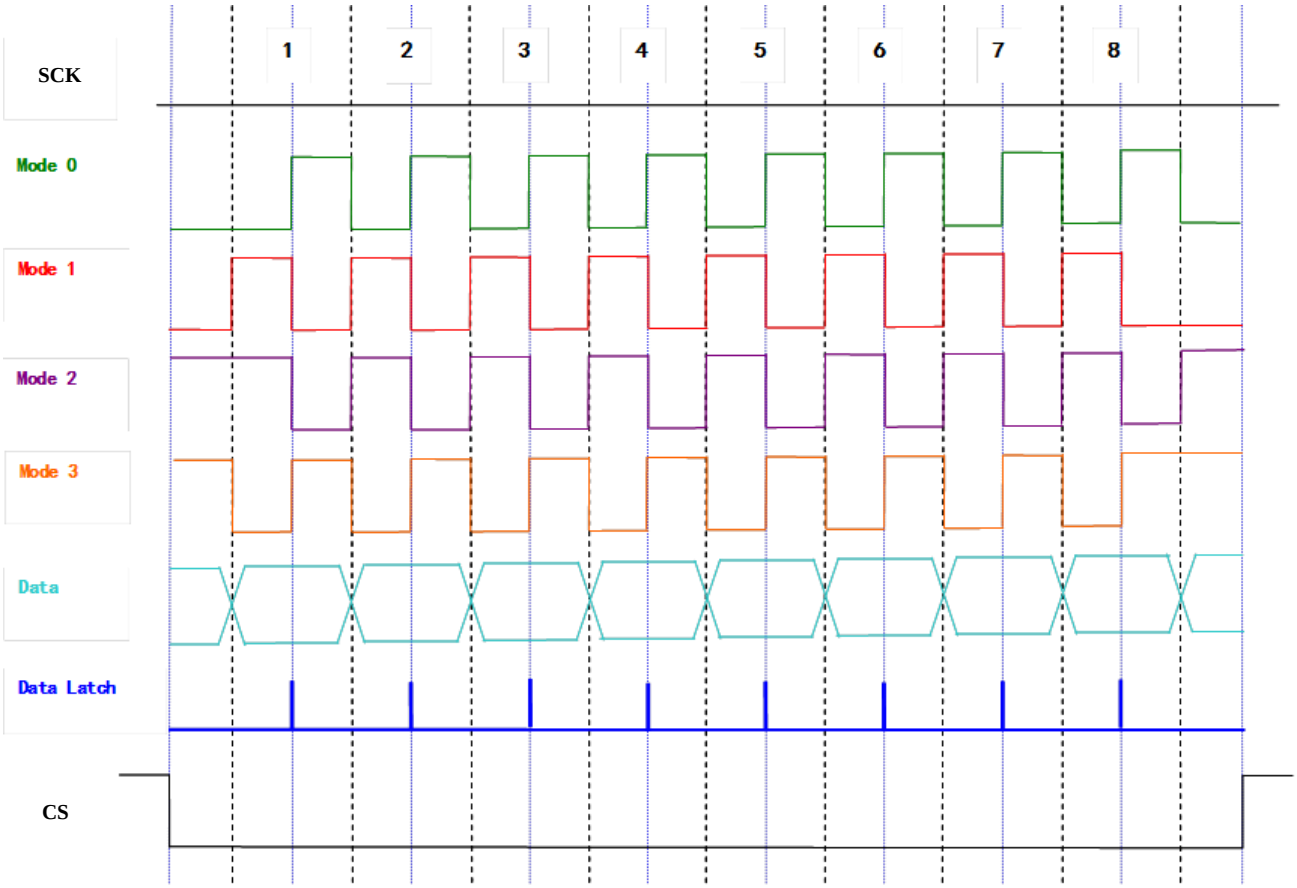
TF[6:0]=56, there are 56-bits (7 bytes) will be transfer.

Note: When SPI is Slave mode, the register has to be set to indicate how many bit data will be received.

7.14.5 SPI Transfer Format

Software selects from four combinations of serial clock (SCK) phase and polarity. The clock polarity is specified by the CPOL control bit which selects an active high or active low clock. The clock phase (CPHA) control bit selects two different transfer formats. The clock phase and polarity should be identical for the master SPI device and the slave device. The following diagrams illustrate SPI transfer format with different CPOL and CPHA in master mode.

	CPOL	CPHA
Mode 0	0	0
Mode 1	0	1
Mode 2	1	0
Mode 3	1	1



7.14.6 SPI Chip Select Control (SPICSC)

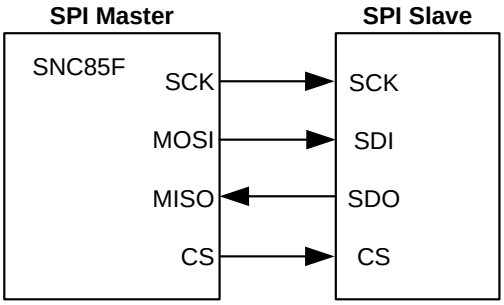
The control of the enable and polarity of chip select pin is done by hardware or software. In hardware controlled CS, the CS polarity is specified by the CSPOL control bit which selects an active high or active low output. In software controlled CS, the SW_CS control bit is used to control one cycle running time of SPI. The chip select (CS) control bit chooses the CS pin is controlled by HW or SW. In slave mode, CS is the chip select pin of the SNC85F it is always active low.

BIT	15	14	13	12	11	10	9	8
	-	SW_CS	-	-	-	-	-	-
R/W	-	R/W	-	-	-	-	-	-
default	-	0	-	-	-	-	-	-
BIT	7	6	5	4	3	2	1	0
	-	-	-	CSPOL	-	-	SLED0	CS
R/W	-	-	-	R/W	-	-	R/W	R/W
default	-	-	-	0	-	-	0	0

Bit	*Name*	*Description*
14	SW_CS	Software control CS 1: CS is high 0: CS is low
4	CSPOL	Chip Select Polarization 1: CS active high 0: CS active low
1	SLED0	0:SLED0 disable 1:SLED0 enable When SLED0 enable, only MOSI pin transfer data, CS/MISO/SCK can be release as GPIO pin.
0	CS	Hardware or Software controls Chip Select Bit 1: HW control CS selected 0: SW control CS selected

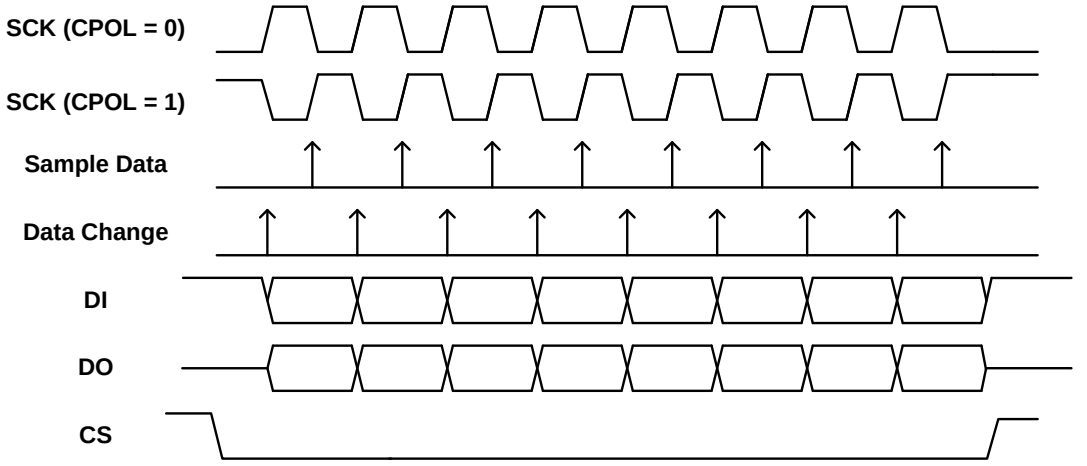
7.15. Serial Peripheral Interface 1 (SPI1,Master mode only)

The SNC85F supports a Serial Peripheral Interface (SPI1). The SPI interface is a synchronous serial data interface that has a relatively simple communication protocol simplifying the programming requirements when communicating with external hardware devices. The interface is often used to communicate with external peripheral devices such as sensors, Flash or EEPROM memory devices etc. The device supports Master mode only which can meet the requirements of a majority of applications. The SNC85F provides standard single I/O mode to elevate accessing external Flash or EEPROM speed. The maximum SPI clock rate is up to 12.288MHz.

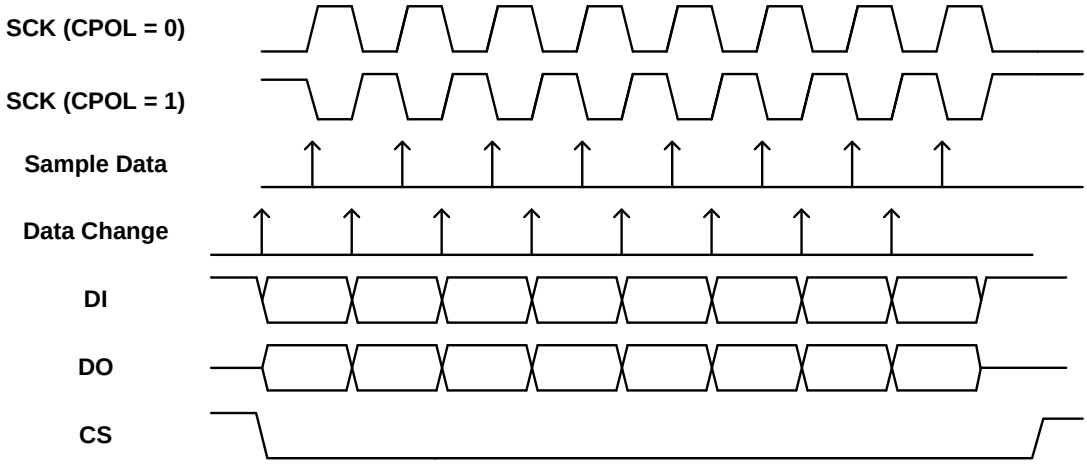


SPI Standard Mode Connection

Software can select any of four combinations of serial clock (SCK) phase and polarity. The clock polarity is specified by the CPOL control bit which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. The following is an SPI transfer format with different CPOL and CPHA values.



CHPA = 1



CHPA = 0

CPOL	CPHA	Function
0	0	Data is read on the clock's rising edge (low->high transition) and data is changed on a falling edge (high->low clock transition).
0	1	Data is read on the clock's falling edge and data is changed on a rising edge
1	0	Data is read on clock's falling edge and data is changed on a rising edge.
1	1	Data is read on clock's rising edge and data is changed on a falling edge.

7.16. I2C

The I2C (Main Serial Port) is a serial communication interface for data exchanging from one MCU to one MCU or other hardware peripherals. These peripheral devices may be serial EEPROM, A/D converters, Display device, etc. The MSP module can operate in one of two modes

- *Full Master Mode*
- *Slave Mode (with general address call)*

The MSP features include the following:

2-wire synchronous data transfer / receiver.

Master (SCL is clock output) or Slave (SC is clock input) operation.

SCL, SDA are programmable open-drain output pin for multiple salve devices application.

Support 400K clock rate.

End-of-Transfer/Receiver interrupt.

7.17. UART

Users can download data from PC through this UART interface. Besides, the UART interface also provides two transmission modes 8-bit and 16-bit.

The UART set-up is shown as bellow.

BIT	15	14	13	12	11	10	9	8
	RxDEnb	RxDStatus		RxDPCE	RxDPCS	RxDPCR	RxDMode	RxD_Reverse
R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W
default	**0**	**00**		**0**	**0**	**0**	**0**	**0**
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
		RxDataRst	TxDataRst	TxDEnb	TxDPCE	TxDPCS	TxDMode	TxD_Reverse
R/W		**C1**	**C1**	R/W	R/W	R/W	R/W	R/W
default		**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit	*Name*	*Description*
15	RxDEnb	RxD enable control 0: disable 1: enable
14:13	RxDStatus	RxD transmission status 00: no data received 01: data received but corrupt 1x: data received ok
12	RxDPCE	Rxd parity check enable 0: disable 1: enable
11	RxDPCS	parity check even/odd select 0: even 1: odd
10	RxDPCR	parity check result 0: error 1: ok
9	RxDMode	8-bit/16-bit mode select 0: 8-bit 1: 16-bit
8	RxD_Reverse	RxD reverse 0: original 1: reverse

7		
6	RxDataRst	Write 1: Reset Rx buffer Write 0: no operation
5	TxDataRst	Write 1: Reset Tx buffer Write 0: no operation
4	TxDEnb	Txd enable control 0: disable 1: enable
3	TxDPCE	parity check enable 0: disable 1: enable
2	TxDPCS	parity check even/odd select 0: even 1: odd
1	TxDMode	8-bit/16-bit mode select 0: 8-bit 1: 16-bit
0	TxD_Reverse	0: original 1: reverse

UART Baud Rate Configure Register(BRCR)

User should select a property baud rate by set baud rate setting register. The detail setting shown as bellow:

BRCR initial value = xxxx xx10 0111 0110

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
---					Divider								Pre-scalar		
---					R/W								R/W		

Baud Rate	Pre-scalar	Divider	Deviation	VALUE in BRCR
1200	111b	80	+0.0%	0x287
2400	110b	80	+0.0%	0x286
4800	101b	80	+0.0%	0x285
9600	100b	80	+0.0%	0x284
19200	011b	80	+0.0%	0x283
38400	010b	80	+0.0%	0x282
51200	001b	120	+0.0%	0x3C1
57600	001b	**107**	+0.6%	0x359
102400	001b	60	+0.0%	0x1E1
115200	001b	53	-1.2%	0x1A9

If the Divider is less than 16, the value will be equal to 16

Note: The default baud rate is 1200.

Pre-scalar=000=> SYS_CLK/1 001 => SYS_CLK /(2) 010=> SYS_CLK /(4)….. 111=> SYS_CLK /(128)

UART timing = **12.288MHz**/(Divider x Divider from pre-scalar)

Example:

BRCR=0x1A9 => pre-scalar=001b Divider=53 => UART Baud rate=12.288MHz/(2x 27)= 115924 Hz

UART Serial Data Output (RxData)

This register is the data buffer of RxD data for UART interface.

RxData initial value = 0000 0000 0000 0000

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RxData															
R/W															

Note: In 8-bit mode, bit8~bit15 will fill in “0”

UART Serial Data In (TxData)

This register is the data buffer of TxD data for UART interface.

TxData initial value = 0000 0000 0000 0000

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
TxData															
R/W															

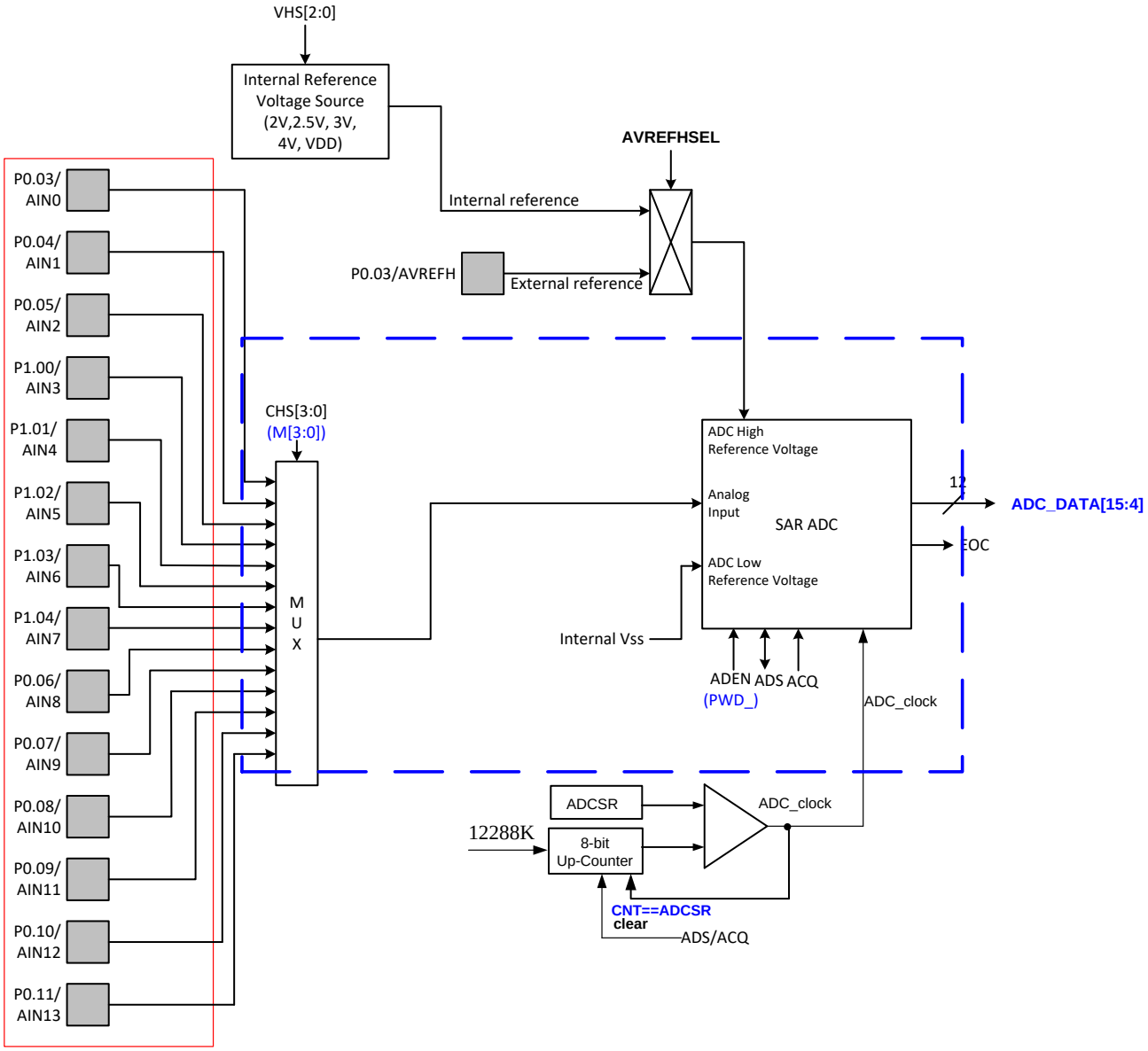
Note: In 8-bit mode, bit8~bit15 will be don’t care.

7.18. Analog to digital converter (ADC)

This analog to digital converter (ADC) has 14 external channels, with 4096-step resolution to transfer analog signal into 12-bits digital data. The sequence of ADC operation is to select input source (AIN0 ~ AIN13) at first, then set CHS and ADS bit to “1” to start conversion. When the conversion is complete, the ADC circuit will set EOC bit to “1” and final value output in ADC Data Register.

Use CHS [3:0] to select AIN pin and ADCEN enables global ADC channel, the analog signal inputs to ADC engine. The ADC reference high voltage includes two source, one is internal voltage (AVREFH_SEL=0), and the other one is external reference voltage input pin from P0.03 pin (AVREFH_SEL=1).

The ADC converting rate can be selected by ADCSR[7:0] bits.



7.18.1 ADC CONVERTING TIME

The ADC converting time is from ADS=1 (Start to ADC convert) to EOC=1 (End of ADC convert). The converting time duration is depended on ADC clock rate.

ADC clock source is controlled by ADCSR [7:0] bits. The ADC converting time affects ADC performance. If input high rate analog signal, it is necessary to select a high ADC converting rate. If the ADC converting time is slower than analog signal variation rate, the ADC result would be error. So to select a correct ADC clock rate and ADC resolution to decide a right ADC converting rate is very important.

ADC_Sample_Rate = 12.288MHz/((ADCSR+1) *16)

ADCSR[7:0]	ADC_clock(KHz)	ADC_SPS(KHz)
5	2048.0	64.00
7	1536.0	48.00
11	1024.0	32.00
15	768.0	24.00
23	512.0	16.00
31	384.0	12.00
47	256.0	8.00
63	192.0	6.00
255	48.0	1.50

7.18.2 ADC CONTROL NOTICE

ADC SIGNAL:

The ADC high reference voltage is internal VDD or external voltage source. The ADC low reference voltage is ground. The ADC input signal voltage range must be from high reference voltage to low reference voltage.

The external high reference voltage from P0.03 must be higher than “Low reference voltage + 2V”. The low reference voltage is ground. So the external high reference voltage range must be between 2V and VDD.

ADC PROGRAM:

The first step of ADC execution is to setup ADC configuration. SNC85F SAR-ADC provides single mode and continuous mode. The ADC program setup sequence and notices are as following.
Single Mode: SAR ADC convert for one time.

- Step 1: Enable ADC. ADCEN is ADC control bit to control. ADCEN = 1 is to enable ADC. ADCEN = 0 is to disable ADC.
- Step 2: If the ADC high reference voltage is from external voltage source, set the AVREFHSEL = 1. The ADC external high reference voltage inputs from P0.03 pin. It is necessary to set P0.03 as input mode without pull-up resistor.
  If the ADC high reference voltage is from internal voltage source. It is necessary to set high reference voltage by VHS [2:0]
- Step 3: Select the ADC input pin by CHS [3:0]. When one AIN pin is selected to be analog signal input pin, it is necessary to setup the pin as input mode and disable the pull-up resistor by program.
- Step 4: Start to execute ADC conversion by setting ADS = 1.
- Step 5: Wait the end of ADC converting through checking EOC = 1. ADS is cleared when the end of ADC converting automatically. EOC bit indicates ADC processing status immediately and is cleared when ADS = 1. Users needn't to clear it by program.

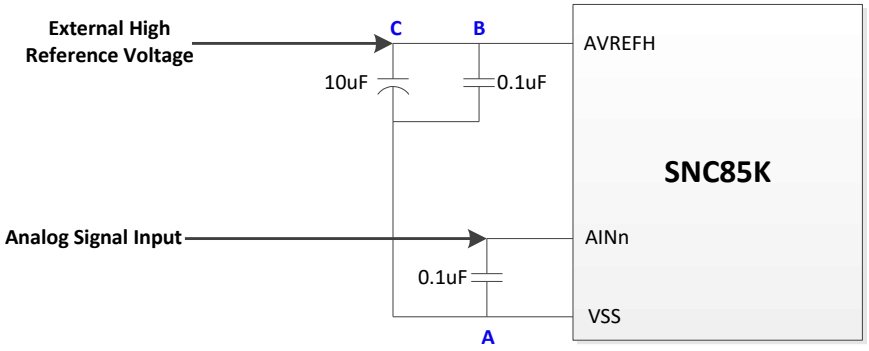
Continuous Mode: SAR ADC Convert continuously. User don't need to restart when ADC is converted done.

- Step 1: Enable ADC. ADCEN is ADC control bit to control. ADCEN = 1 is to enable ADC. ADCEN = 0 is to disable ADC.
- Step 2: If the ADC high reference voltage is from external voltage source, set the AVREFHSEL = 1. The ADC external high reference voltage inputs from P0.03 pin. It is necessary to set P0.03 as input mode without pull-up resistor.
  If the ADC high reference voltage is from internal voltage source. It is necessary to set high reference voltage by VHS [2:0]
- Step 3: Select the ADC input pin by CHS [3:0]. When one AIN pin is selected to be analog signal input pin, it is necessary to setup the pin as input mode and disable the pull-up resistor by program.
- Step 4: Start to execute ADC conversion by setting ACQ = 1.
- Step 5: User needs to set buffer length by ADC_BUF_LEN [3:0]. The converted ADC data will write into destination ram buffer by DMA.
- Step 6: ACQ is cleared when the end of ADC converting automatically. EOC bit indicates ADC processing status immediately and is cleared when ACQ = 1. Users needn't to clear it by program.
  User can also check converted data in ram by ADC_Buf_Index.

ADC PIN CONFIGURATION

ADC input pins are shared by GPIO pins. ADC channel selection is through CHS [3:0] bits in ADCCR0
register. CHS [3:0] value points to the ADC input channel directly, CHS [3:0] =0000b selects AIN0, CHS[3:0]=0001 b selects AIN1, etc. Only one pin of GPIO can be configured as ADC input in the same time.

7.18.3 ADC CIRCUIT



The analog signal is inputted to ADC input pin “AINn”. The ADC input signal must be through a 0.1uF capacitor “A”. The 0.1uF capacitor is set between ADC input pin and VSS pin, and must be on the side of the ADC input pin as possible. If the ADC high reference voltage is from external voltage source, the external high reference is connected to AVREFH pin (P0.03). The external high reference source must be through a 10uF “C” capacitor first, and then 0.1uF capacitor “B”. These capacitors are set between AVREFH pin and VSS pin, and must be on the side of the AVREFH pin as possible.

7.18.4 ADC REGISTERS

ADC CONTROL REGISTER0

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
ADCCR0 (0x43)			AVREFH_SEL	ADCEN	VHS[2:0]			ACQ
R/W			R/W	R/W	R/W			W
default			0	0	0			0
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	EOC	ADS	ADC_DATA_EN		CHS[3:0]			
R/W	R/W	R/W	R/W		R/W			
default	0	0	0		0			

BIT	Description
AVREFH_SEL	ADC high reference voltage source select bit 0: Internal reference voltage (P0.03 as GPIO or AIN0) 1: Enable external reference voltage from P0.03
ADCEN	ADC control bit. 0: Disable 1: Enable

	Note: In sleep mode, disable ADC for reduce power consumption
VHS	ADC internal reference high voltage select bit 000: 2.0V 001: 2.5V 010: 3.0V 011: 4.0V 100: VDD Other: Reserved
ACQ	ADC start to sampling signal, FW needs to set “1” enable at first. HW will automatically control the signal after second time.
EOS	ADC status bit 0: ADC progressing 1: End of conversion(automatically set by hardware; manually cleared by firmware)
ADS	ADC start sample signal for one time. FW need to set “1” to start(automatically cleared in the end of conversion)
ADC_DATA_EN	Control bit of HW fill data into ADC DATA REG from SAR ADC 0: Stop 1: Start
CHS	ADC input channel select 0000: AIN0 / P0.03 0001: AIN1 / P0.04 0010: AIN2 / P0.05 0011: AIN3 / P1.00 0100: AIN4 / P1.01 0101: AIN5 / P1.02 0110: AIN6 / P1.03 0111: AIN7 / P1.04 1000: AIN8 / P0.06 1001: AIN9 / P0.07 1010: AIN10 / P0.08 1011: AIN11 / P0.09 1100: AIN12 / P0.10 1101: AIN13 / P0.11 Other: Reserved

ADC CONTROL REGISTER1

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

ADCCR1 (0x44)	ADCBUF_EN	ADCBUF_LEN[3:0]				Sign Bit		
R/W	R/W	R/W				R/W		
default	0	0				0		
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	ADCSR[7:0]							
R/W	R/W							
default	0							

BIT	Description
ADCBUF_EN	ADC buffer control bit. HW will fill the ADCR_BUF RAM from ADC Data REG 0: Stop 1: Start
ADCBUF_LEN	ADC buffer length, Start address from 0x400. The length if ADC Buffer's ram, the unit is 64(0x40)word, the length is (ADCBUF_LEN+1)*0x40 0000: the Length of ADC Buffer's RAM is 64(0x40) 0001: the Length of ADC Buffer's RAM is 128(0x80) 0010: the Length of ADC Buffer's RAM is 192(0xC0) … 1111: the Length of ADC Buffer's RAM is 1024(0x400)
Sign Bit	ADC Data expression bit 0: ADC data is unsigned. 1: ADC data is signed.
ADCSR	

Bank Num	Address Range	Description	Total Size (word)
4	0x400~0x4FF	ADC RAM/User RAM	256
5	0x500~0x5FF	ADC RAM/User RAM	256
6	0x600~0x6FF	ADC RAM/User RAM	256
7	0x700~0x7FF	ADC RAM/User RAM	256

ADCSR[7:0]	ADC_clock(KHz)	ADC_SPS(KHz)
5	2048.0	64.00
7	1536.0	48.00
11	1024.0	32.00

		15	768.0	24.00	
		23	512.0	16.00	
		31	384.0	12.00	
		47	256.0	8.00	
		63	192.0	6.00	
		255	48.0	1.50	

ADC BUFFER INDEX REGISTER

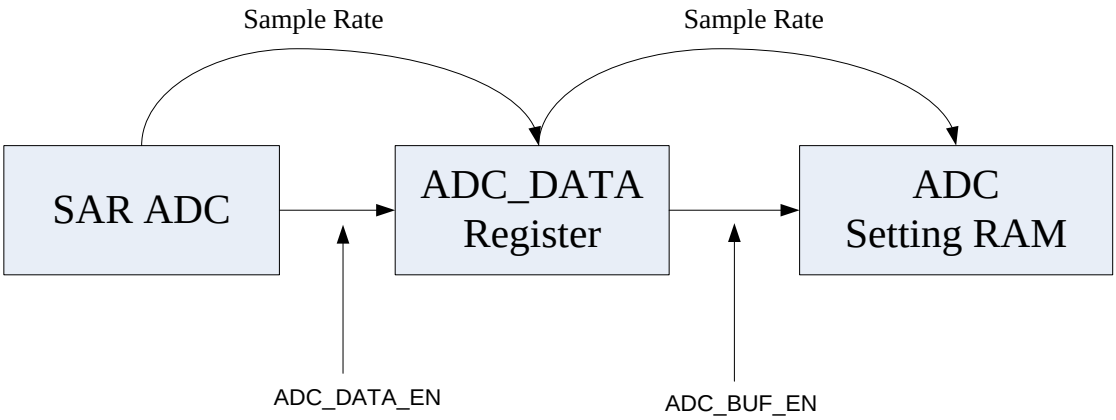
BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
ADC_BUF_INDEX (0x45)	ADC_BUF_Toggle	ADC_Buf_Index[14:0]						
R/W	R/W	R/W						
default	0	0x400						
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	ADC_Buf_Index[14:0]							
R/W	R/W							
default	0x400							

BIT	Description
ADC_BUF_Toggle	If the ADC fill index have over ADC channel buffer length, the bit will toggle and HW reset the ADC BUF index.
ADC_BUF_Index	The ADC fill index from the data register of ADC channel to ADC channel Buffer RAM Range: 0x400~0x7FF

ADC DATA REGISTER

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
ADC_DATA_REG (0x46)	ADC_DATA[15:0]							
R/W	R							
default	0							
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	ADC_DATA[15:0]							
R/W	R							
default	0							

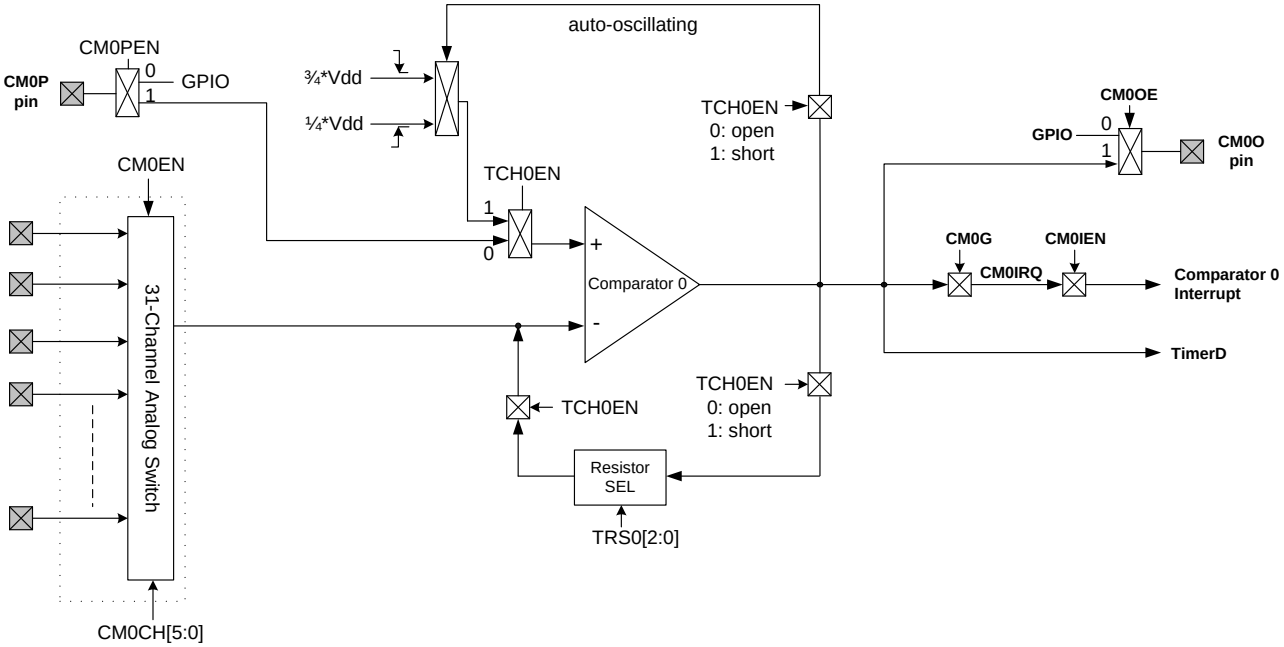
BIT	Description
ADC_DATA_REG	ADC channel Data Register, user can read the register.



7.19. Comparator

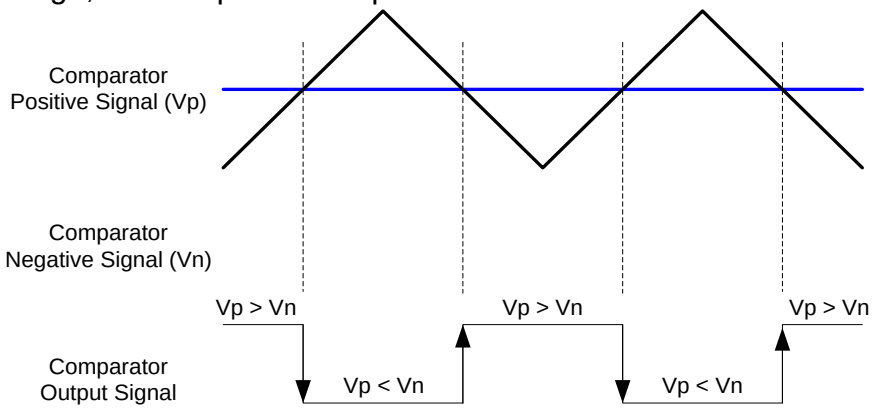
The SNC85F includes an analog comparator function. There are Max. 31-channel negative input pins, auto-oscillating circuit with controllable feedback resistors, as well as programmable interrupt trigger configurations. The comparator circuit operates as a normal comparator or can be configured for Cap-Sensing applications. The main parts of the comparator circuit includes the following:

- 31-channel negative input selection.
- Comparator output function.
- Auto-oscillating control block.
- Cap-Sensing compensation.
- Interrupt function.



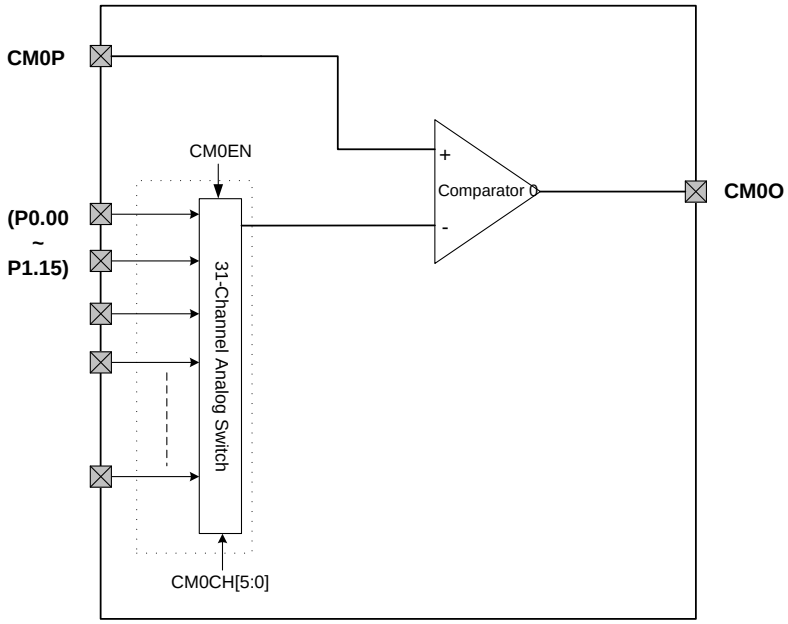
7.19.1 Comparator Operation

The comparator operation is to compare the voltage between comparator positive input and negative input terminals. When the positive input voltage is greater than the negative input voltage, the comparator output is high status. When the positive input voltage is less than the negative input voltage, the comparator output is low status.



7.19.2 Normal Comparator Configuration

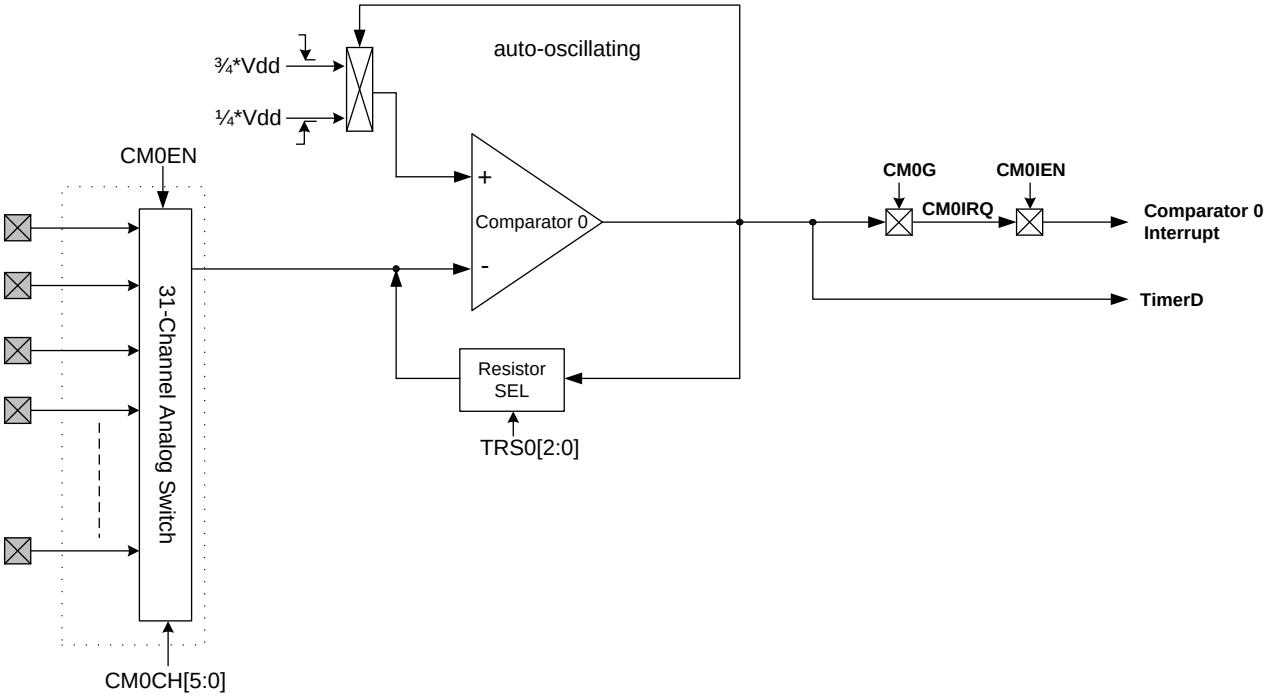
The comparator function through register settings can be used as normal comparator mode. When TCH0EN=0, the comparator will disconnect the internal circuit. When CM0PEN=1 and CM0OE=1, the comparator positive input is connected to GPIO and the comparator output is connected to GPIO. The comparator negative input terminals support up to a maximum of 40 channels controlled by CH0CH[5:0] analog switch selection bits.



TCH0EN=0, Normal Comparator Mode

7.19.3 Cap-Sensing Configuration

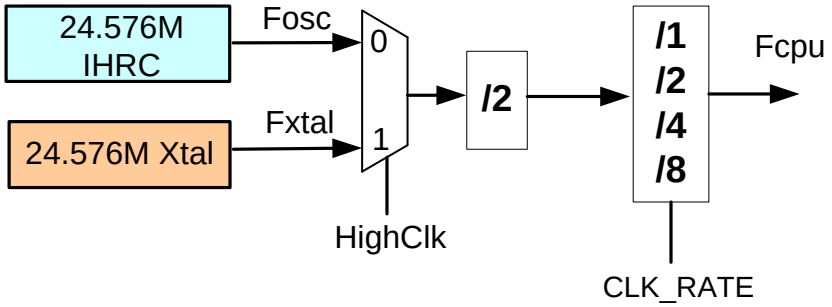
The negative input terminal connects to the external input pin and auto-oscillating output terminal. When TCH0EN=1, the comparator connects to the internal auto-oscillating circuit and the positive input terminal connects to the internal reference voltage source. The comparator negative input terminal supports up to a maximum of 40 channels controlled by CH0CH[5:0] analog switch selection bits. The CM0OUT flag indicates the comparator result is available and immediately accessible while the CM0IRQ only indicates the event of the comparator result.



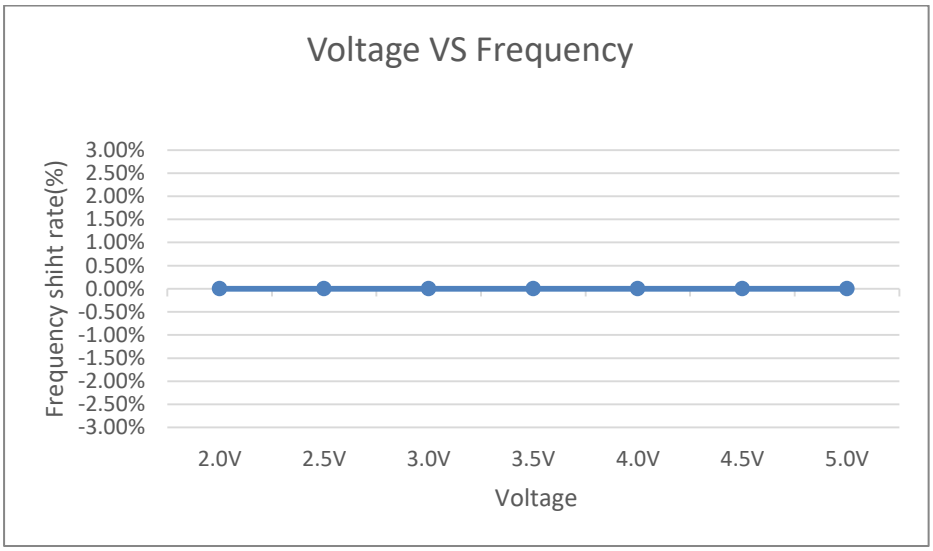
TCH0EN=1, Cap-Sensing Mode

7.20. System Clock

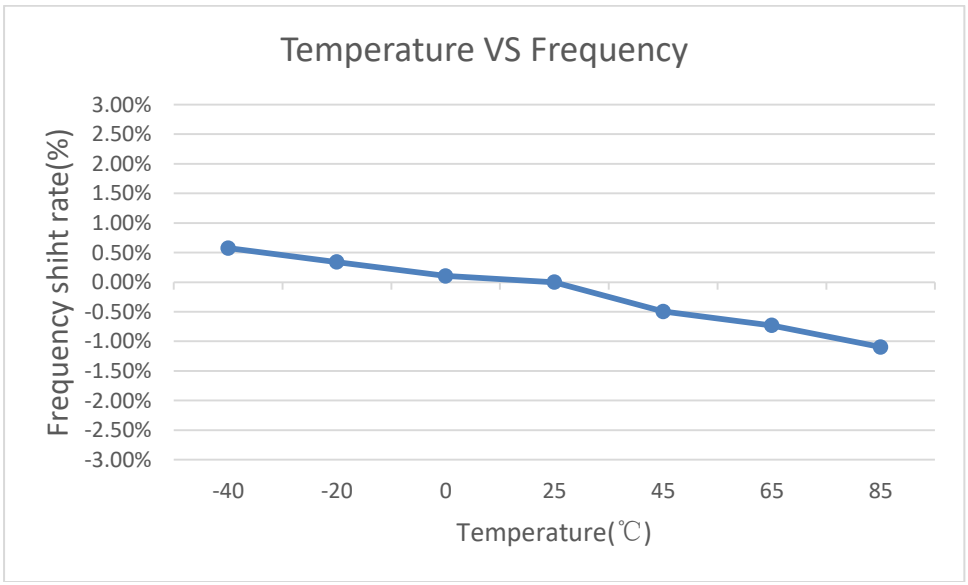
The SNC85F supports selectable internal high-speed RC(IHRC) or external 24.576MHz crystal clock sources.



IHRC frequency is affected by voltage and temperature of the system where the following illustrates the relationship.



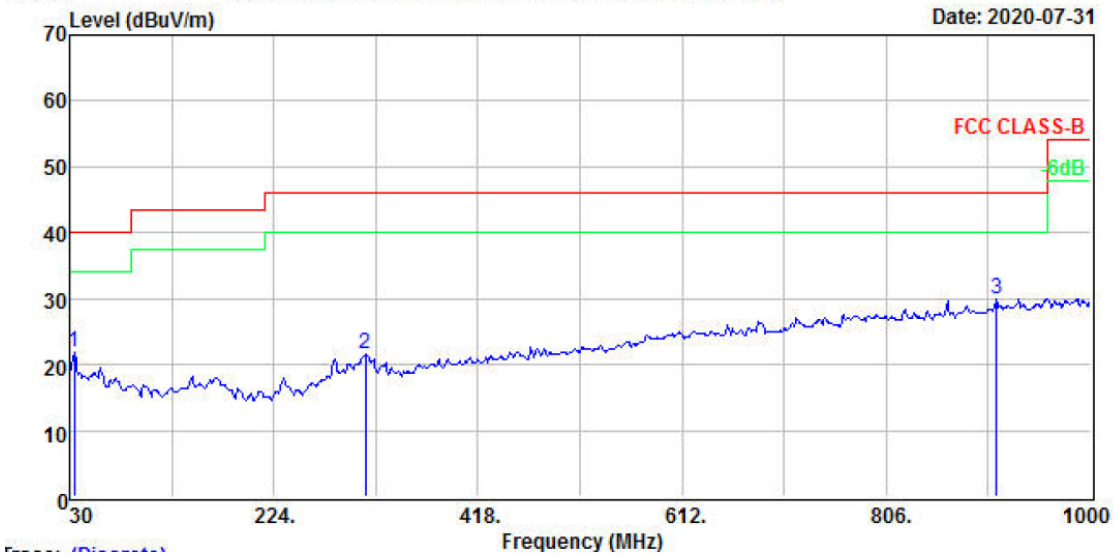
The Figure shows the relationship between high-clock frequency and temperature at VDD=3V



7.21. EMI Test result

SNC85F has built-in EMI enhancement technology that can greatly reduce EMI interference.

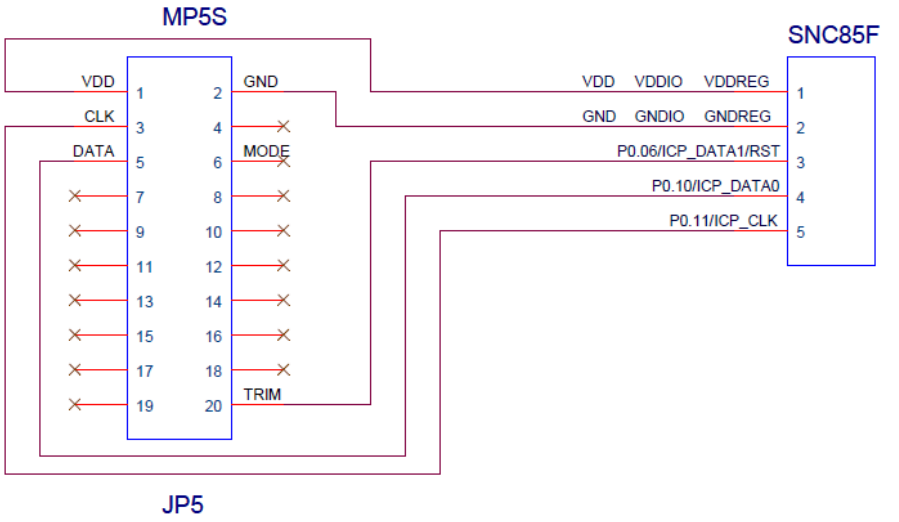
As shown below, the SNC85F has passed FCC testing scan with considerable margin.

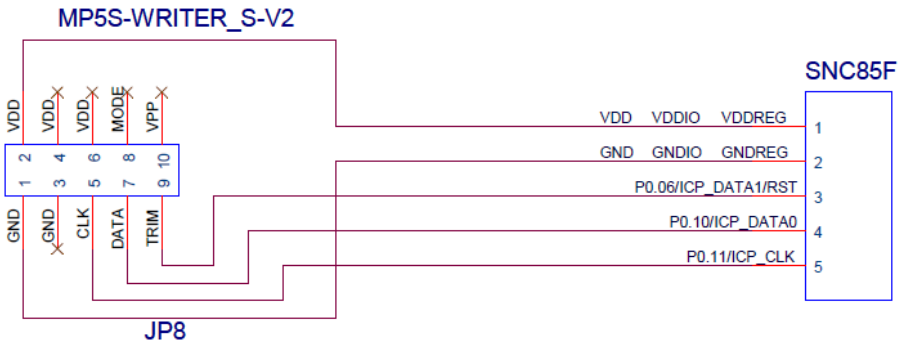


8 APPLICATION CIRCUIT

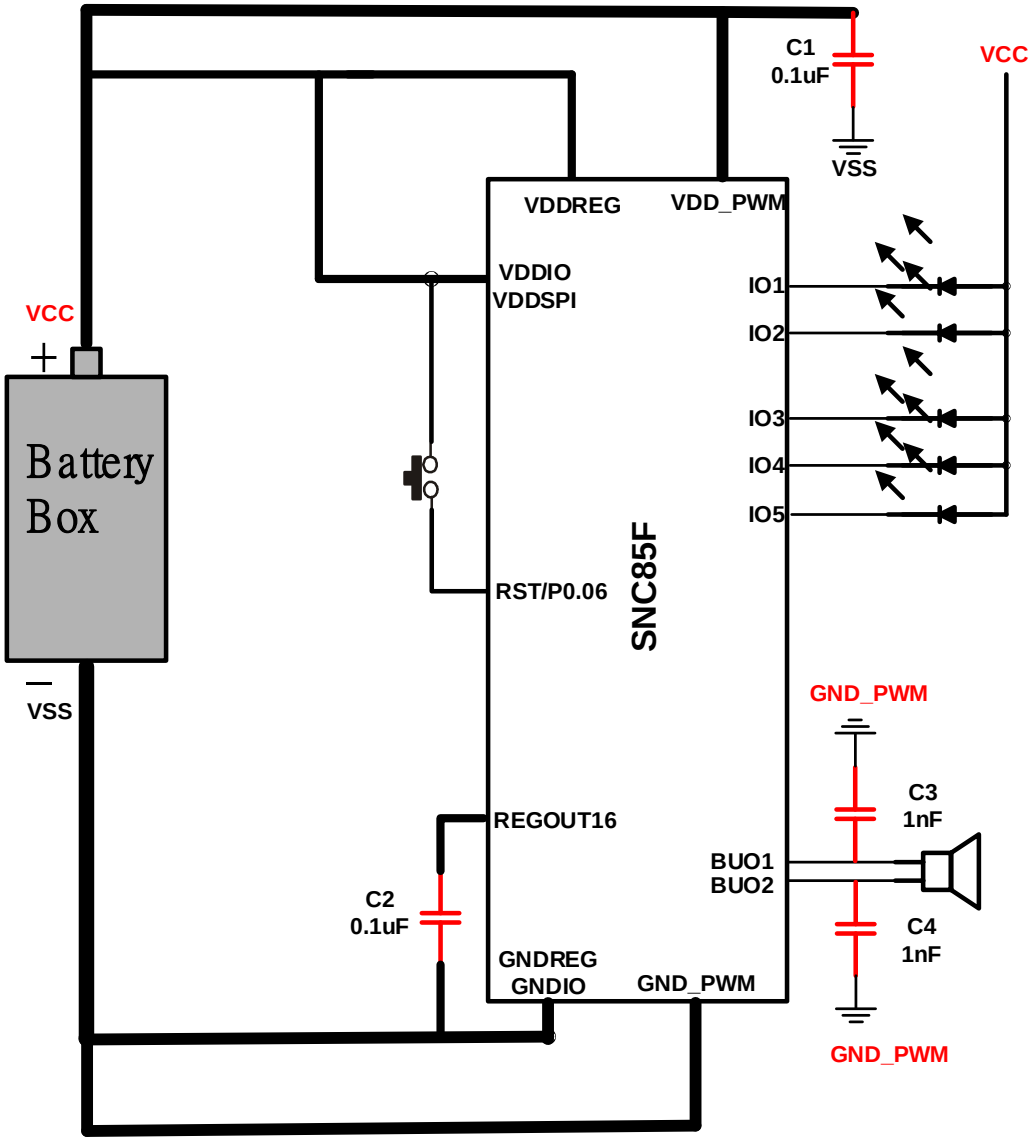
8.1.1 I/F of Programming mode

1. VDD
2. GND
3. ICP_Clock
4. ICP_DATA0
5. ICP_DATA1



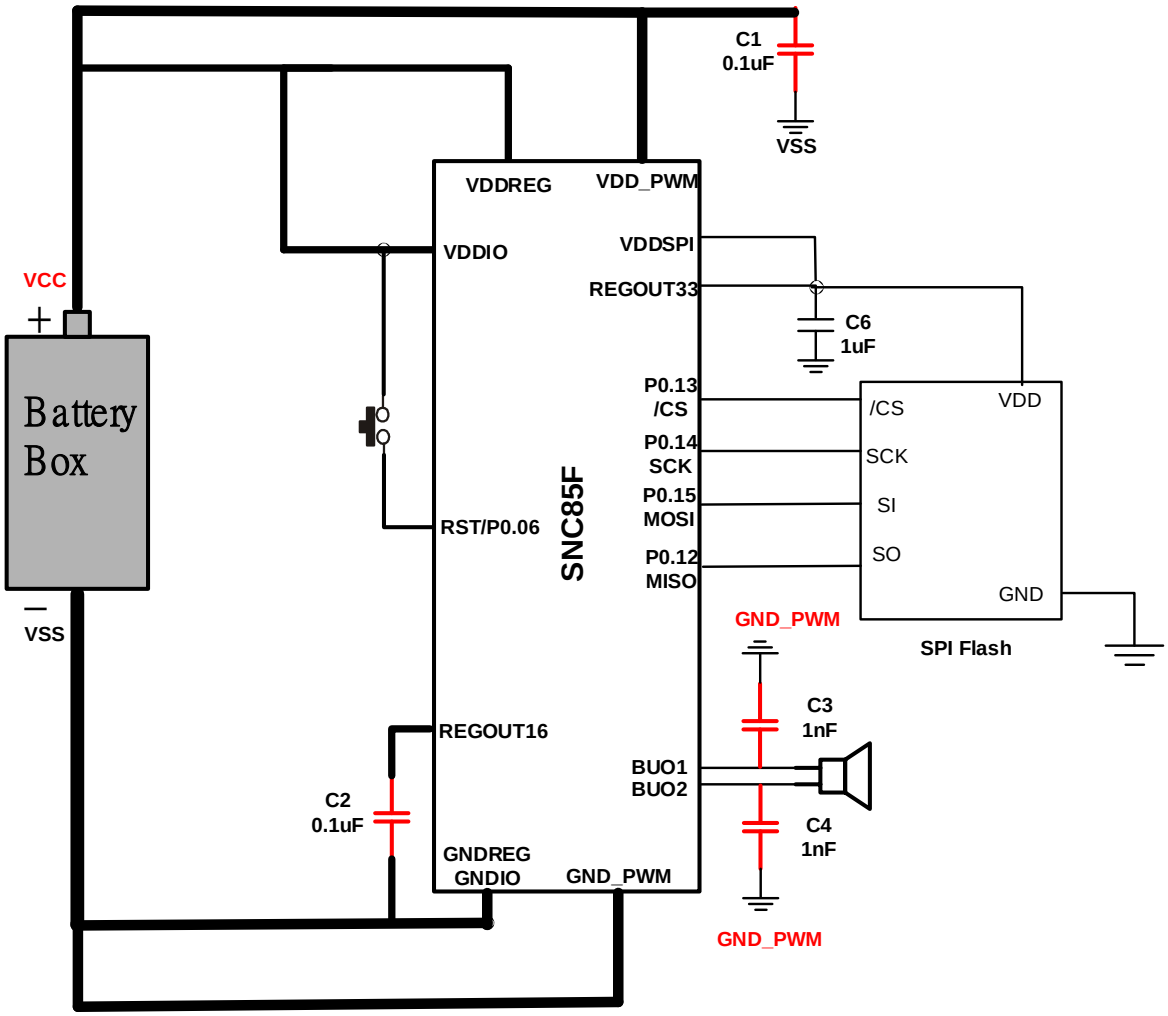


8.1.2 System clock from 24.576M IHRC Source



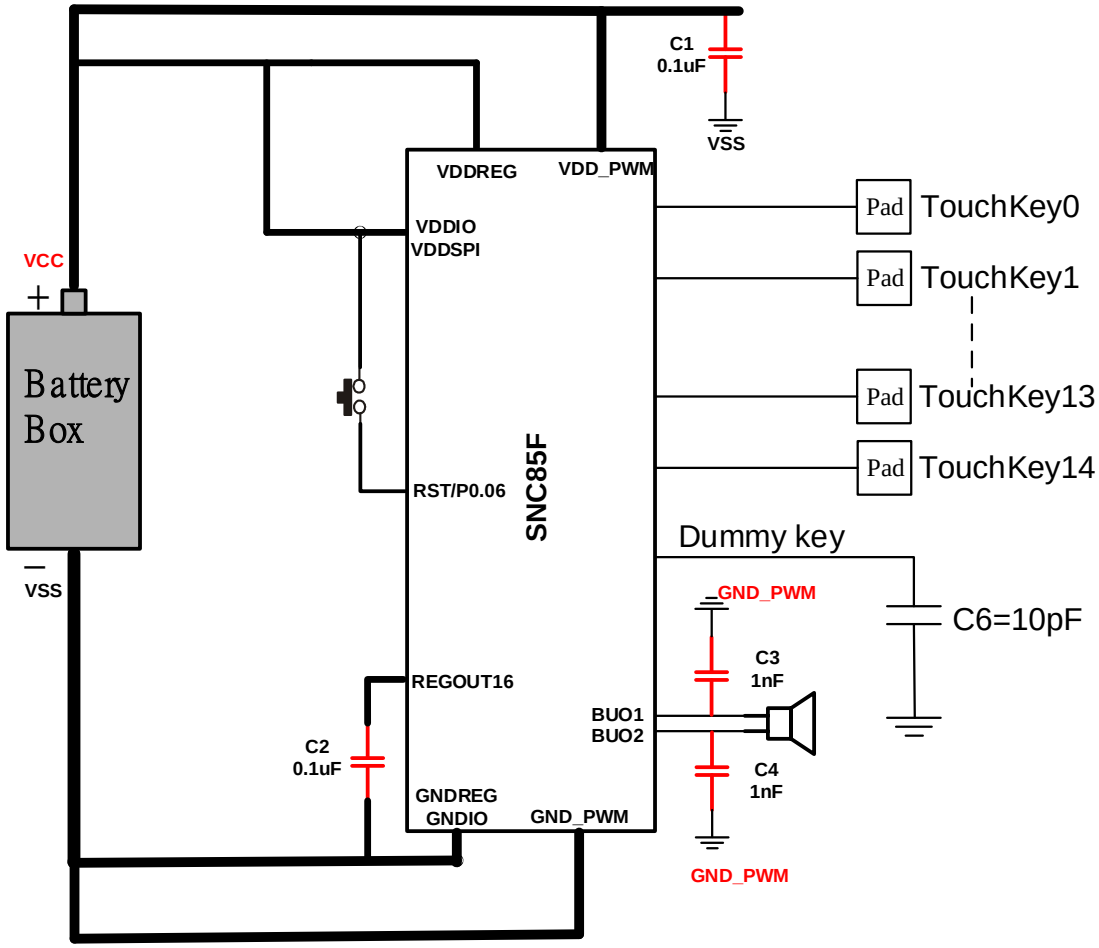
Note1: C1/C2 are necessary component for SNC85F
Note2: C3/C4 are necessary component for system ESD protection.

8.1.3 Application circuit with SPI Flash



Note1: C1/C2 are necessary component for SNC85F
Note2: C3/C4 are necessary component for system ESD protection.

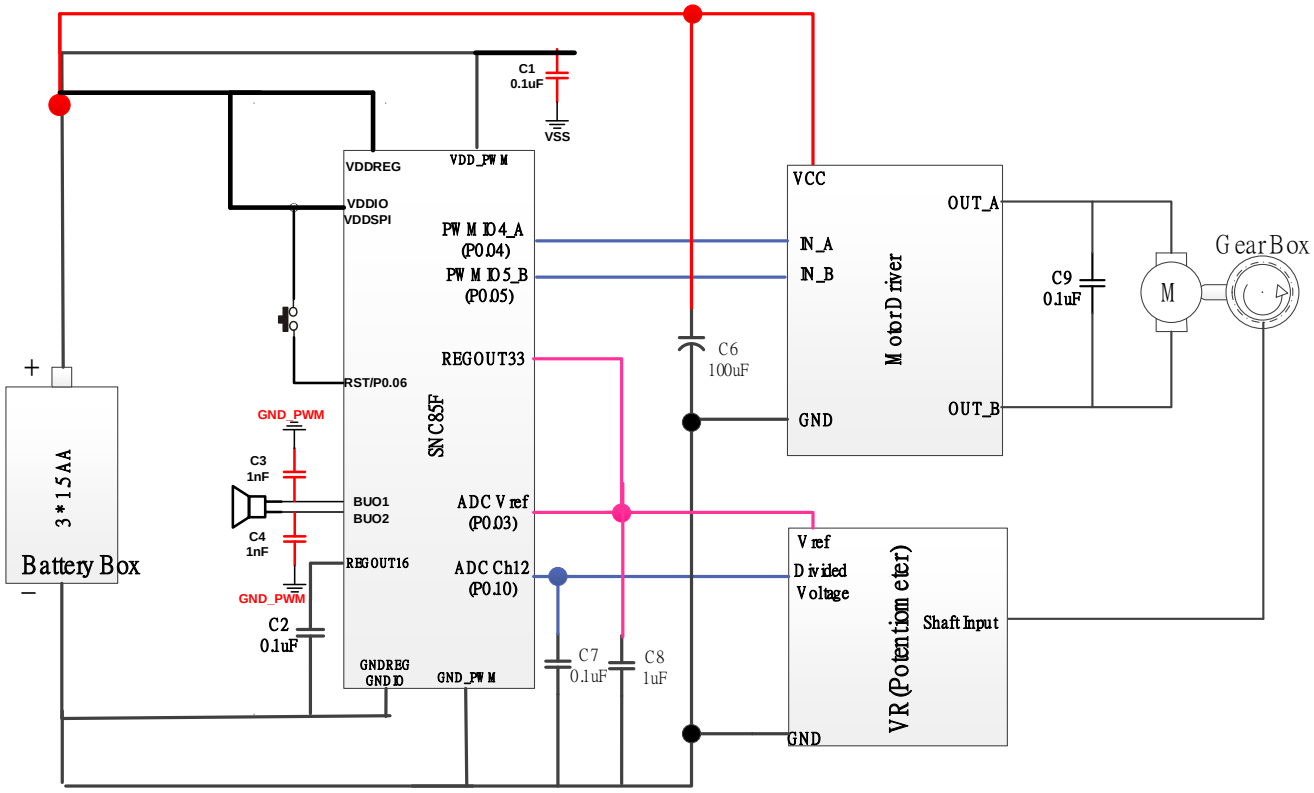
8.1.4 Application circuit with Cap-touch key



Note1: C1/C2 are necessary component for SNC85F
Note2: C3/C4 are necessary component for system ESD protection.

8.1.5 Application circuit with ADC/Motor driver

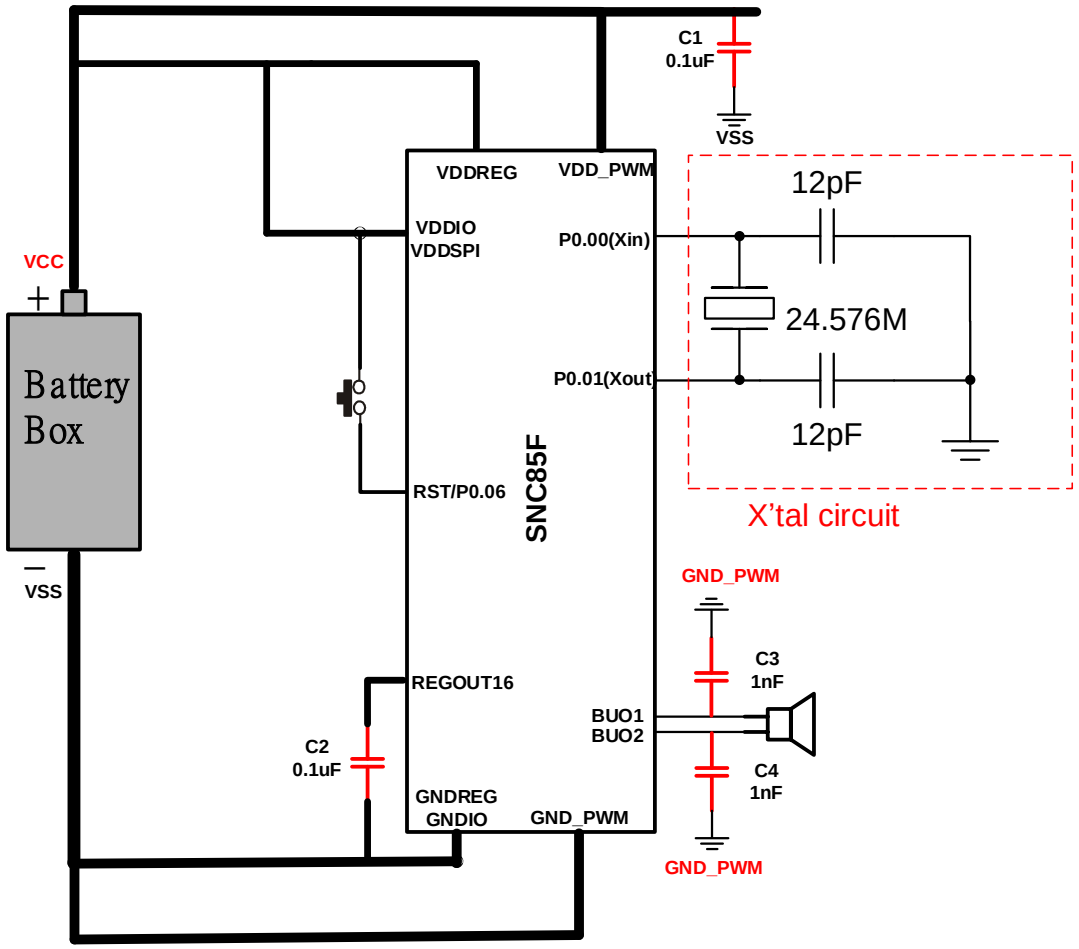
Only for SNC85F320D/SNC85F670D



Note1: C1/C2 are necessary component for SNC85F
Note2: C3/C4 are necessary component for system ESD protection.

8.1.6 System clock from 24.576M Xtal Source

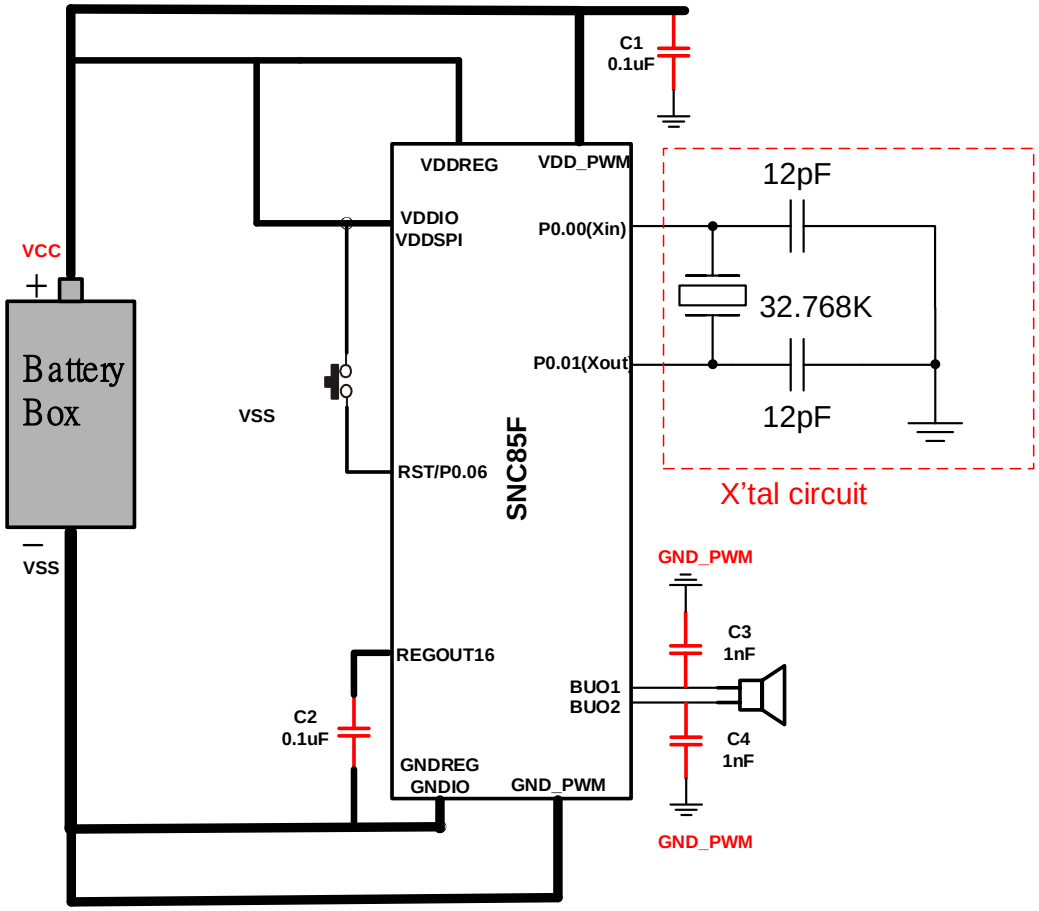
Only for SNC85F500E/SNC85F670E/SNC85F500A/SNC85F670A/SNC85F320D/SNC85F670D



Note1: C1/C2 are necessary component for SNC85F
Note2: C3/C4 are necessary component for system ESD protection.

8.1.7 Low clock from 32.768k Xtal Source

Only for SNC85F500E/SNC85F670E/SNC85F500A/SNC85F670A/SNC85F320D/SNC85F670D

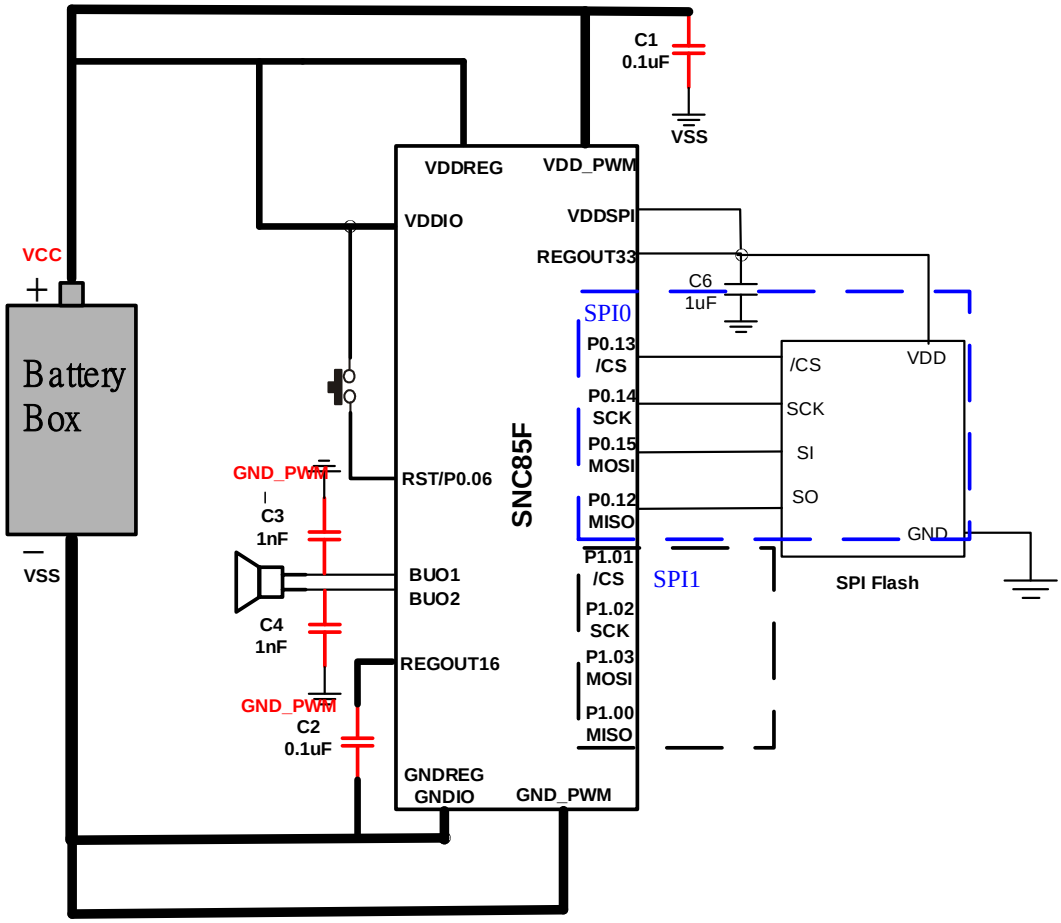


Note1: C1/C2 are necessary component for SNC85F
Note2: C3/C4 are necessary component for system ESD protection.

8.1.8 Application circuit for two SPI interfaces

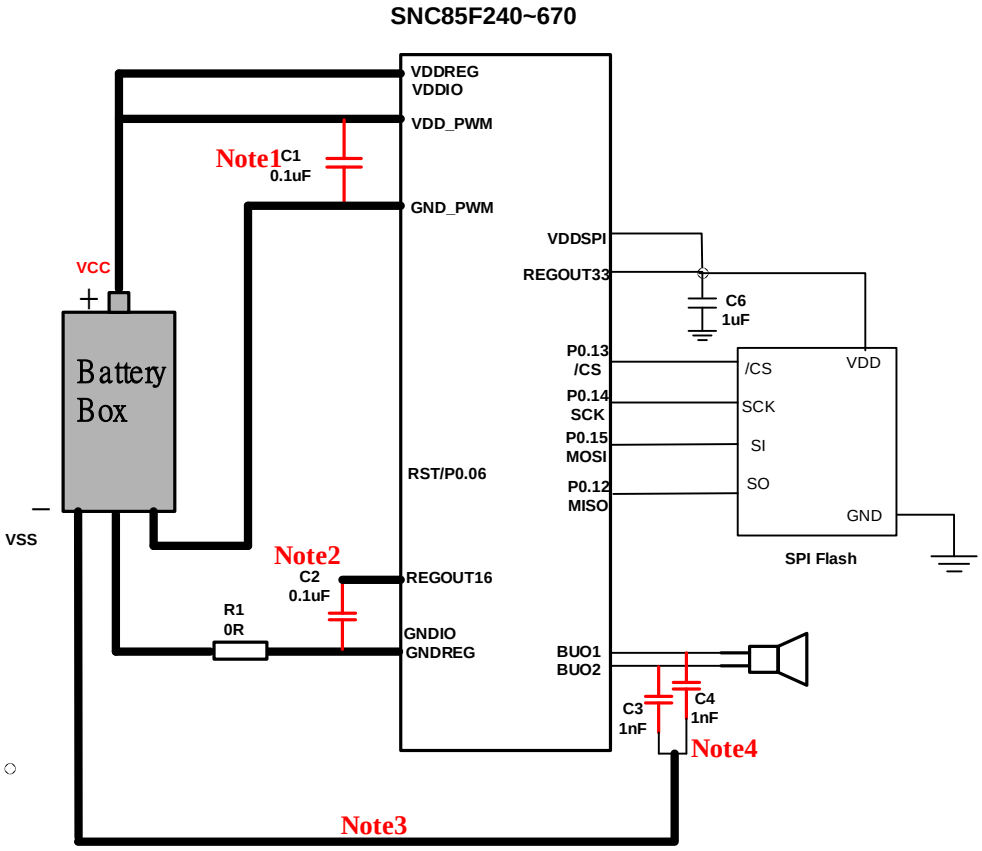
SPI0 is used for SPI flash.

SPI1 is used for SPI communication.



Note1: C1/C2 are necessary component for SNC85F
Note2: C3/C4 are necessary component for system ESD protection.

8.1.9 PCB Layout guide.

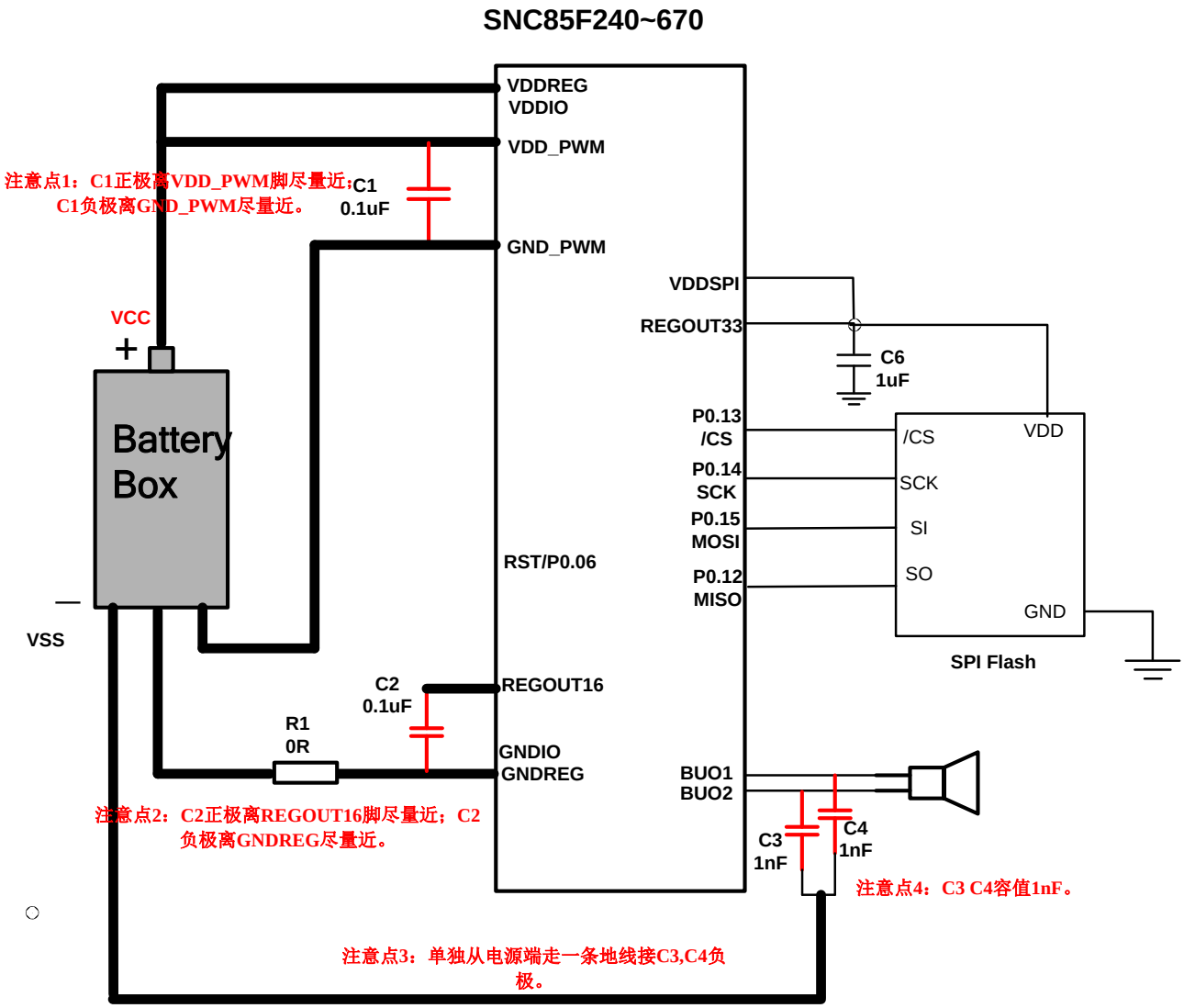


Note1: The capacitor C1 (0.1uF) is suggested as close to the chip as possible, C1+ close to VDD_PWM and C1- close to GND_PWM.

Note2: The capacitor C2 (0.1uF) is suggested as close to the chip as possible, C2+ close to REGOUT16 and C2- close to GNDREG.

Note3&Note4: Use a separate ground wire to connect the capacitor C3(1nF) and C4(1nF).

Chinese version:



9 ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	-0.3	5.5	V
Input Voltage	V_{IN}	V_{SS}-0.2	V_{DD}+0.2	V
Operating Temperature	T_a	-20	85.0	^oC
Storage Temperature	T_{STG}	-40.0	125.0	^oC

10 ELECTRICAL CHARACTERISTICS

DC Characteristics (Ta = 25 ^oC)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	1.8	-	5.5	V	
Standby Current	I_{SBY}	-	10	20	uA	V_{DD}=4.5V,LDO33 off
Operating Current1	I_{OP1}	-	3.0	-	mA	V_{DD}=3V, 12MIPS PWM off, no load. Execute "NOP" instruction
Operating Current2	I_{OP1}	-	2.0	-	mA	V_{DD}=3V, 6MIPS PWM off, no load. Execute "NOP" instruction
IDLE Mode Current1	I_{IDLE1}	-	13	-	uA	V_{DD}=3V, CPU halt, PWM off, 32K x'tal off, ILRC on
Input Pull-low Resistance0	R_{PL0}	-	1.0M	-	Ω	V_{DD}=5V
			1.8M			V_{DD}=3V
Input Pull-low Resistance1	R_{PL1}	-	100K	-	Ω	V_{DD}=5V
			200K			V_{DD}=3V
I/O Drive current	I_{OH2}	-	8	-	mA	V_{DD}=3V, V_O=0.8*VDD
			16			V_{DD}=4.5V, V_O=0.8*VDD
I/O Sink current	I_{OL2}	-	16	-	mA	V_{DD}=3V , V_O=0.13*VDD
			32			V_{DD}=4.5V, V_O=0.13*VDD
SPI I/O Drive current (P1.00~P1.03/P0.12~P0.15)	I_{OH3}	-	12	-	mA	V_{DD}=3V, V_O=0.8*VDD
			21			V_{DD}=4.5V, V_O=0.8*VDD
SPI I/O Sink current (P1.00~P1.03/P0.12~P0.15)	I_{OL3}	-	12	-	mA	V_{DD}=3V , V_O=0.13*VDD
			21			V_{DD}=4.5V, V_O=0.13*VDD
Input Low voltage	V_{IL}	VSS	0.3*VDD	-	V	-
Input high voltage	V_{IH}	-	0.7*VDD	VDD	V	-
Low voltage Reset (LVR)	V_{RST}	1.65	1.70	1.75	V	-
System Clock (ROSC)	F_{SYS}	24.45	24.576	24.70	MHz	± 0.5% @3V
PWM drive current	I_{PPD}		250		mA	V_{DD}=3V, V_O=1.5V

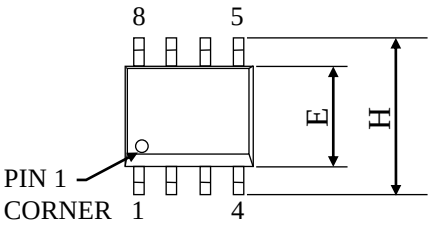
PWM sink current	I_{PPS}		250		mA	V_{DD}=3V, V_O=1.5V

Regulator Characteristics (Ta=25 ^oC)

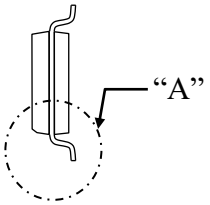
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Voltage	V_{REGI}	2.2	4.5	5.5	V	
Output Voltage	V_{REGO}	3.2	3.3	3.4	V	Input Voltage = 4.5V
Maximum Current Output	I_{REGO}		60		mA	VDD=3.6V LDO output 3.3V drop to 2.7V

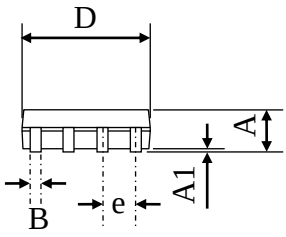
11 PACKAGE INFORAMTION

11.1. 8-pin SOP (150mil)

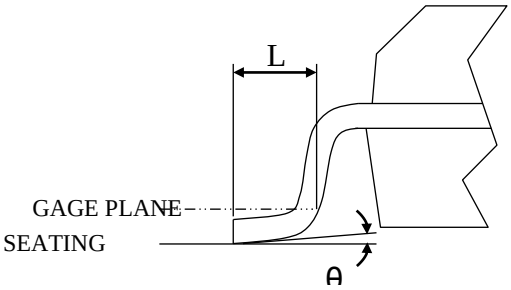


TOP VIEW





SIDE VIEW



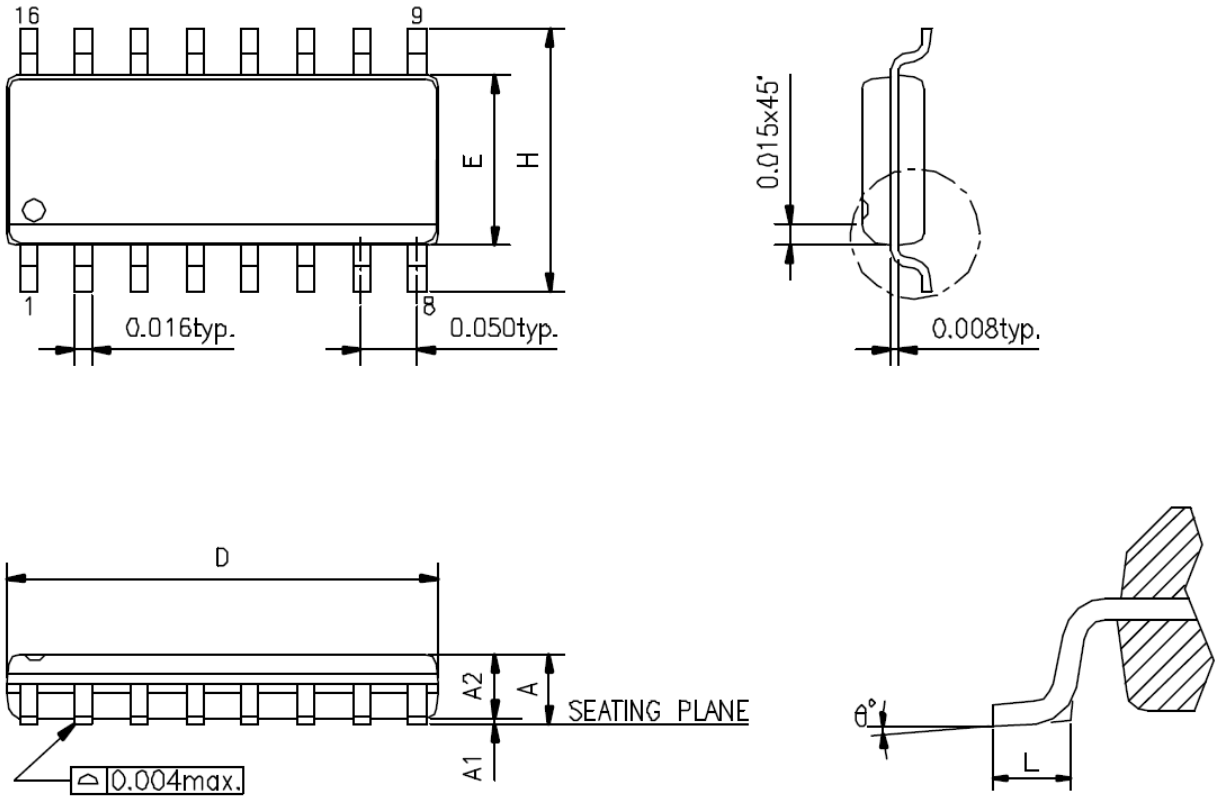
DETAIL "A"

SYMBOLS	Dimension in mm			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	--	--	1.75	--	--	0.069
A1	0.10	--	0.25	0.004	--	0.010
B	0.31	--	0.51	0.012	--	0.020
D	4.90 BSC			0.193 BSC		
E	3.90 BSC			0.153 BSC		
e	1.27 BSC			0.050 BSC		
H	6.00 BSC			0.236 BSC		
L	0.40	--	1.27	0.016	--	0.050
θ	0°	--	8°	0°	--	8°

Notes：

1. CONTROLLING DIMENSION：mm
2. JEDEC OUTLINE : MS-012 AA

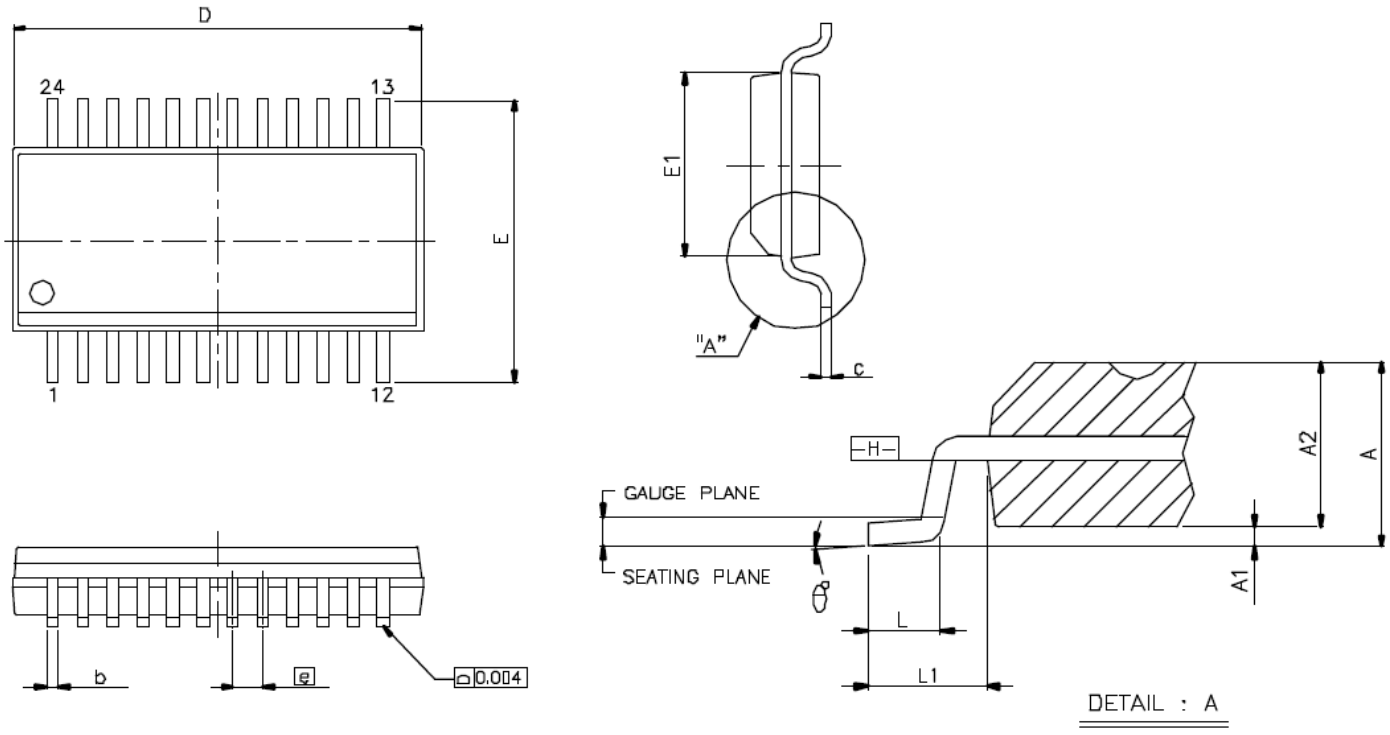
11.2. 16-pin SOP (150mil)



Symbols	Min.	Max.
A	0.053	0.069
A1	0.004	0.010
A2	0.049	0.065
D	0.386	0.394
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT: INCH

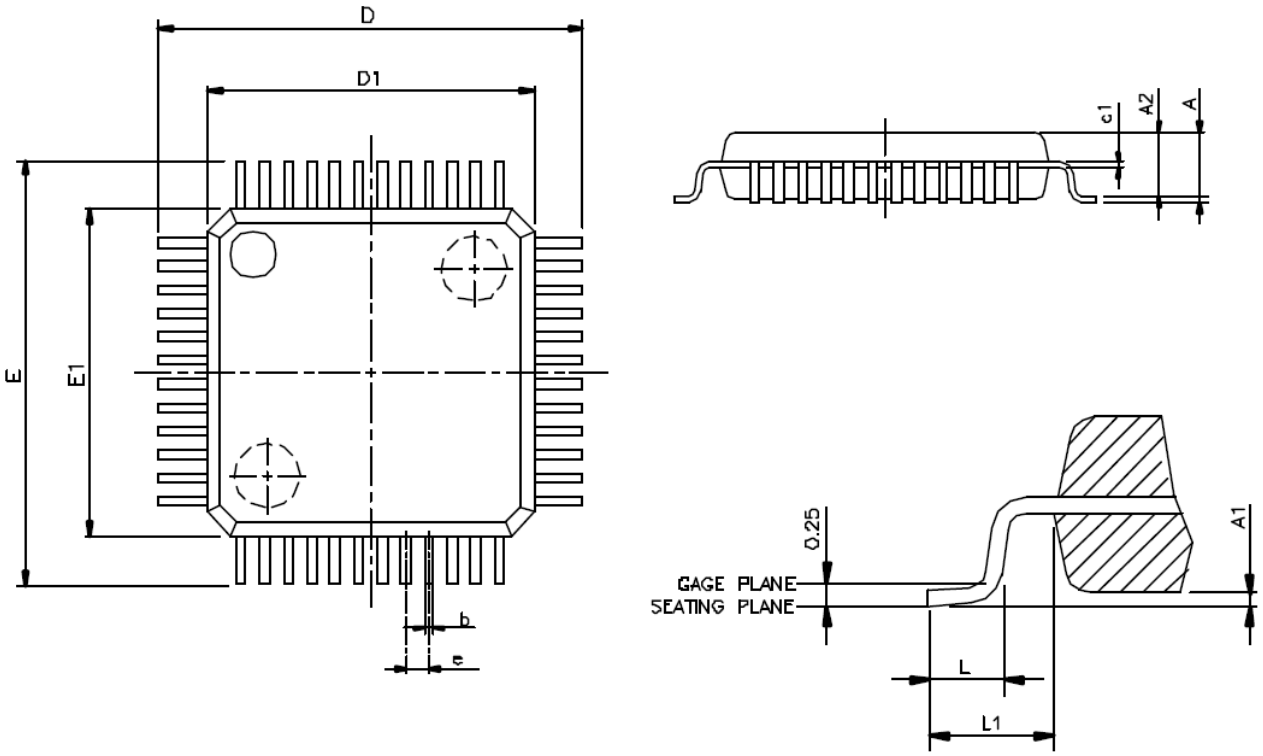
11.3. 24-pin SSOP (150mil)



Symbols	Min.	Max.	Max.
A	0.053	0.064	0.069
A1	0.004	0.006	0.010
A2	-	-	0.059
D	0.337	0.341	0.344
E	0.228	0.236	0.244
E1	0.150	0.154	0.157
b	0.008	-	0.012
c	0.007	-	0.010
e	0.025 BASIC		
L	0.016	0.025	0.050
L1	0.041 BASIC		
θ°	0	-	8

UNIT: INCH

11.4. 48-pin LQFP (7x7x1.4mm)



Symbols	Min.	Max.
A	-	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

UNIT: MM

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