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AMENDMENT HISTORY

Version	Date	Description
Ver 1.0	August 21, 2009	First issue
Ver 1.1	December 10, 2010	Modify ELECTRICAL CHARACTERISTICS



1 INTRODUCTION

SNL200_MTP is the MTP chip with one 32M bit flash memory. It is for emulating the SNL241, SNL261 and SNL281 real chip. It is also an 8-bit LCD controller embedded 2304 dots with 4-grays LCD driver. It contains an 8-bit CPU core, Picture Processing Unit (PPU), Sound Processing Unit (SPU) and other primary functions for LCD games, Education Learning Aids (ELA).

The PPU can process all the graphic data and control the picture display of the system. The SPU is a 16-channel wave table music synthesizer compatible with standard MIDI stream format. It's low power consumption makes it ideal for all battery operated handheld

2 FEATURES

2.1. CPU

- ◆ Single Power Supply 2.4V – 5.1V
- ◆ System clock : 16MHZ Int. Rosc (32768HZ X'tal for slow mode)
- ◆ Dedicated 24 I/O pins
- ◆ Built-in an 8x8 multiplier
- ◆ RAM: 2496 Bytes * 8 bits (including LCD display RAM)
- ◆ Flash memory: 2M X 16 bits(can support SNL241 / SNL261 / SNL281)
- ◆ 4 Operating modes: Normal, Slow, Idle and Halt.
- ◆ Universal Asynchronous Receiver/Transmitter (UART), 1200 bps to 115.2kbps
- ◆ Serial Peripheral Interface (SPI) is provided
- ◆ SONiX SNAD01 ADC Interface.
- ◆ H/W 16x8 Matrix key scan Interface (Occupy 8 I/O and share with 16 COM signal)
- ◆ 4 H/W PWM I/Os with 256 levels duty control
- ◆ IR function is provided
- ◆ 16 CH Voice/MIDI synthesizer, compatible with General MIDI stream format
- ◆ Mark Event Supported in both Wave and Melody.
- ◆ Individual adaptive playing speed from 4k - 64kHz for all 16 voice channels.
- ◆ 10 Bit Direct Drive push pull type current DAC.
- ◆ Low Voltage Reset(LVR) is provided
 - Reset at 2.4V
- ◆ Voltage Detect (LVD) is provided(2.4/2.6/2.8V)

2.2. LCD/PPU

- ◆ LCD resolution: 32x64 or 32x72 (programmable), 1/32 duty, 1/6 bias
- ◆ Built-in Voltage booster and voltage regulator
- ◆ 32 levels Brightness Adjustment
- ◆ Support four grays color
- ◆ Object oriented design support 3 depth layers for all graphic objects.
- ◆ Graphic object support diverse size
- ◆ Support H/W scrolling function



3 FUNCTION DESCRIPTION

SNL200MTP is use to emulate SNL261/281 for function verification during design stage, so all the functions are almost the same as SNL261/281 except memory parts. User can direct to reference SNL261/281 specifications for detail information.

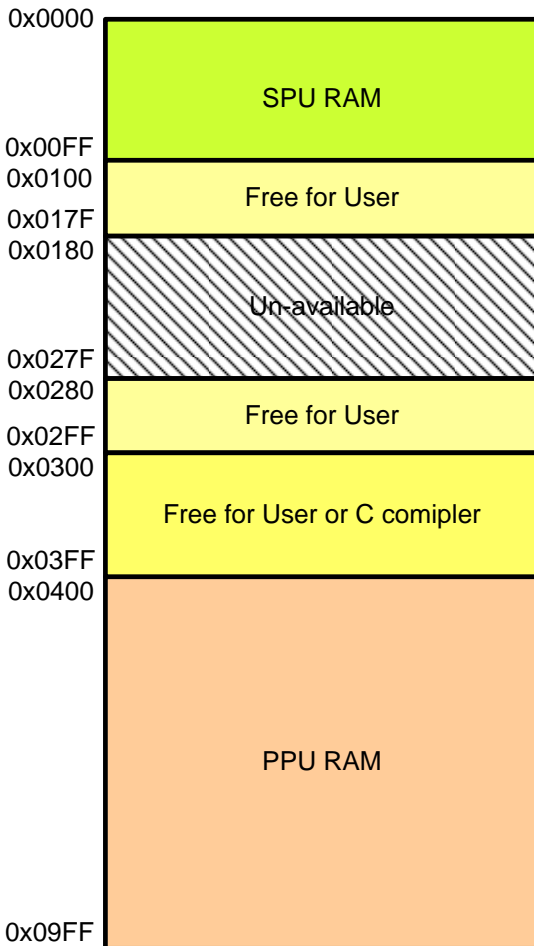
3.1. Flash memory

SNL200MTP contains a 2M x16 bits flash memory which is shared by program and resource data. Program, voice, melodies, data, images and instrument waveforms are shared within this same flash memory area.

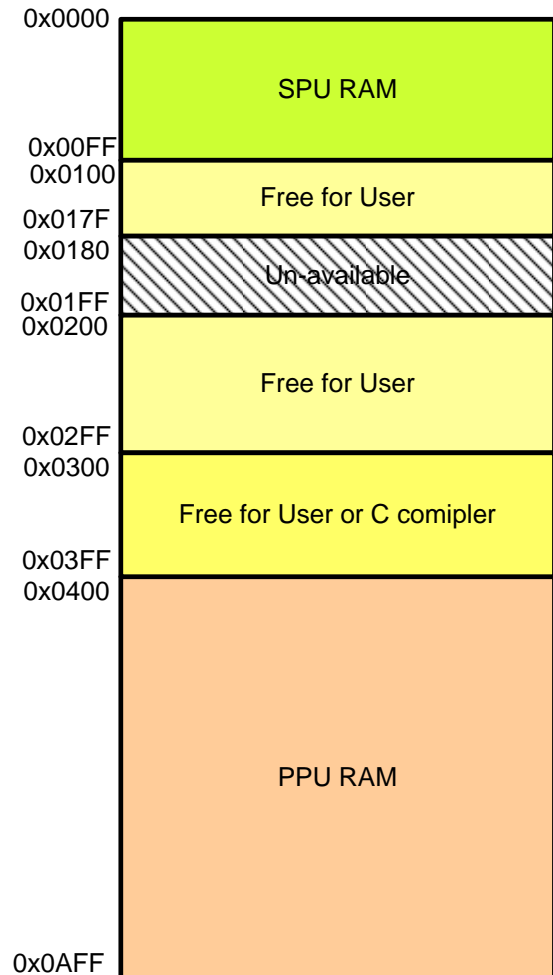
User can use SONiX flash writer to erase and program the flash memory.

3.2. RAM

MTP Chip configure to SNL261



MTP Chip configure to SNL281





4 PIN ASSIGNMENT

Pin NO	Symbol	I/O	Function Description
1~7	NC		Not connect
8	VDDCLK	P	Positive power for low clock
9	XOUTL	O	Low clock crystal output
10	XINL	I	Low clock crystal input
11~12	NC		Not connect
13	VSSCLK	P	Negative power for low clock
14	PWRON_LED	O	To indicate chip is in Power on stage
15	HCLK_Sel	I	High clock select, user should connect to VDD
16~18	NC		Not connect
19	GND	P	Negative power supply
20	VDD	P	Positive power supply for IO
21~28	P57~P50	I/O	Bit7~Bit0 of IO Port 5
29	GND	P	Negative power supply
30	CVDD	P	Positive power supply for CPU Core
31	RegOut	P	3V regulator output
32	VDD	P	Positive power supply for IO
33~40	P67~P60	I/O	Bit7~Bit0 of IO Port 6
41	GND	P	Negative power supply
42	VDD	P	Positive power supply for IO
43~50	P07~P00	I/O	Bit7~Bit0 of IO Port 0
51	GND	P	Negative power supply
52,56	VSSPP	P	Negative power supply for Audio
53,55	BN0, BP0	O	Push pull Audio output.
54	VDDPP	P	Positive power supply for Audio
57~67	NC		Not connect
68	F_A0	I	Address 0 input
69	F_CS_	I	Chip select input
70	A0	O	Address 0 Output
71	CS_	O	Chip select Output
72~73	GND	P	Negative power supply
74~77	NC		Not connect
78	VDD	P	Positive power supply for IO
79	CVDD	P	Positive power supply for CPU Core
80	GND	P	Negative power supply
81~85	NC		Not connect

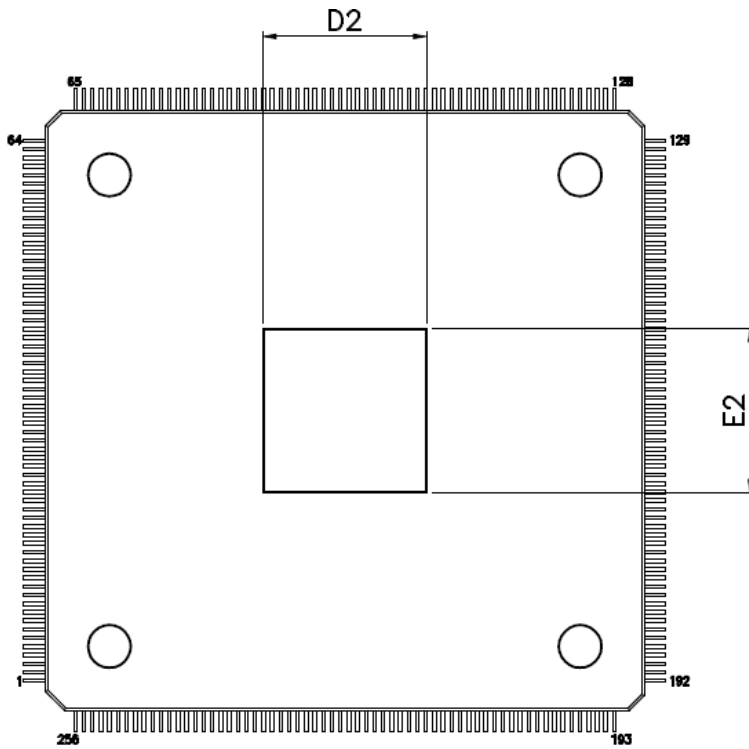
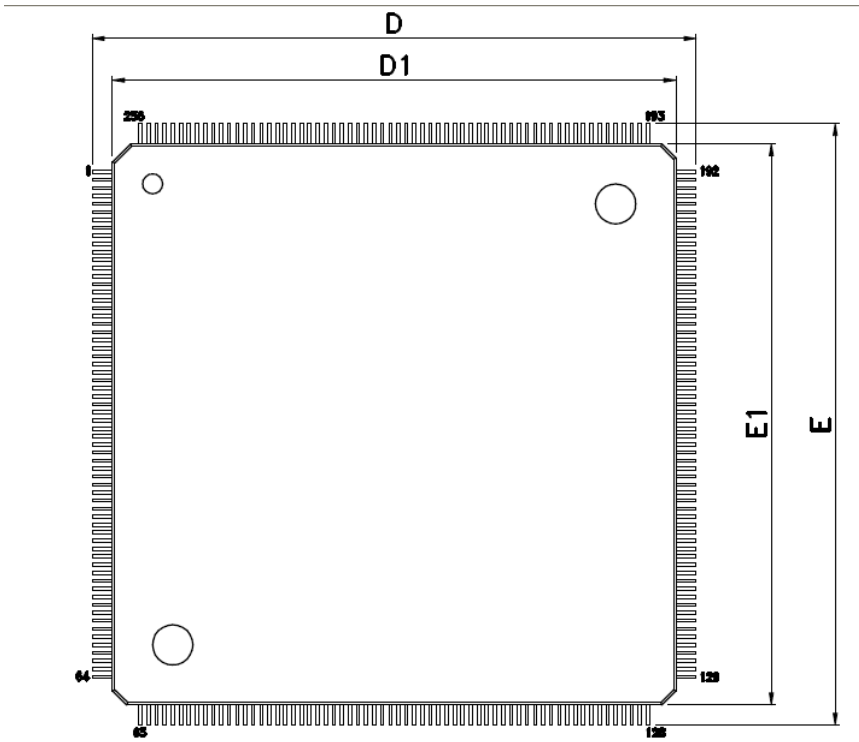


SNL200MTP
(with 2Mx16 Flash Memory)

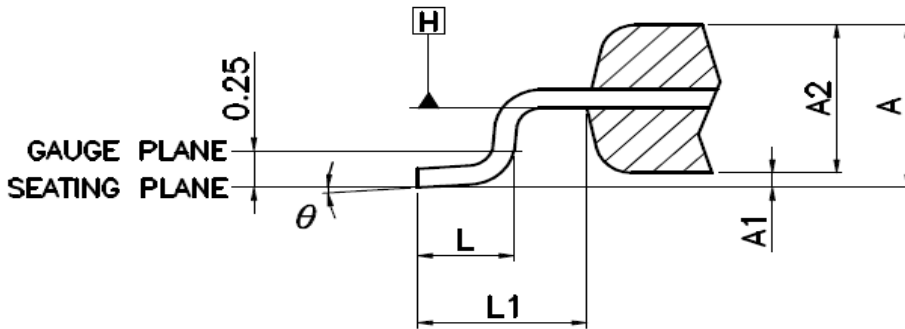
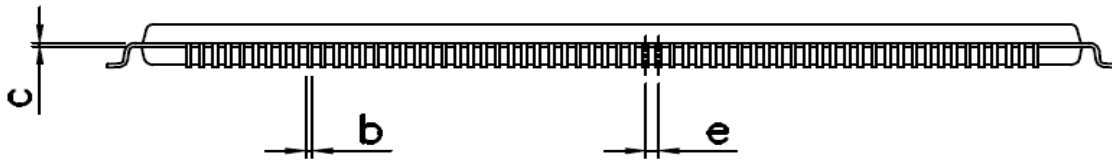
86,87	VDD	P	Positive power supply for IO
88~95	NC		Not connect
96,97	GND	P	Negative power supply
98	VDD		Positive power supply for IO
99	NC		Not connect
100	VDDCP	P	Positive power supply for Charge pump
101	VSSCP	P	Negative power supply for Charge pump
102~103	C1N,C1P	P	Charge pump cap
104~105	C2N,C2P	P	Charge pump cap
106	CPOUT	P	Charge pump output
107	VLCD	P	LCD voltage generation
108~111	V4~V1	P	LCD voltage generation
112~126	COM0~14	O	LCD COM0~COM14 output
127~129	NC		Not connect
130~146	COM15~31	O	LCD COM15~COM31 output
147~191	SEG0~44	O	LCD SEG0~SEG44 output
192~193	NC		Not connect
194~212	SEG45~63	O	LCD SEG45~SEG63 output
213~220	SEG64~71	O	LCD SEG64~SEG71 output (Note)
221~231	NC		Not connect
232~233	VDD	P	Positive power supply for IO
234	RST_	I	Chip Reset (Active low)
235	GND	P	Negative power supply
236	ICECLK	I	ICE clock input
237	GND	P	Negative power supply
238	SCK	I	SPI ICE clock input
239	ICEEN	I	ICE enable pin
240	ICEDI	I	SPI ICE data input
241	ICEDO	P	SPI ICE data output
242	CSB	I	SPI ICE chip enable
243	CVDD	P	Positive power supply for CPU Core
244~252	NC		Not connect
253	GND	P	Negative power supply
254	VDD	P	Positive power supply for IO
255~256	NC		Not connect

Note : If user would like use SNL200MTP chip to emulate the SNL261, the pin NO. 213~221 can be treated as NC pin.

5 LQFP-256 Outline



(THERMALLY ENHANCED VARIATIONS ONLY)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.00	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	30.00 BSC		
D1	28.00 BSC		
E	30.00 BSC		
E1	28.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

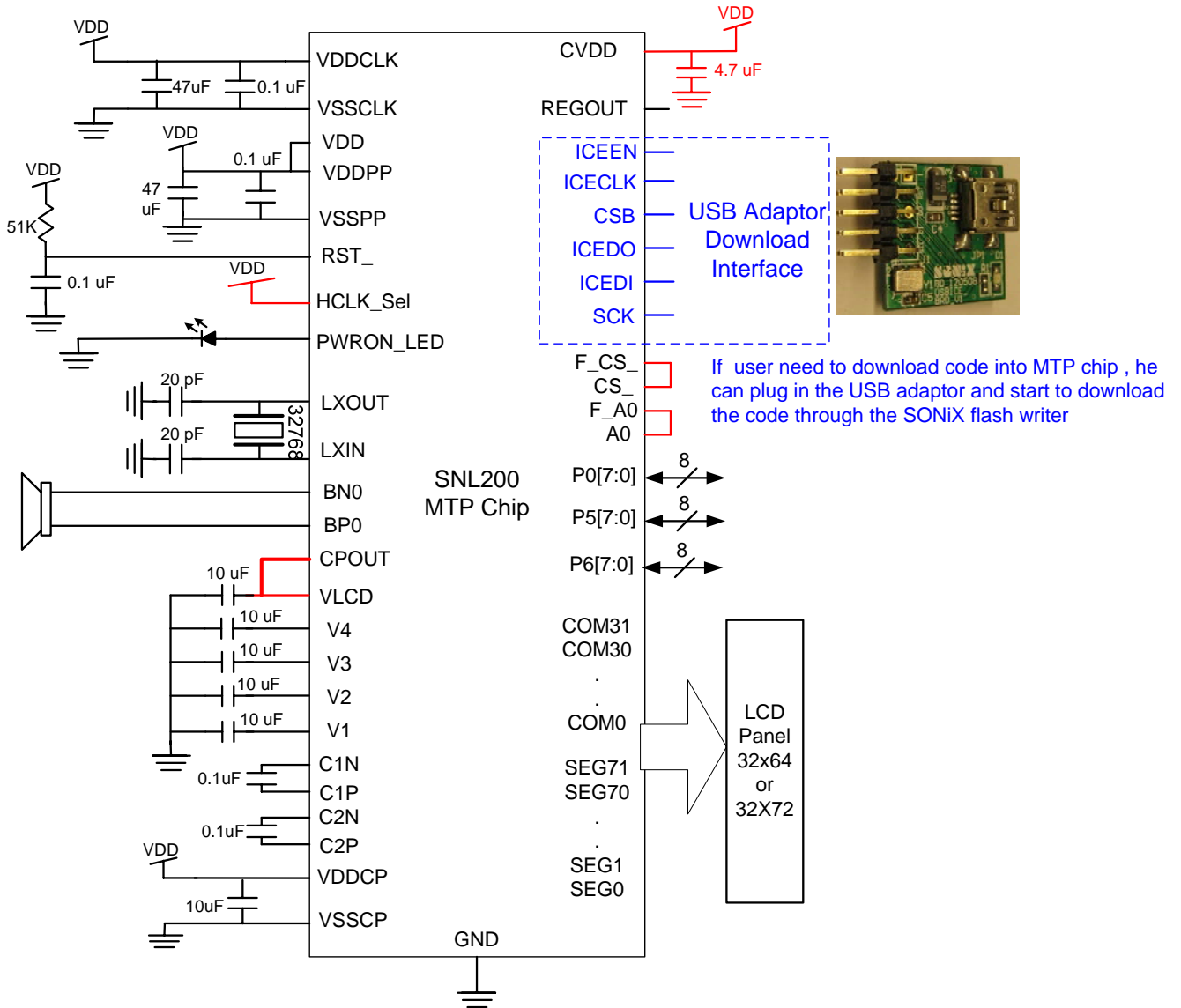
PAD SIZE	E2		D2	
	MIN.	MAX.	MIN.	MAX.
△ 370X370MIL	8.795	9.398	8.795	9.398

NOTES:

- JEDEC OUTLINE :
MS-026 BJC
MS-026 BJC-HD(THERMALLY ENHANCED VARIATIONS ONLY)
- DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H].
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

6 Application circuit

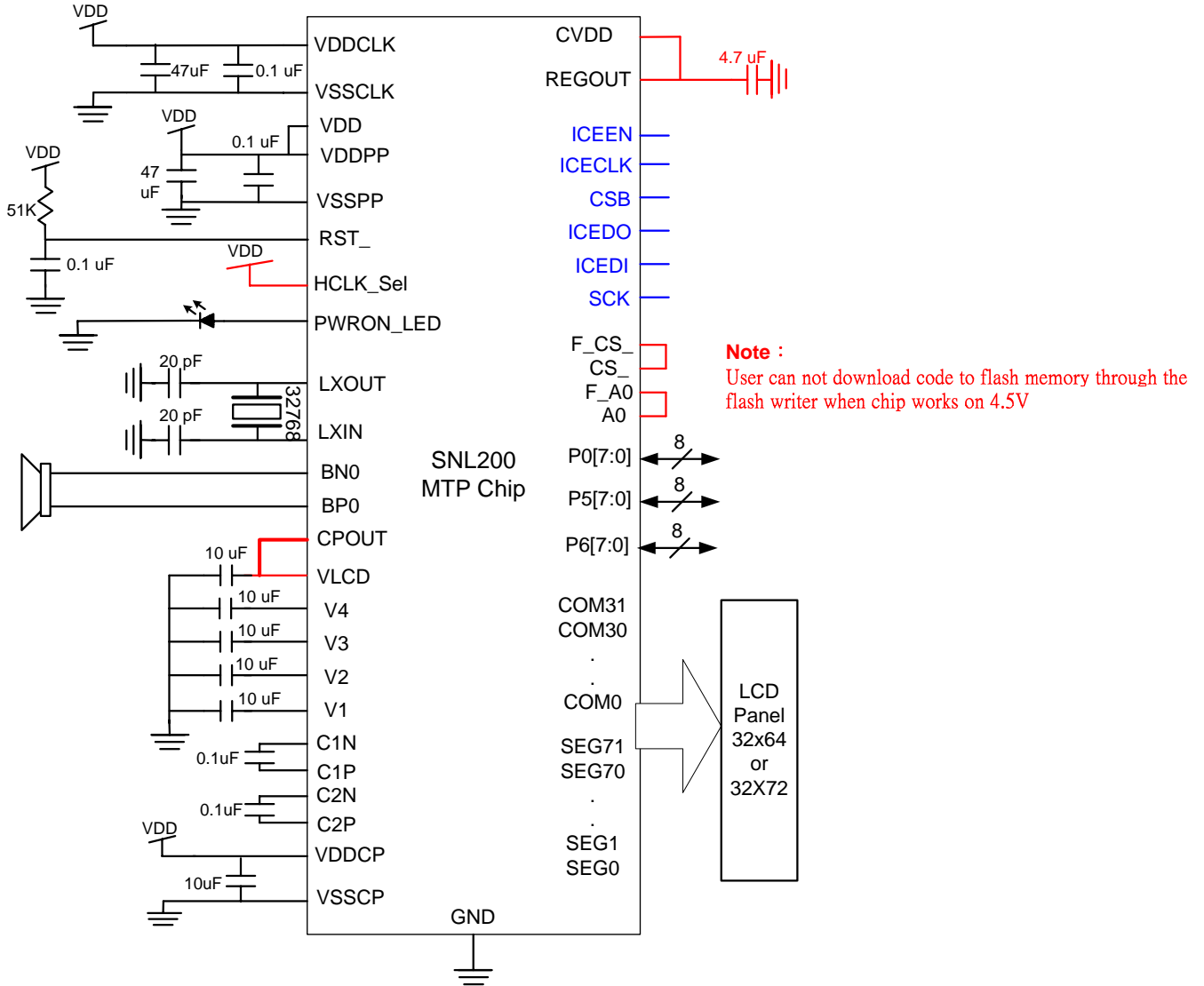
- ◆ **Power Supply: 3 V**
- ◆ **System Clock: 16M Int. Rosc**
- ◆ **Low Clock: 32768 X'tal**
- ◆ **Voice output: Push Pull DAC Output**



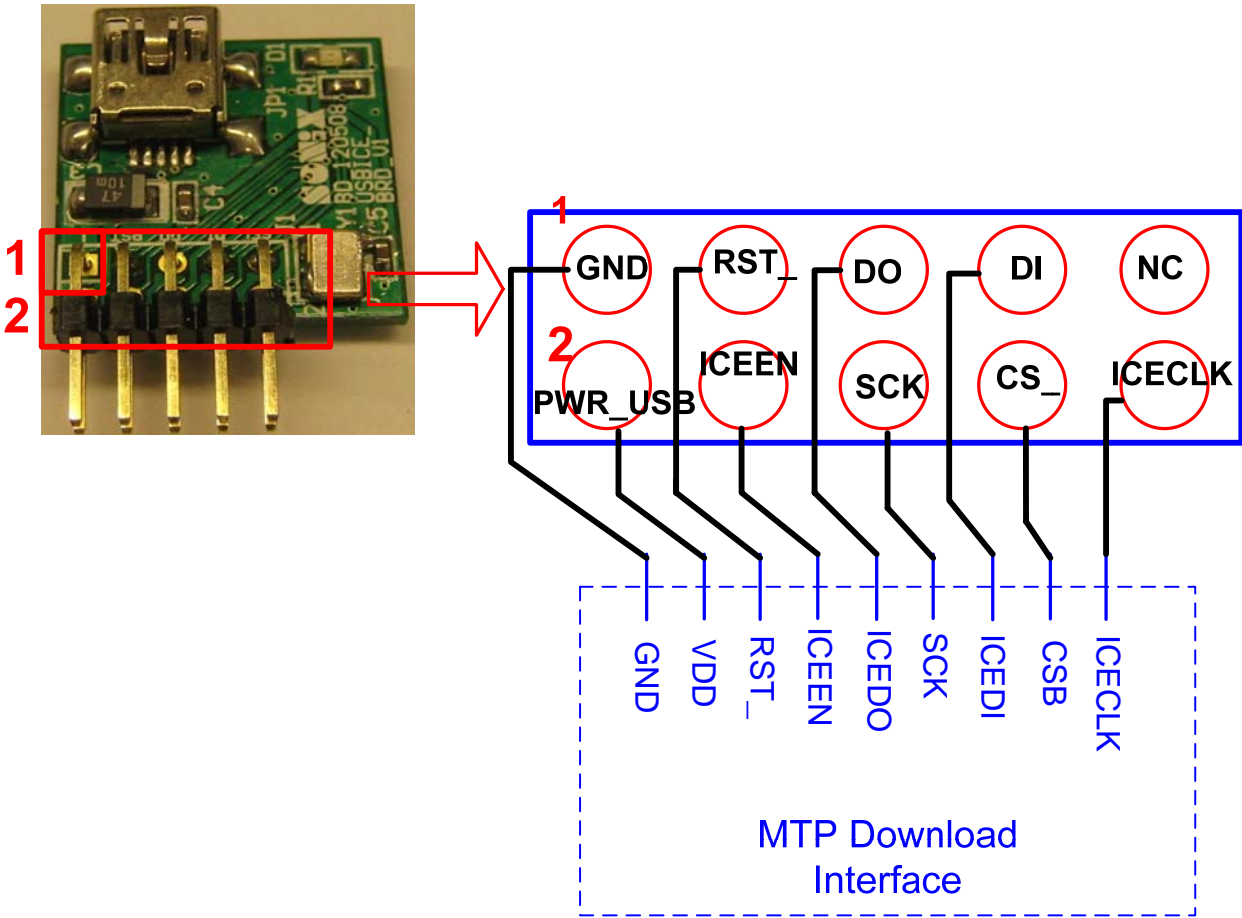


SNL200MTP (with 2Mx16 Flash Memory)

- ◆ **Power Supply: 4.5 V**
- ◆ **System Clock: 16M Int. Rosc**
- ◆ **Low Clock: 32768 X'tal**
- ◆ **Voice output: Push Pull DAC Output**



7 USB Adaptor Connection





8 ELECTRICAL CHARACTERISTICS

Item	Sym.	Min	Typ.	Max	Unit	Condition
Operating Voltage	V _{DD}	2.4	-	5.1	V	
Standby Current 1	I _{SBY}	-	6	-	uA	V _{DD} =3V
Standby Current 2	I _{SBY}	-	9	-	uA	V _{DD} =5V
Normal mode operating current	I _{NOPR}	-	12	-	mA	V _{DD} =3V, no load, push pull turned off. Execute "NOP" instruction
Slow mode operating current	I _{SOPR}	-	70	-	uA	V _{DD} =3V, CPU clock is 32 KHz, Push Pull off, LCD driver off
Idle mode operating current 1	I _{SOPR}	-	50	-	uA	V _{DD} =3V, CPU halt, Push-Pull off, LCD driver on, without panel.
Idle mode operating current 2	I _{SOPR}	-	10	-	uA	V _{DD} =3V, CPU halt, Push-Pull off, LCD driver off
Input pull low impedance of P0,P5,P6	R _i	-	1M	-	Ω	V _{DD} =3V
P0, P5, P6 Drive Current	I _{OD}	-	4	-	mA	V _{DD} =3V, V _O =2.4V
P0, P5, P6 Sink Current	I _{OS}	-	6	-	mA	V _{DD} =3V, V _O =0.4V
Low voltage Reset (LVR)			2.4		V	
Push-Pull current	I _{PP}	-	70	-	mA	V _{DD} =3V, Output 1Khz Sin wave.
LCD driver voltage	VLCD		5.73		V	± 5% @ V _{DD} =5V, LCDREG register = 0x74, No load
Frequency shift	Rosc		16.384		MHz	± 3% @3V
Input Low voltage	V _{IL}	V _{SS}	-	0.3* V _{DD}	V	
Input high voltage	V _{IH}	0.7* V _{DD}	-	V _{DD}	V	



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