======== CONTENTS ========

1. INTRODUCTION 3

2. FEATURES 3

2.1 H/W FEATURE 3
2.2 F/W FEATURE 4

3. PIN ASSIGNMENTS 4

4. SYSTEM DESCRIPTION 5

4.1 SYSTEM CLOCK 5
4.2 INTERNAL ROM 5
4.3 INTERNAL RAM 5
4.4 I/O PORT 6
4.5 TIMER/COUNTER 6

5. INTERRUPT 7

6. EXTERNAL STORAGE DEVICES 7

6.1 PROGRAM SPI FLASH CONTROLLER 7

7. AUDIO CODEC 7

7.1 ANALOG TO DIGITAL CONVERTER (ADC) 7
7.2 DIGITAL TO ANALOG CONVERTER (DAC) 8

8. COMMUNICATION INTERFACE 8

8.1 I2S INTERFACE 8
8.2 SPI INTERFACE 8

9. REGULATOR 8

10. ABSOLUTE MAXIMUM RATING 8

11. ELECTRICAL CHARACTERISTICS 9

12. APPLICATION CIRCUIT 10

AMENDENT HISTORY

Version	Date	Description
Ver 1.0	2010/10/08	Formal release
Ver 1.1	2012/04/16	Update info at Electrical Characteristics
Ver 1.2	2012/05/17	Update info about Standby Current
Ver 1.3	2013/11/08	Add Chap 10: Absolute Maximum Rating

1. Introduction

The SNC71101 is a high quality 16-bit DSP recording engine. With high quality 16-bit ADC &14-bit DAC, the chip can record high quality audio data for further processing. With 48MIPs DSP engine, the recorded data can be compressed for storage. The built in maximum 2KW program RAM is suitable to execute customer's program. The chip built in 44KW program ROM.

There are Audio32 16~32Kbps, SNX8K 8Kbps, melody algorithms for playback, and sound effect such as Robot, Echo, Pitch Up/Down….and so on. In addition, User can run their own application code at SPI Flash, and move codes into internal program ram, which can run at 48MHz.

2. Features

2.1 H/W Feature

- Power supply : 2.7 ~ 3.6V
- Built-in 16-bit DSP core
- 48 MIPS CPU Performance
- Clock Type:
  - 48MHz for system clock (Pumping from 12MHz IHRC by PLL)
  - 32768Hz crystal oscillator or external Rosc for system clock
- Operation Mode:
  - Normal mode (hi-speed clock enable)
  - Slow mode (hi-speed clock disable, slow-speed clock enable)
  - Watch mode (chip entry power-down mode and wake-up per 0.5/1 sec automatically)
  - Power-down mode (both hi-speed and low-speed clock disable)
- 3 for 16-bit Timers, 1 Watch Dog Timer, 1 RTC
  - Timers with Individual pre-scalar and auto-reload function
  - Event Counter (Combine Timer and Input Pin P0.0~P0.2)
  - Watch Dog Timer (WDT) with 0.25/0.5/1/2-sec period
  - RTC with 0.5/1-sec period
- Interrupt Sources
  - 3 for Timers, 1 for RTC, 1 for Communication SPI, 1 for AD, 1 for DA, 1 for I2S
  - 3 for External (P0.0~P0.2), 1 for DMA
- 44K * 16 Internal Program ROM
- Total 4K*16 Internal RAM memory for Program and working RAM
  - Maximum 2K*16 for Program RAM
- Support Barrel Shifter and 16×16 to 32-bit multiplier
- DMA provided for Program SPI flash controller
- Low Voltage Detect (LVD)
- Low Voltage Reset (LVR)
- IO Pins
  - 32 GPIO

2.2 F/W Feature

- Recording Function
  - Support SNX8K 8K Sample Rate, 8Kbps for Recording
  - Long time recording with auto Serial flash Sector Erase
  - Support LVD to protect Serial Flash data
  - Support Auto Recording function
- Playback Function
  - Support several algorithms for foreground and background playback
  - Foreground + Background
    - ✓ SNX8K + Audio32
    - ✓ SNX8K + max 12CH MIDI
    - ✓ Audio32 + Audio32
    - ✓ Audio32 + max 12CH MIDI
  - Support Sound Effect Playback
    - ✓ Robot
    - ✓ Echo
    - ✓ Change Speed
    - ✓ Pitch Shift
  - Support Wave Mark and Silence Detection
  - Support Play, Pause, Resume, Stop, Next, Last and Volume Control
- Power Saving
  - Support Four kinds of Operation Mode function for User to save power

3. Pin Assignments

Symbol	Descriptions	No. of Pin	Pin Count
VREG	Power for Regulator	1	1
VOUT	Regulator voltage output	1	2
GND_REG	Regulator Ground	1	3
CVDD	Power + for core	2	5
CVSS	Power - for core	2	7
VDDIO	Power for IO	2	9
VSSIO	GND for IO	2	11
LXIN	Low speed clock crystal input	1	12
LXOUT	Low speed clock crystal output	1	13
VO1	DAC output	1	14
VDD_SDAD	Power for SD_ADC	2	16
VSS_SDAD	GND for SD_ADC	2	18
MIC_P	SD_ADC Microphone differential input +	1	19
MIC_N	SD_ADC Microphone differential input -	1	20
MIC_S	SD_ADC Microphone single-end input	1	21
VMID	SD_ADC Middle reference voltage	1	22
AUX	SD_ADC AUX analog input for Line-in	1	23
FMIN	SD_ADC FM analog input for Line-in	1	24
MICBIAS	MIC bias voltage	1	25
RSTB	Chip reset	1	26
TEST	For test only	1	27
P0.0~P0.15	General I/O port P0.0~P0.15	16	43

P1.0~P1.15	General I/O port P1.0~P1.15	16	59
Ext_LDO	Enable/disable External LDO	1	60

4. System Description

4.1 System Clock

SNC71101 is a dual clock system that it provides high-speed clock (12MHz IHRC up to 48MHz) and low-speed clock (12MHz or 32768Hz). The SNC71101 use internal PLL to up sample clock speed to 48MHz

4.2 Internal ROM

SNC71101 provides hi-compression algorithm to compress voice data in order to save more memory size. So all the de-compression program has be built at the internal ROM of SNC71101 and system will reserved some necessary ROM space for those de-compression program automatically once user active the de-compression function. There are totally 44K words of SNC71101 internal ROM.

Address Range	Size (Words)	Usage	DSP	DMA
0x00000000 ~ 0x00007FFF	32K	Program ROM 1	R	---
0x00200000 ~ 0x00202FFF	12K	Program ROM 2	R	---

4.3 Internal RAM

SNC71101 built-in totally 4KW Internal RAM for application. However, the high-half addressing RAM can be set as Program-RAM region, and this size is programmable which can from 256 Word to 2K Word. If the RAM is be act as Program-RAM, this region will map to address 0x300800 ~ 0x300FFF.

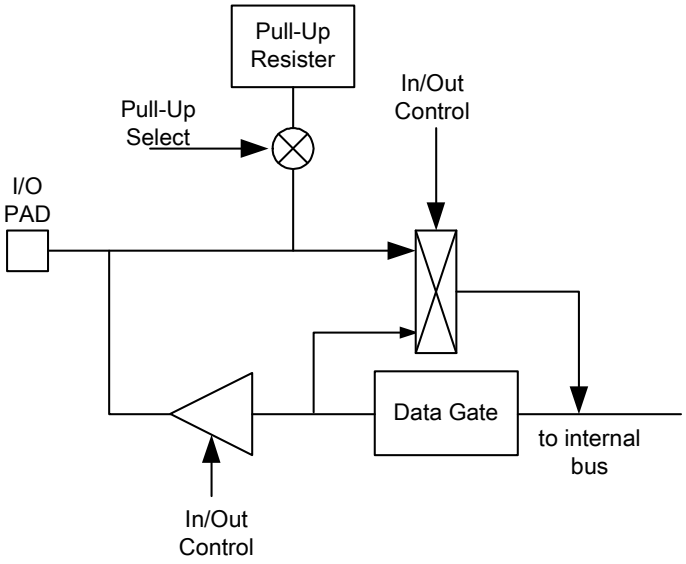
Address Range	Size (word)	Usage	DSP	DMA
0x0000 ~ 0x07FF	2K	Working RAM	R/W	R/W
0x0800 ~ 0x0FFF	2K	Working/Program RAM (*)	R/W	R/W

(*) : Working RAM address 0x0800~0x0FFF is mapping to Internal Program memory address 0x300800~0x300FFF

4.4 I/O Port

SNC71101 provides totally 32 I/O pins (P0.0~P1.15). The input pull-high resistor of each pin can be programmed by port pull-high register and the direction of I/O port is selected by port direction register. The I/O port can wake the chip up from the stop mode and watch mode. These 32 programmable I/O pins provides not only a simply input/output function but also can configure to be chip select pins of extension bus and multi-function peripheral interface. For the detail please refer to following sections.

The internal structure of I/O pins is showed in Figure-1.



I/O Configuration of Port0.0 ~ Port1.15

Figure-1

4.5 Timer/Counter

SNC71101 provides three 16-bit timer/event counters (T0/T1/T2). Each timer is 16-bit binary up-count timer with pre-scalar and auto-reload function. ***Timer 0 (T0) was used when voice playing, so user should avoid to use T0***.

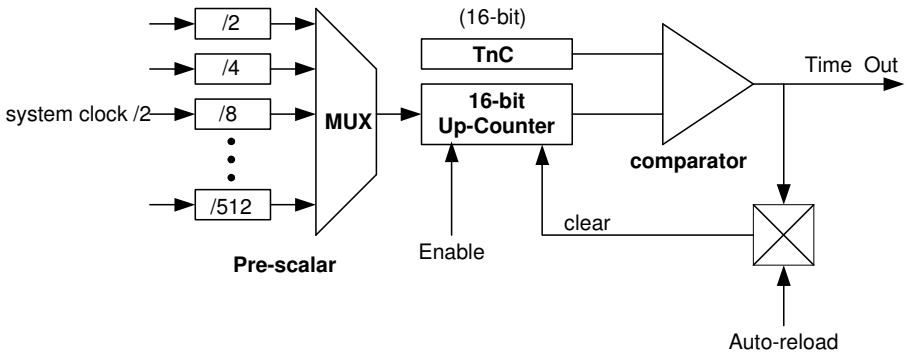


Figure-2

5. Interrupt

At the moment when SNC71101 enters the interrupt service routine, the GIE bit (in INTEN) will be cleared to "0"for blanking other interrupt. However, during this stage, other enabled interrupt sources still can issue their requests but the requests are queued in INTRQ. GIE will be restored to "1" while DSP exits ISR. Then the other valid interrupt can be granted and served immediately.

Interrupt Vector	Priority	Entry Location	Descriptions
Reset	x	0x000000	Reset
reserved		0x000010	
AD	3	0x000014	AD FIFO full
T0	4	0x000018	T0 overflow
P0.0	5	0x00001C	Falling/Raising edge of P0.0
T1	6	0x000020	T1 overflow
P0.1	7	0x000024	Falling/Raising edge of P0.1
T2	8	0x000028	T2 overflow
P0.2	9	0x00002C	Falling/Raising edge of P0.2
reserved		0x000030	
DA	10	0x000034	DA FIFO empty
SPI	2	0x000038	SPI Interrupt
reserved		0x00003C	
I2S	1	0x000040	I2S Interrupt
reserved		0x000044 ~ 0x000054	
RTC	11	0x000058	RTC overflow
reserved		0x00005C ~ 0x000078	

6. External Storage Devices

6.1 Program SPI Flash Controller

SNC71101 built-in a SPI Flash controller interface to support 1/2/4 bit read/write mode, it can run 6/12/24/48 MHz clock frequency. In additional, SNC71101 can run program on SPI Flash.

7. Audio CODEC

7.1 Analog to Digital Converter (ADC)

In SDC71101 has one channel high performance Analog-to-Digital Converter (ADC) for micro-phone application, and its typical SNR is 90dB. This Analog-to-Digital Converter build-in PGA(~12dB ~ +33dB, 1.5dB/step), BOOST(0 ~ +30dB) and AGC function. The AGC

parameter is programmable for different application. It supports 8/12/16/22.05/24/32/44.1/48KHz sample rate for user's application.

7.2 Digital to Analog Converter (DAC)

A 14-bit DAC are embedded in SNC71101, and its typical SNR is 65dB. A 16x16 FIFO is used to prevent the sound glitch when CPU is busy. It supports 8/12/16/22.05/24/32/44.1/48KHz sample rate for user's application.

8. Communication Interface

8.1 I2S Interface

SNC71101 built-in an I2S interface, and it can output digital audio data to external audio DAC. Two L/R channel 16x16 FIFO is used to prevent the sound glitch when CPU is busy.

8.2 SPI Interface

The SPI (serial peripheral interface) is a synchronous serial bus that provides good support for communication with SPI-compatible peripheral devices. The SPI peripheral is a synchronous, 7-wire interface consisting of two data pins (SPITxD and SPIRxD); two additional pins (SPIED3 and SPIED2) for 4-bit mode access, two slave select pins (/SS1, /SS2); and a synchronous clock pin (SCLK). The two data pins permit full-duplex and half-duplex operation to other SPI-compatible devices. The SPI also includes programmable baud rates, clock phase (CPHA), and clock polarity (CPOL).

9. Regulator

The SNC71101 built-in a linear regulator for core power (CVDD). The accuracy output voltage is 1.8V±0.18V and it can be power downed by software.

10. Absolute Maximum Rating .

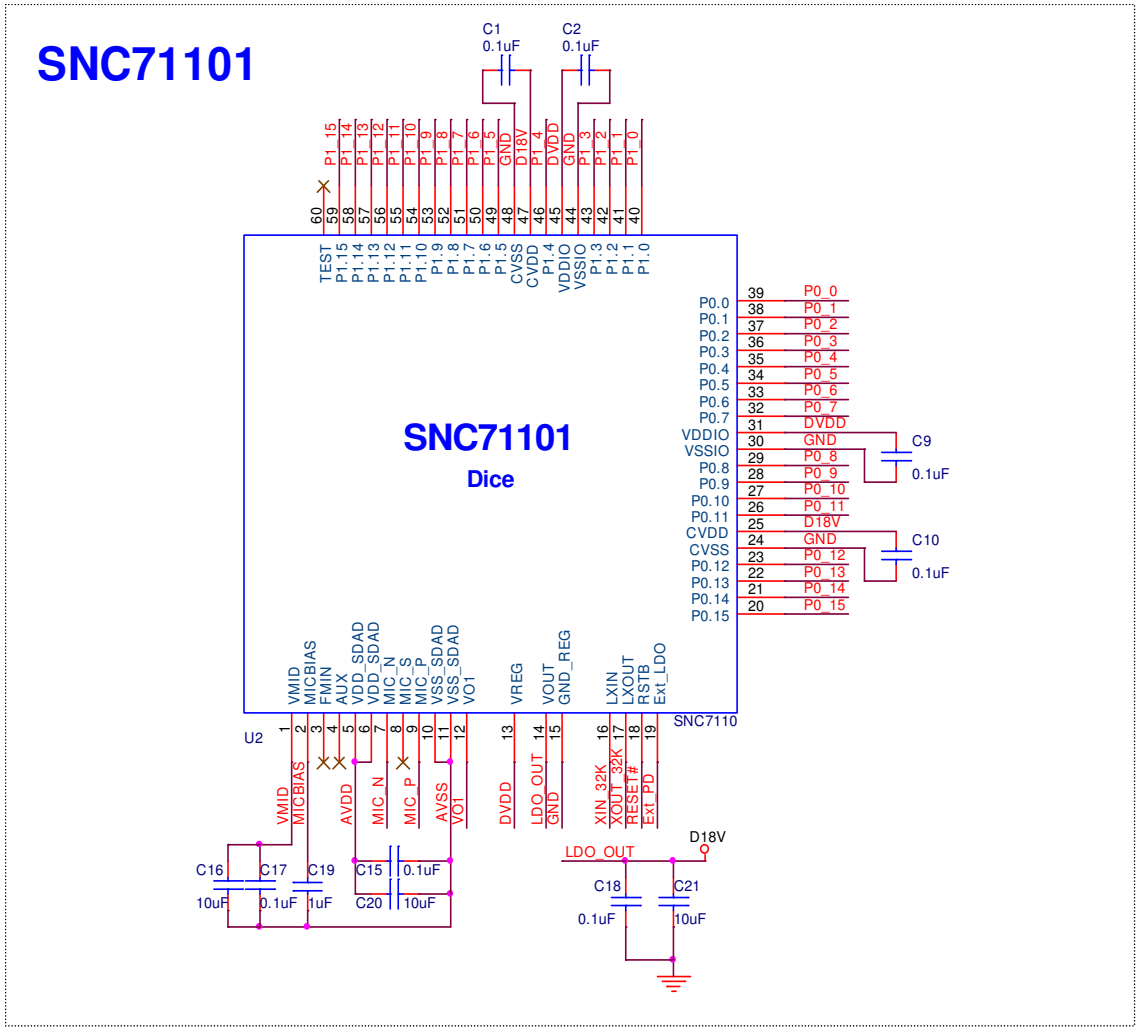
Items	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	-0.3	6.0	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}-0.3	V
Operating Temperature	T_{OP}	0	55.0	℃
Storage Temperature	T_{STG}	-55.0	125.0	℃

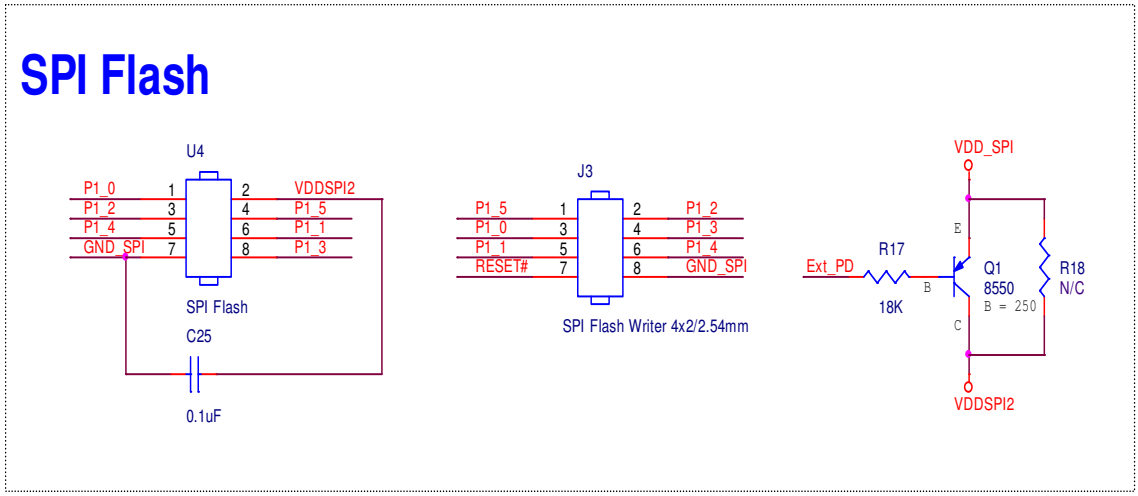
11. Electrical Characteristics

Item	Sym.	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.7	-	3.6	V	
Standby current	I_{SBY}	-	-	8	uA	V_{DD}=3V, no load
Operating Current	I_{OPR}	-	20		mA	V_{DD}=3V, no load
Input High Level	V_{IH}		$0.7V_{DD}$		V	
Input Low Level	V_{IL}		$0.3V_{DD}$		V	
Output High Level	V_{OH}		2.4		V	
Output Low Level	V_{OL}		0.4		V	
Input Pull-High Resistor	R_{PH}		75K		Ω	
Drive current of P0, P1.0, P1.6~P1.15,	I_{OD}	-	4	-	mA	V_O=2.4V
Sink current of P0, P1.0, P1.6~P1.15,	I_{OS}	-	4	-	mA	V_O=0.4V
Drive current of P1.1~P1.5	I_{OD}		16		mA	V_O=2.4V (note1)
Sink Current of P1.1~P1.5	I_{OS}		16		mA	V_O=0.4V (note1)

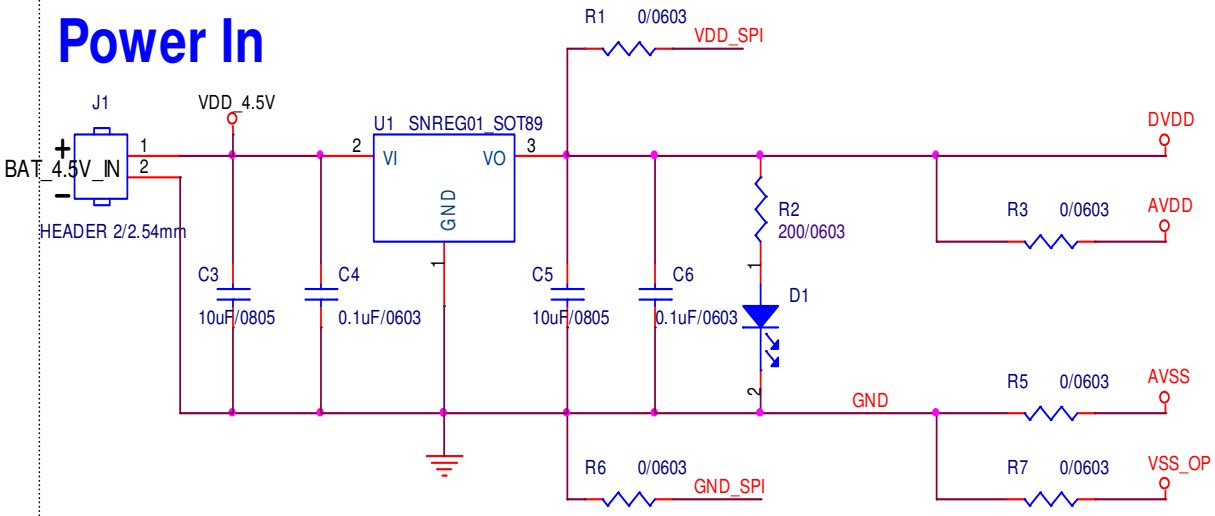
Note1: P1.1~P1.5 own two option for drive / sink current (16 or 12mA), the default is 16mA

12. Application Circuit

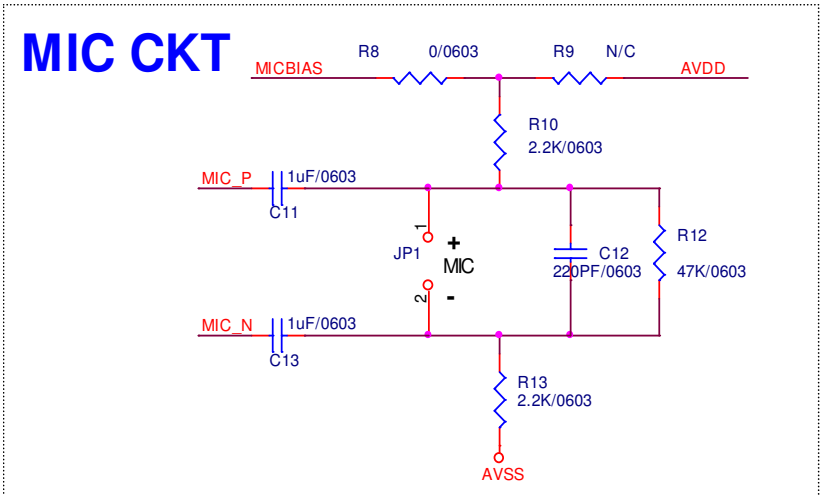




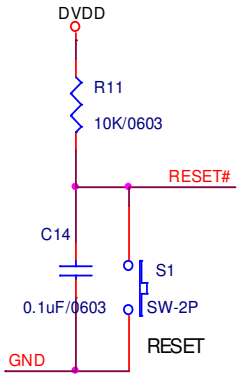
Power In



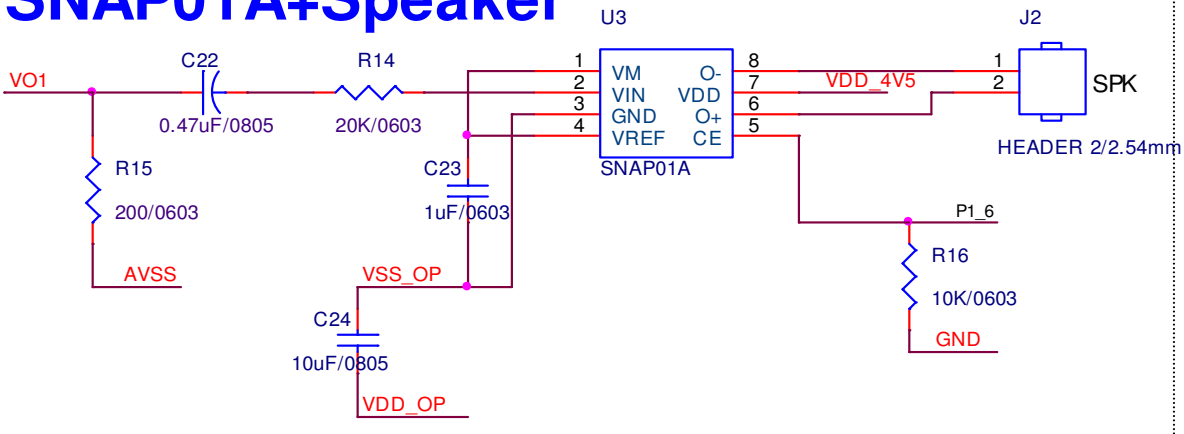
MIC CKT



Reset



SNAP01A+Speaker



DISCLAIMER

The information appearing in SONiX web pages (“this publication”) is believed to be accurate.
However, this publication could contain technical inaccuracies or typographical errors. The reader should not assume that this publication is error-free or that it will be suitable for any particular purpose. SONiX makes no warranty, express, statutory implied or by description in this publication or other documents which are referenced by or linked to this publication. In no event shall SONiX be liable for any special, incidental, indirect or consequential damages of any kind, or any damages whatsoever, including, without limitation, those resulting from loss of use, data or profits, whether or not advised of the possibility of damage, and on any theory of liability, arising out of or in connection with the use or performance of this publication or other documents which are referenced by or linked to this publication.
This publication was developed for products offered in Taiwan. SONiX may not offer the products discussed in this document in other countries. Information is subject to change without notice. Please contact SONiX or its local representative for information on offerings available. Integrated circuits sold by SONiX are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only.
The application circuits illustrated in this document are for reference purposes only.
SONIX DISCLAIMS ALL WARRANTIES, INCLUDING THE WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. SONIX reserves the right to halt production or alter the specifications and prices, and discontinue marketing the Products listed at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders.
Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by SONIX for such application.