
SNC7330 Series

32-bit Dual-core Microcontroller

Features

CPU

- Two ARM® Cortex®-M3 Processors (Core 0 and Core 1), each with frequency up to 96 MHz
- One serial wire debug (SWD) port
- Built-in memory protection unit (MPU)
- Built-in nested vectored interrupt controller (NVIC)
- One interrupt signal for the interaction between the two cores
- System tick (SysTick) timer
- System clocks
 - 12 MHz IHRC at 1.1V
 - 12 MHz XTAL at 1.1V
 - 32 kHz XTAL and ILRC at 3.3V for RTC
- Fast Fourier transform (FFT) and finite impulse response (FIR) accelerators (Core 1)

Memory

- Internal memory
 - ROM size for Core 0: 64 KB
 - PRAM size for Core 0: 64 KB
 - ROM size for Core 1: 128 KB
 - Shared AHB SRAM: 128 KB
 - Shared Mailbox RAM: 4 KB
- SPI NOR flash controller (SPIFC)
 - Clock frequency: Up to 48 MHz
 - Size: Up to 256 MB
 - Supports 1/2/4-bit data mode
 - Supports eExecute-In-Place (XIP)
- Supports one 16 KB I-cache
- ROM and RAM remapping
- DMA controller with eight channels

System

- Power Management Unit (PMU)
 - Operation modes: Normal/deep sleep/deep power-down (DPD)
 - DPD with optional RTC wakeup
- Low voltage reset (LVR)
 - 0.9V for cores
 - 1.8V for I/O (power-on)
 - 2.1V for I/O (normal mode)

Clock

- Real time clock (RTC)
- Two 8-bit watchdog timers (WDT)

Audio Codec

- Audio sample rates: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 kHz
- 24-bit Sigma Delta ADC with 100 dB Signal-to-Noise Ratio (SNR) performance

- Single-ended or differential microphone inputs
- 24-bit Sigma Delta DAC with 100 dB Signal-to-Noise Ratio (SNR) performance
- Mono Class-AB amplifier with speaker driver

Peripheral

- 10-bit SAR ADC 1 MSPS up to six input channels
- Serial Peripheral Interface 0 (SPI0) controller
 - Master or slave mode operation
 - Supports 4-bit to 16-bit frame size
 - Supports 8-frame FIFO for receiver and transmitter
 - Supports 1-bit data mode only
- Serial Peripheral Interface 1 (SPI1) controller
 - Master mode only
 - Supports 8-bit to 48-bit frame size in buffer mode
 - Supports 1/2/4-bit data mode
 - Supports 1/4/8-bit error correcting code (ECC)
- Up to two universal asynchronous receivers/transmitters (UART)
- USB 2.0 high speed device
 - Compliant with USB 2.0 specification
 - Supports one dedicate control endpoint and seven configurable endpoints
 - Supports MSC/HID/UAC class
- Up to two master/slave inter-integrated circuit (I²C) buses
- Up to three integrated interchip sound (I²S) interfaces
 - Communicates in master or slave mode
 - Connects to audio codecs in slave mode only
 - Left/right justified format
- SD/SDIO controller
- Up to eight timers/counters with 32-bit pre-scale counter (CT32B)
 - Each supports one capture input and up to three PWM outputs
- Up to 36 general-purpose input/output (GPIO) pins

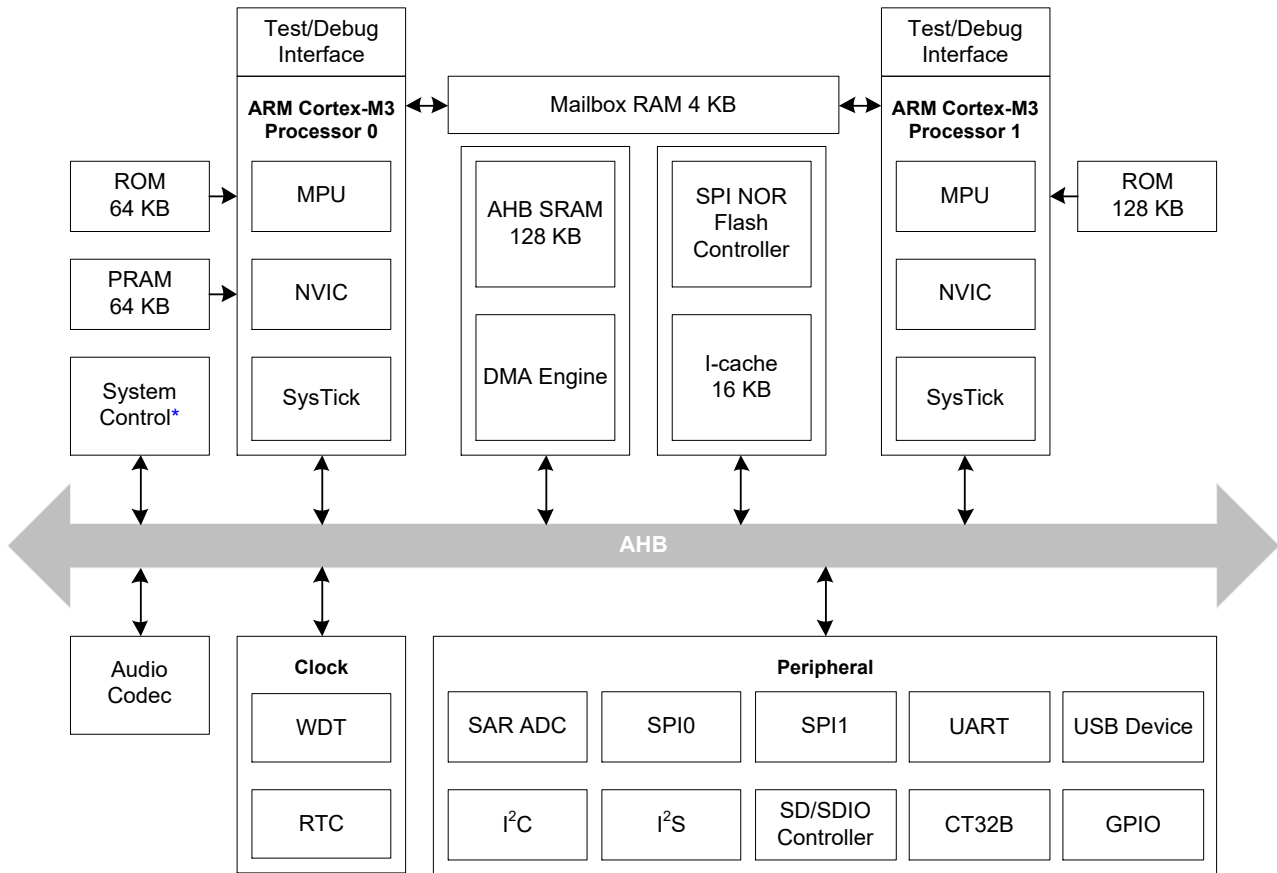
Voltage

- Operating voltage:
 - 3.3V typically
 - 5V typically (with audio codec)
- Core: 1.1V typically
- LDO: 1.1V for core; 1.8V for audio codec

Package

- QFN32L (4 x 4 mm)
- QFN52L (6 x 6 mm)
- LQFP64L (7 x 7 mm)

Functional Block Diagram



* For ARM Cortex-M3 Processor 0 only

Description

The SNC7330 series has two 32-bit ARM® Cortex®-M3 processors in symmetric dual-core architecture. Each of the two cores controls respective designated peripherals, cooperates with the other, and can be independently programmed. The two processors of the SNC7330 series operate at a frequency of up to 96 MHz individually. Supporting RAM array with data bandwidth of up to 5 GB/sec and deep power-down mode consuming less than 1 µA, the SNC7330 series is designed for high performance and low power consumption embedded applications.

The SNC7330 series offers standard peripherals, including SAR ADC, SPI, UART, USB device, I²C, I²S, SD/SDIO controller, and GPIOs. The software development kit (SDK) provides various sample codes that are compatible with the Keil® MDK-ARM® compiler. With the peripherals and the SDK, the SNC7330 series makes seamless integration and streamlined development possible for applications such as gaming keyboards and gaming mice.

Device Comparison

Device	Package (mm)	USB Device	I/O	SAR ADC	SPI	UART	I ² C	I ² S	SD/SDIO	PWM	Audio Codec	Flash
SNC73310	QFN52L (6 x 6)	✓	36	6-CH	2	2	2	3	✓	24	- ¹	-
SNC73313	QFN52L (6 x 6)	✓	36	6-CH	2	2	2	3	✓	24	- ¹	512 KB
SNC73314	QFN52L (6 x 6)	✓	36	6-CH	2	2	2	3	✓	24	- ¹	1 MB
SNC73323	LQFP64L (7 x 7)	✓	27	6-CH	2	2	1	1	✓	21	MIC x2 SPK x1 HP x1	-
SNC73381	QFN32L (4 x 4)	✓	21	4-CH	2	2	2	1	✓	20	-	512 KB

¹ Supports external audio codec, SNAUD01 or SNAUD02.

Absolute Maximum Ratings^{2 3}

Parameter		MIN.	MAX.	Unit
Supply voltage	V _{DD} /V _{DD11}	-0.3	1.2	V
	V _{DD33}		3.63	
Supply voltage for audio codec	V _{DD18}	-0.3	1.9	
	V _{DDSPK}		5.5	
Input voltage	V _{IN11}	-0.3	1.2	
	V _{IN33}		3.63	
Input voltage for audio codec	V _{IN18}	-0.3	1.9	
	V _{IN5}		5.5	
Ambient temperature	T _A	0	75	°C
Junction temperature	T _J	-40	125	
Storage temperature	T _{STG}	-40	125	

Recommended Operating Conditions

Parameter		MIN.	TYP.	MAX.	Unit
Device supply voltage, I/O, V _{DD33}	Without audio codec and USB application	2.20	3.30	3.63	V
	Without audio codec and with USB application	2.97			
	With audio codec	3.30			
Supply ground, V _{SS}		0			
Analog supply ground, V _{SSA}		0			
Ambient temperature, T _A		0	–	75	
Junction temperature, T _J		-40	–	125	
Electrostatic discharge, V _{ESD}	Human body model (HBM)	-2000	–	2000	V
	Charged device model (CDM)	-500	–	500	
Speaker amplifier supply voltage, V _{DDSPK}		3.3	5.0	5.5	
Ground for audio codec, V _{SSAUD} , V _{SSSPK}		0			

Electrical Characteristics

Parameter		Conditions (T _A = 25 °C)	MIN.	TYP.	MAX.	Unit
Low voltage reset (3.3V domain)	V _{LVR21}	–	–	2	–	V
Low voltage reset (1.1V domain)	V _{LVR09}	–	0.9	0.95	1.0	
IHRC	F _{IHRC}	Accuracy to ± 2%	11.76	12	12.24	MHz
SYS_ILRC	F _{ILRC}	For WDT frequency	–	32	–	kHz
Internal pull-up/pull-down resistance	R _{PU} /R _{PD}	–	30K	40K	66K	Ω
IO driving CFG0 ⁴	IO _{CFG0}	All GPIOs	–	3.8	–	mA
IO driving CFG1 ⁴ (default)	IO _{CFG1}		–	7.7	–	

² Long-term exposure to absolute maximum ratings may affect device reliability, and permanent damage may occur if the operation exceeds the maximum ratings.

³ All voltage values are with respect to V_{SS}.

⁴ CFG_x represents the configurations of GPIO Port *n* driving control register (*x* = 0–3; *n* = 0–2).

Parameter		Conditions (T _A = 25 °C)	MIN.	TYP.	MAX.	Unit
IO driving CFG2 ⁴	IO _{CFG2}		–	11.5	–	
IO driving CFG3 ⁴	IO _{CFG3}		–	15	–	
IO sink CFG0 ⁴	IO _{CFG0}		–	3.8	–	
IO sink CFG1 ⁴ (default)	IO _{CFG1}		–	7.5	–	
IO sink CFG2 ⁴	IO _{CFG2}		–	11	–	
IO sink CFG3 ⁴	IO _{CFG3}		–	14.5	–	
LDO11 output voltage	V _{LDO11}	–	1.11	1.15	1.19	V
LDO11 output current	I _{LDO11}	–	–	–	100	mA
LDO18 output voltage	V _{LDO18}	With audio codec	1.7	–	1.87	V
SAR ADC ENOB	ENOB	–	–	9	–	bits
SAR ADC DNL	DNL	–	-2	–	2	LSB
SAR ADC INL	INL	–	-2	–	2	
Sigma Delta Analog-to-Digital Converter (ADC for audio codec)						
Full scale input	V _{INFS}	PGABST = 0 dB PGAGAIN = 0 dB	–	1.0 0	–	V _{rms} dBV
Signal-to-noise ratio	SNR	Gain = 0 dB, A-weighted	–	100	–	dB
Total harmonic distortion + noise	THD + N	Input = -3 dBV	–	-85	–	
Microphone inputs and programmable gain control						
Programmable PGA gain	–	–	-12	–	35.25	dB
Programmable PGA gain step size		Guaranteed monotonic	–	0.75	–	
Programmable boost gain		–	0	20	50	
Microphone bias						
Middle voltage	V _{MID}	–	–	0.5* LDO18	–	V
Bias voltage	V _{MICBIAS}	–	–	2.56* V _{MID}	–	
Bias current source	I _{MICBIAS}	–	–	3	–	mA
Full scale output	–	Gain = 0 dB	–	0.8	–	V _{rms}
Signal-to-noise ratio	SNR	Gain = 0 dB	–	100	–	dB
Total harmonic distortion + noise	THD + N	Input = -3 dBFS	–	-85	–	
Programmable gain control						
Programmable gain	–	–	-96	–	0	dB
Programmable gain step size	–	Guaranteed monotonic	–	0.375	–	
Speaker output (with 8ohm bridge tied load)						
Full scale output	–	Gain = 0 dB	–	1.6	–	dB

Parameter		Conditions (T _A = 25 °C)		MIN.	TYP.	MAX.	Unit
Supply current in normal mode	I _{CPU12}	Core 0 running CoreMark, HXTAL= on, PLL = off, Clock = HXTAL	F _{CPU} = 12 MHz	–	1.6	–	mA
	I _{CPU24}	Core 0 running CoreMark, HXTAL= on, PLL = on, Clock = PLL	F _{CPU} = 24 MHz	–	7.5	–	
	I _{CPU48}		F _{CPU} = 48 MHz	–	9	–	
	I _{CPU96}	F _{CPU} = 96 MHz	–	12	–		
	I _{DCPU96}	Core 0 and Core 1 running CoreMark, HXTAL= on, PLL = on, Clock = PLL	F _{CPU} = 96 MHz	–	15	–	mA
	I _{USBHS}	Core 0 and Core 1 running USB application ⁵ , HXTAL= on, PLL = on, Clock = PLL		–	43	–	
Supply current in deep sleep mode ⁶	I _{DSL} P	V _{CORE} = 0.95V ⁷ , All clocks = off	F _{CPU} = 0 MHz	–	0.4	1.2	
Supply current in deep sleep mode (USB suspend) ⁸	I _{SUSP}	V _{CORE} = 0.95V ⁷ , All clocks = off		–	0.43	1.2	
Supply current in deep power-down mode without RTC ⁹	I _{DPD}	V _{CORE} = 0V, All clocks = off Without flash and audio codec	F _{CPU} = 0 MHz	–	1	3	μA
		V _{CORE} = 0V, All clocks = off With flash and without audio codec		–	3	5	
		V _{CORE} = 0V, All clocks = off Without flash and with audio codec		–	9	11	
Supply current in deep power-down mode with RTC ⁶	I _{RTC}	V _{CORE} = 0V, RTC clock source = LXTAL Without flash and audio codec	F _{CPU} = 0 MHz	–	6.5	–	μA
	I _{RTC1SEC}	Running RTC application ¹⁰ , RTC clock source = LXTAL Without flash and audio codec	F _{CPU} = 12 MHz	–	110	–	
	I _{RTC5SEC}			–	26	–	
	I _{RTC10SEC}			–	17	–	
	I _{RTC30SEC}			–	10	–	
	I _{RTC60SEC}			–	9	–	

⁵ Transmits/receives data in USB high speed mode.

⁶ Wakes up by GPIO or RTC.

⁷ The LVR09 does not occur in deep sleep mode.

⁸ Wakes up by GPIO, RTC or USB.

⁹ Wakes up by GPIO

¹⁰ Measured throughout an RTC running cycle. In the cycle, the RTC wakes up, and the system loads the application from the flash to the PRAM. After executing 1000 instructions at 12 MHz, the system enters deep power-down mode until the next RTC wakeup.

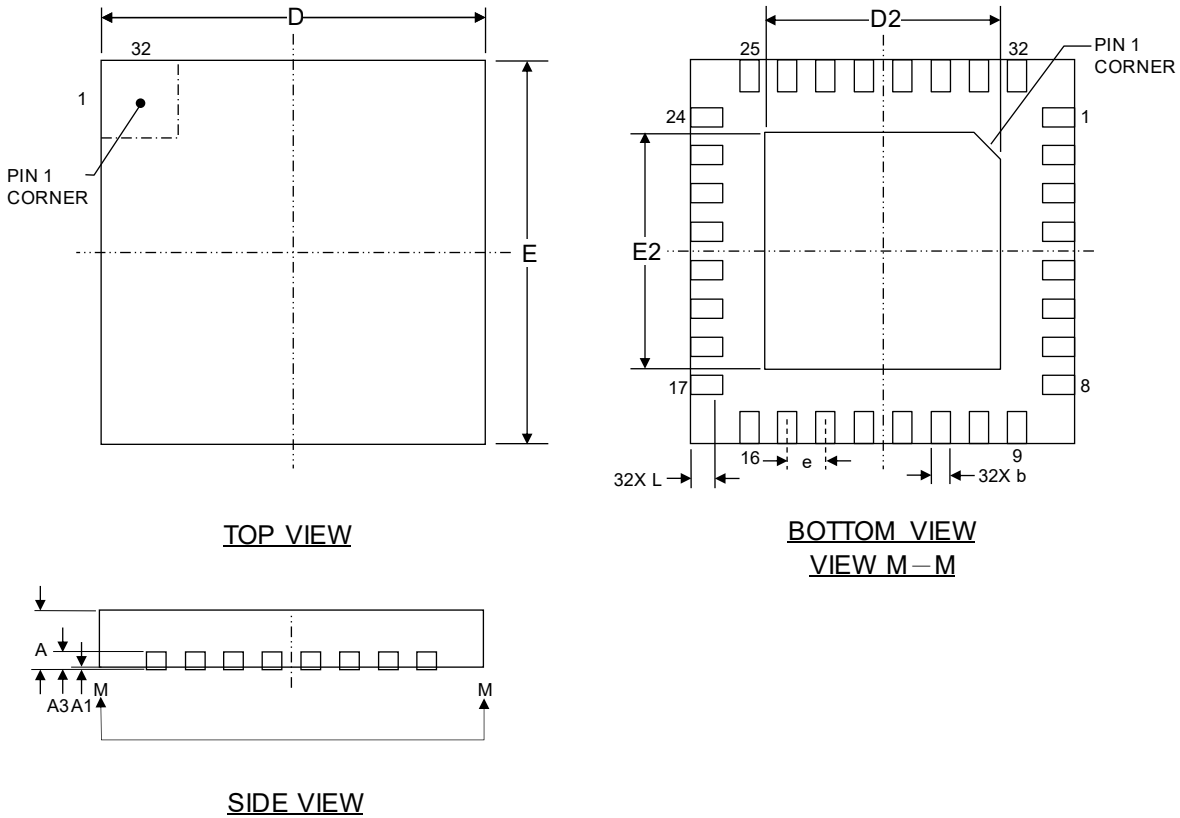
Parameter		Conditions (T _A = 25 °C)		MIN.	TYP.	MAX.	Unit
	I _{RTC}	V _{CORE} = 0V, RTC clock source = LXTAL With flash and without audio codec	F _{CPU} = 0 MHz	–	8.5	–	
	I _{RTC1SEC}	Running RTC application ¹⁰ , RTC clock source = LXTAL With flash and without audio codec	F _{CPU} = 12 MHz	–	112	–	
	I _{RTC5SEC}			–	28	–	
	I _{RTC10SEC}			–	19	–	
	I _{RTC30SEC}			–	12	–	
	I _{RTC60SEC}			–	11	–	
	I _{RTC}			V _{CORE} = 0V, RTC clock source = LXTAL Without flash and with audio codec	F _{CPU} = 0 MHz	–	14.5
	I _{RTC1SEC}	Running RTC application ¹⁰ , RTC clock source = LXTAL Without flash and with audio codec	F _{CPU} = 12 MHz	–	118	–	
	I _{RTC5SEC}			–	34	–	
	I _{RTC10SEC}			–	25	–	
	I _{RTC30SEC}			–	18	–	
	I _{RTC60SEC}			–	17	–	

Revision History

Date	Revision	Description
07-Jun-2022	1.0	Initial release
19-Jul-2022	1.1	Added SNC73332M0UTJG-000 and SNC73380M1NMJG-000 and all related information Updated SPIFC, SPI0, and SPI1 in all related sections Updated ambient temperature in Absolute Maximum Ratings
26-Sep-2022	1.2	Added SNC73334M1NTFG-000 and SNC73381M1NMJG-000 and all related information Updated Features \ System Updated Functional Block Diagram Updated deep power-down current and deep sleep current in Electrical Characteristics
09-Nov-2022	2.0	Removed SNC73330M0NTJG-000, SNC73331M0VTJG-000, SNC73332M0UTJG-000, and SNC73380M1NMJG-000 and all related information Added SNC73310M0NAJG, SNC73311M0VAJG, and SNC73323M0UDFG and all related information Updated IHRC in Electrical Characteristics
02-Dec-2022	2.1	Updated the nomenclature
02-Mar-2023	2.2	Added SNC73313 and SNC73314 and all related information Removed SNC73334 and all related information Updated Electrical Characteristics
02-Jun-2023	2.3	Removed SNC73311 and SNC73323 and all related information Removed LVD33 in Features Added Recommended Operating Conditions Updated Electrical Characteristics
22-Apr-2024	2.4	Updated Features \ Audio Codec Added SNC73323 and all related information Updated Recommended Operating Conditions Updated Electrical Characteristics

Package Dimensions

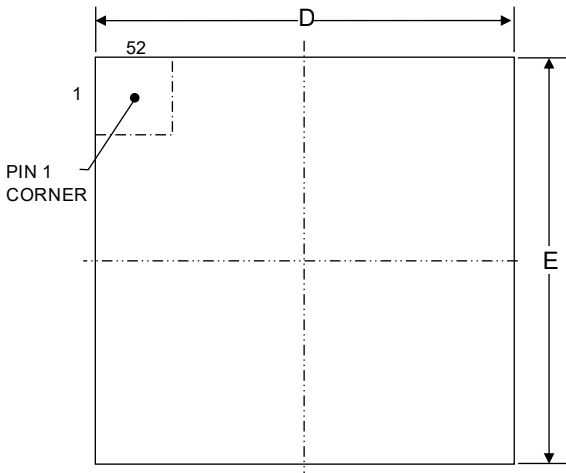
QFN32L (4 x 4 x 0.8 mm/Pitch: 0.4)



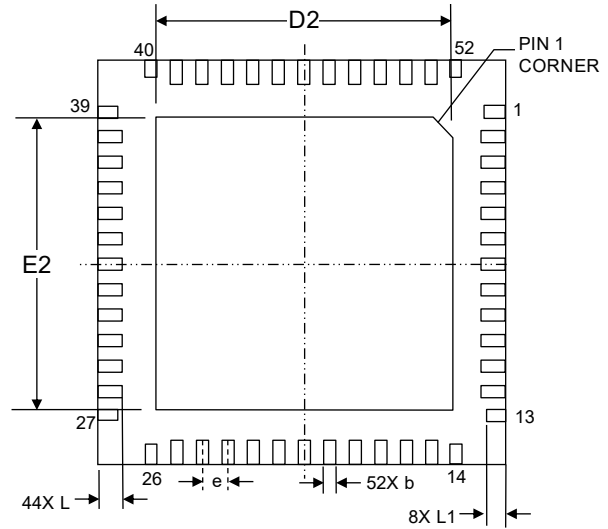
Symbols	Dimension in mm ¹¹			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.028	0.031	0.035
A1	0.00	0.02	0.05	0.000	0.000	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	4.00 BSC			0.157 BSC		
E	4.00 BSC			0.157 BSC		
e	0.40 BSC			0.016 BSC		
D2	2.00	2.45	2.90	0.080	0.096	0.114
E2	2.00	2.45	2.90	0.080	0.096	0.114
L	0.25	0.35	0.45	0.010	0.013	0.017

¹¹ Controlling dimension: millimeter (mm)

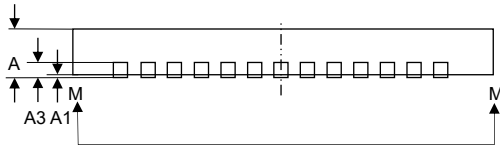
QFN52L (6 x 6 x 0.8 mm/Pitch: 0.4)



TOP VIEW



BOTTOM VIEW
VIEW M-M

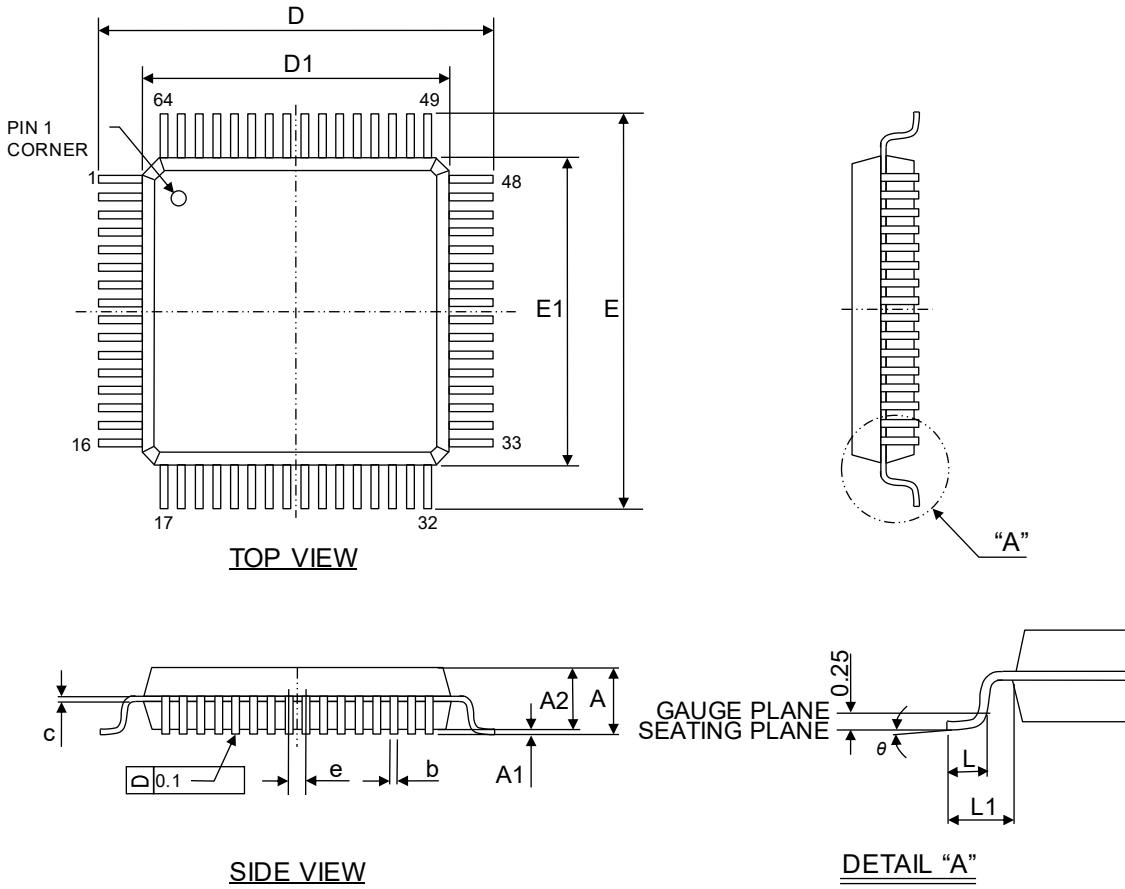


SIDE VIEW

Symbols	Dimension in mm ¹²			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.028	0.031	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.203 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	6.00 BSC			0.236 BSC		
E	6.00 BSC			0.236 BSC		
e	0.40 BSC			0.016 BSC		
D2	4.45	4.60	4.75	0.175	0.181	0.187
E2	4.45	4.60	4.75	0.175	0.181	0.187
L	0.35	0.40	0.45	0.013	0.015	0.017
L1	0.31	0.36	0.41	0.012	0.014	0.016

¹² Controlling dimension: millimeter (mm)

LQFP64L (7 x 7 x 1.4 mm / Pitch: 0.4)



Symbols	Dimension in mm ¹³			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.25	0.002	–	0.010
A2	1.35	1.40	1.45	0.053	0.055	0.057
b ¹⁴	0.13	0.19	0.25	0.005	0.007	0.010
c	0.09	–	0.20	0.004	–	0.008
D	9.00 BSC			0.354 BSC		
D1 ¹⁵	7.00 BSC			0.276 BSC		
e	0.40 BSC			0.016 BSC		
E	9.00 BSC			0.354 BSC		
E1 ¹⁵	7.00 BSC			0.276 BSC		
L	0.40	0.60	0.80	0.016	0.024	0.032
L1	1.00 REF			0.039 REF		
θ	0°	3.5°	7°	0°	3.5°	7°

¹³ Controlling dimension: millimeter (mm)
¹⁴ Dimension "b" does not include dambar protrusion.
¹⁵ Dimensions "D1" and "E1" do not include mode protrusions.

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