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AMENDENT HISTORY

Version	Date	Description
Ver 1.0	2011/11/11	First Issue
Ver 1.1	2011/11/21	Modify NAND flash IF function, it is “Read only” mode
Ver 1.2	2011/12/19	a. Modify CS2 mapping address from 8M to 4M bits b. Modify SD-Audio DAC SNR from 90dB to 80dB
Ver 1.3	2012/04/16	a. Update typo at GPIO number at P4 (page 6) b. Adds contents at Electrical Characteristics chapter
Ver 1.4	2012/06/15	a. Adds testing temperature. b. Adds Chap 19 : Reference Schematic
Ver 1.5	2013/11/07	Add Chap 17: Absolute Maximum Rating

1. Introduction

The SNC7001A is a 16-bit DSP processor. It runs at 48MHz with 48MIPS high performance processing speed. Therefore, the SNC7001A is applicable to process voice recognition and picture display related algorithms. The memory includes a 32KW Program RAM and 16KW Working RAM. The 32KW Program RAM supports re-bootable function in order to develop more complex application programs.

Peripherals embedded in the SNC7001A include NAND FLASH with ECC controller (read only), SD/MMC controller, USB device, LCD Interface, UART interface, MSP, SPI master/slave interface, CMOS Image Sensor controller, PWM Output, Audio ADC and DAC, I2S and SAR ADC.

2. Features

- Built-in 16-bit DSP core
- 48 MIPS CPU Performance under 48MHz, 1 Clock per 1 Instruction.
- Clock Type:
  - 48MHz for system clock
  - 32768Hz for system clock
- High Speed Clock Source (pumping from 12MHz → 48MHz by PLL circuit)
  - 12MHz crystal oscillator
  - 12MHz IHRC
- Low Speed Clock Source:
  - 32768Hz crystal oscillator
  - 32768Hz external Rosc
- Operation Mode:
  - Normal mode (hi-speed clock enable)
  - Slow mode 1 (hi-speed clock enable, PLL disable, slow-speed clock disable)
  - Slow mode 2 (hi-speed clock disable, slow-speed clock enable)
  - Watch mode (chip entry power-down mode and wake-up per 0.5/1 sec automatically)
  - Power-down mode (both hi-speed and low-speed clock disable)
- Three 16-bit Timers, 1 Watch Dog Timer, 1 RTC
  - Timers with Individual pre-scalar and auto-reload function
  - Event Counter (Combine Timer and Input Pin P0.0~P0.2)
  - Watch Dog Timer (WDT) with 0.25/0.5/1/2-sec period
  - RTC with 0.5/1-sec period
- Interrupt Sources
  - 1 for ADC, 3 for Timers, 1 for RTC, 1 for SPI, 1 for AD, 1 for DA, 1 for I2S, 1 for MSP
  - 3 for External (P0.0~P0.2), 1 for USB, 1 for NAND Flash, 4 for DMA
- 32K * 16 Internal Program RAM (need boot form external flash storage)
- Total 16K*16 Internal RAM memory configuration for Program and working RAM
  - Mode 0: 8K*16 Program RAM + 8K*16 Working RAM
  - Mode 1: 4K*16 Program RAM + 12K*16 Working RAM
  - Mode 2: 12K*16 Program RAM + 4K*16 Working RAM (default)
  - Mode 3: 16K*16 Working RAM

- Support Barrel Shifter and 16×16 to 32-bit multiplier
- DMA provided (USB/NandFlash/SD/LCD/SPI)
- Built-in ICE Debug Function

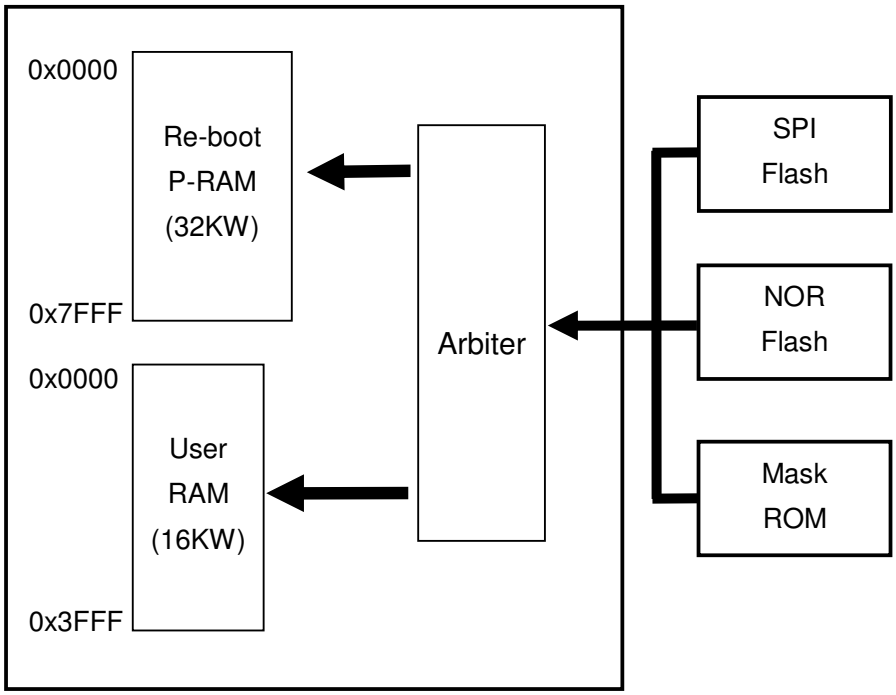
3. Pin Assignments

Symbol	Descriptions	No. of Pin	Pin Count
VDDA_LDO	Power for Regulator	1	1
VDDAL_LDO	Regulator voltage output	1	2
VSSA_LDO	Regulator Ground	1	3
VDD	Power + for core	5	8
VSS	Power - for core	5	13
VDDDP	Power for IO	6	19
VSSDP	GND for IO	7	26
VDD_DAC	Power for Audio DAC	2	28
VSS_DAC	GND for Audio DAC	2	30
VCOM	Audio DAC Common mode output	1	31
DAC_VMID	Audio DAC VMID output	1	32
VDDA_DRV	Audio DAC Driver Power	2	34
VSSA_DRV	Audio DAC Driver GND	2	36
VOUTP	Audio DAC output (+)	1	37
VOUTN	Audio DAC output (-)	1	38
ADC_VMID	SD ADC VMID output	1	39
MICBIAS	SD ADC Microphone Bias Voltage output	1	40
FMIN	SD ADC FM signal input pin	1	41
AUX	SD ADC AUX signal input pin	1	42
VDDA_ADC	Power for SD ADC	2	44
VSSA_ADC	GND for SD ADC	2	46
MIC_N	SD ADC MIC difference input (-)	1	47
MIC_S	SD ADC MIC single input	1	48
MIC_P	SD ADC MIC difference input (+)	1	49
VDDA_SAR	Power for SAR ADC	2	51
VSSA_SAR	GND for SAR ADC	2	53
AVREFH	Reference Voltage for SAR ADC	1	54
AIN[3:0]	SAR ADC Anlong input pin	4	59
VO1	Thermal DAC Output	1	60
XIN_12M	High speed clock crystal input	1	61
XOUT_12M	High speed clock crystal output	1	62
XIN_32K	Low speed clock crystal input	1	63
XOUT_32K	Low speed clock crystal output	1	64
CKSEL	Crystal/RC-type oscillator select for high speed clock	1	65
RSTB	Chip reset	1	66
TEST	For test only	1	67
PHY_DM	USB Data +	1	68
PHY_DP	USB Data -	1	69
VDDA_PHY	USB power + (3.3V)	2	71

VDDAL_PHY	USB power + (1.8V)	2	73
VSSA_PHY	USB power -	2	75
P0.0~P0.15	General I/O port P0.0~P0.15	16	91
P1.0~P1.15	General I/O port P1.0~P1.15	16	107
P2.0~P2.15	General I/O port P2.0~P2.15	16	123
P3.0~P3.15	General I/O port P3.0~P3.15	16	139
P4.0~P4.11	General I/O port P4.0~P4.11	12	151
ICE	ICE Interface	5	156
CODE_SEL	Standalone Boot Path Select	1	157

4. Memory

There are 32KW Program Boot RAM and 16KW User RAM in SNC7001A. It boots program code into Program Boot RAM from an external storage device and then begins to run at program address 0x0000. The SNC7001A has 16KW RAM which has four modes of configuration (Mode 0~Mode 3) to select the Program RAM and Working RAM size for different application.



4.1 Internal Re-boot Program RAM

There is 32KW of SNC7001A boot program RAM. User built-in his own program and SNC7001A algorithm library in the boot program RAM for his application. After reset, it will boot user's code into internal 32KW P-RAM from external storage (SPI Flash, NOR Flash or Mask ROM) automatically. During operation mode, user can also reload other code into the internal P-RAM at address 0x0800 ~ 0x7FFF. This area can be thought of as (warm) "Re-boot area". If the user wants to execute a (cold) Re-boot action, the DSP program counter MUST be set to 0x0000 ~ 0x07FF area until the true Re-boot action is finished.

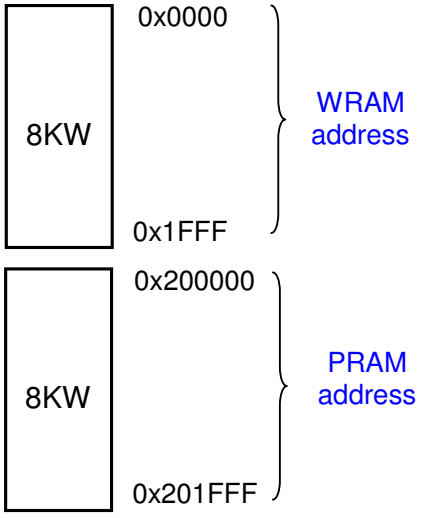
Address Range	Size (word)	Usage	DSP	DMA
0x000000 ~ 0x0007FF	2K	Program RAM	R	--
0x000800 ~ 0x007FFF	30K	Program RAM	R	R/W

4.2 Internal User RAM

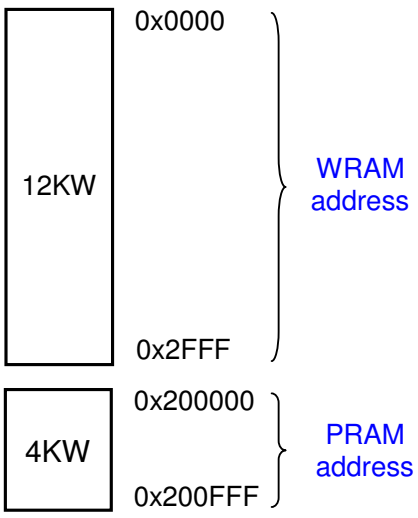
Total 16K*16 Internal RAM memory configuration for Program and Working RAM

- Mode 0: 8K*16 Program RAM + 8K*16 Working RAM
- Mode 1: 4K*16 Program RAM + 12K*16 Working RAM
- Mode 2: 12K*16 Program RAM + 4K*16 Working RAM (default)
- Mode 3: 16K*16 Working RAM

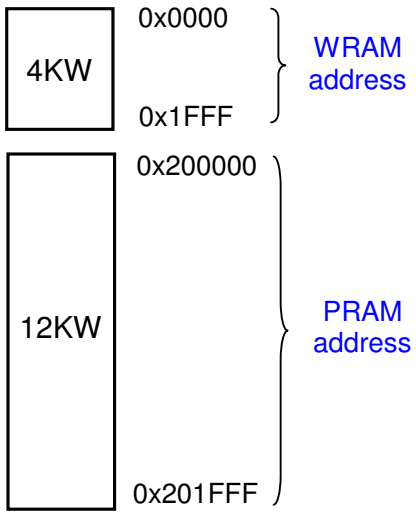
Mode 0



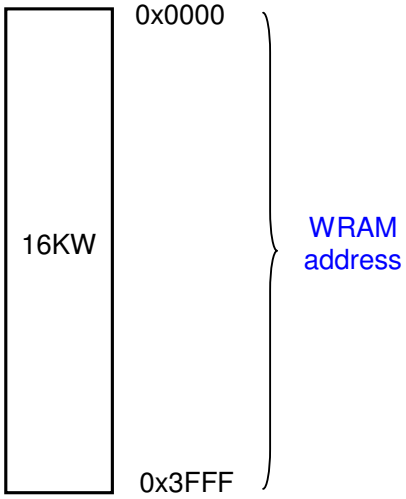
Mode 1



Mode 2



Mode 3



4.3 External Program Memory

Address Range	Size (word)	Usage	DSP	DMA
0x400000 ~ 0xBFFFFF	8M	CS1 SPI Flash /CS1 NOR Flash	R	R/W
0xC00000~ 0xFFFFFF	4M	CS2 NOR Flash	R	R/W

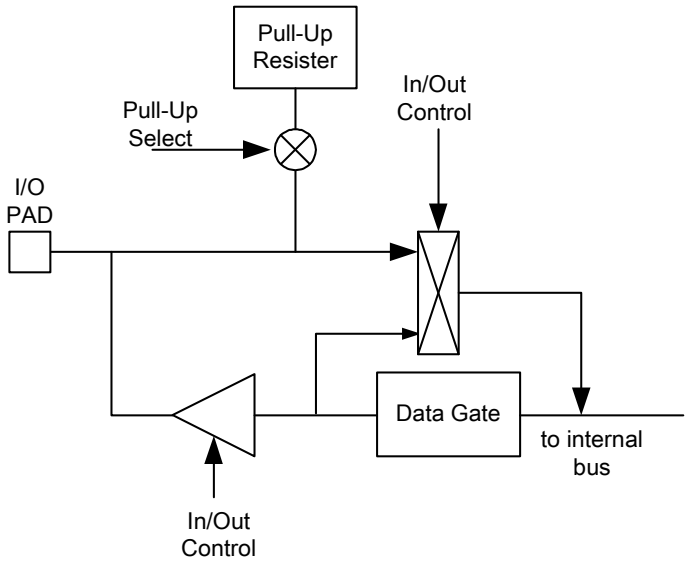
5. System Clock

SNC7001A is a dual clock system that provides high-speed clock (12MHz crystal up to 48MHz) and low-speed clock (12MHz or 32768Hz). The SNC7001A uses an internal PLL to up sample clock speed to 48MHz.

6. I/O Port

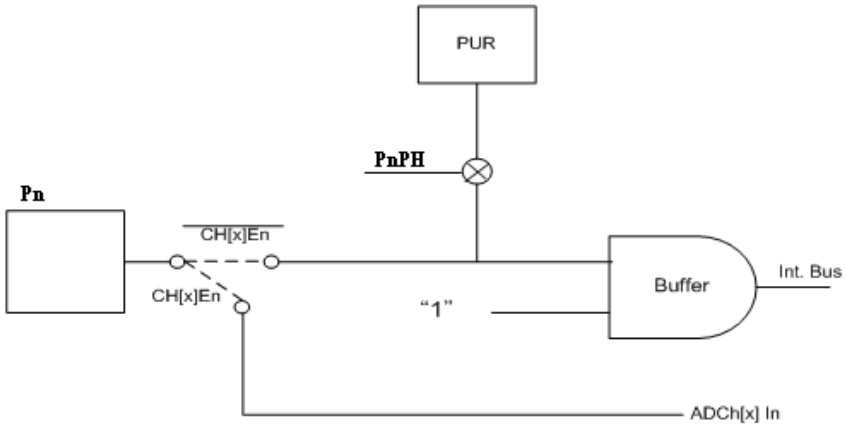
SNC7001A provides a total of 76 I/O pins (P0.0~P4.11) and 4 inputs pins (P4.12~P4.15, which shares with SAR ADC pins). The input pull-high resistor of each pin can be individually programmed by port pull-high register and the direction of I/O port is selected by port direction register. The I/O port P0.0~P0.15 and P1.0~P1.15 can wake up the chip from the standby mode.

These 76 programmable I/O pins and 4 input pins provide not only a simply input/output function but also can configure to be chip select pins of extension bus and multi-function peripheral interfaces. For details please refer to the following sections. Analog input pins (AIN0~AIN3) of SAR ADC can be selected to act as digital input only, please refer Figure-2. The internal structure of I/O pins is showed in Figure-1.



I/O Configuration of Port0.0 ~ Port4.11

Figure-1



Configuration of Port4.12 ~ Port4.15

Figure-2

7. Timer/Counter

SNC7001A provides three 16-bit timer/event counters (T0/T1/T2). Each timer is 16-bit binary up-count timer with pre-scalar and auto-reload function.

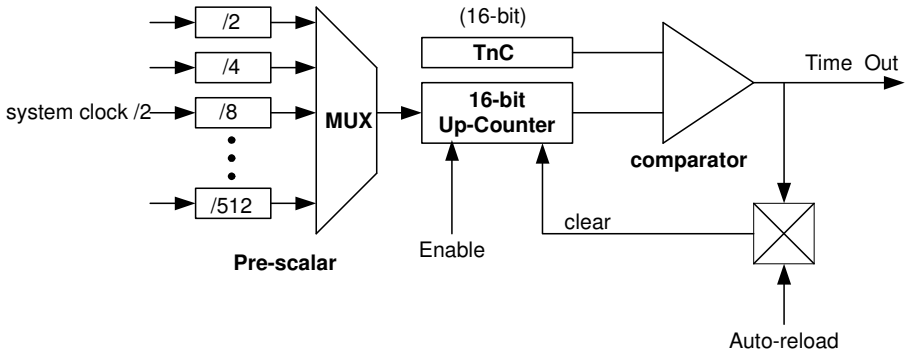


Figure-3

8. Interrupt

At the moment when SNC7001A enters the interrupt service routine, the GIE bit (in INTEN) will be cleared to "0“ for blanking other interrupts. However, during this stage, other enabled interrupt sources still can issue their requests but the requests are queued in INTRQ. GIE will be restored to “1” while DSP exits ISR. Then the other valid interrupt can be granted and served immediately.

Interrupt Vector	Priority	Entry Location	Descriptions
Reset	x	0x000000	Reset
reserved	0	0x000010	
AD	4	0x000014	AD FIFO full
T0	5	0x000018	T0 overflow
P0.0 (UART RxD)	6	0x00001C	Falling/Raising edge of P0.0
T1	7	0x000020	T1 overflow
P0.1 (UART TxD)	8	0x000024	Falling/Raising edge of P0.1
T2	9	0x000028	T2 overflow
P0.2	10	0x00002C	Falling/Raising edge of P0.2
reserved	9	0x000030	
DA	11	0x000034	DA FIFO empty
SPI	3	0x000038	SPI Interrupt
MSP(I2C)	2	0x00003C	MSP Interrupt
I2S	1	0x000040	I2S Interrupt
reserved		0x000044	
reserved		0x000048	
reserved		0x00004C	
USB	12	0x000050	USB Interrupt
CIS_HREF	13	0x000054	CIS HREF Interrupt
RTC	14	0x000058	RTC overflow
NF	15	0x00005C	NF Interrupt
DMA_CIS_W	16	0x000060	DMA_CIS_W Interrupt
DMA_NF_RW	17	0x000064	DMA_NF_R & DMA_NF_W Interrupt
SAR_AD	18	0x000068	SAR ADC interrupt
reserved	19	0x00006C	
reserved	20	0x000070	
reserved	21	0x000074	
DMA_DEV_RW	22	0x000078	DMA_DEV_R & DMA_DEV_W nterrupt

9. External Storage Devices

9.1 Extension Bus

SNC7001A contains a built-in standard 8080 micro-controller interface to extend the memory capability through an extension bus. In addition, the SNC7001A provides a word mode access bus for external memory devices in order to improve efficiency.

The extension bus also allows users to connect different external devices for various applications, such as ROM, RAM, LCM, NOR flash etc.

The SNC7001A can connect to up to two different devices with two available chip select pins. The maximum addressing capability of CS1 is 128M bits and CS2 is 64M bits. User can put his program into each external memory device.

9.2 SPI Flash Controller

SNC7001A has a built-in SPI Flash controller interface to support 1/2/4 bit read/write mode, it can run 6/12/24/48 MHz clock frequency. In additional, SNC7001A can run programs from SPI Flash (at a much reduced rate).

9.3 NAND Flash / SD Card Interface

The flash memory (Mass-storage) interface provides an interface between Mass storage and SNC7001A DSP core. It supports 2 types of storage memory: NAND Flash (**read only**) and SD Card.

- NAND Flash Controller just support read only function, and compatible Xtra-ROM interface.
- SD Card Controller support SD Card1.0/2.0 commands (SDSC/SDHC)

10. Audio CODEC

10.1 ADC

In SNC7001A, we provide one set of high performance one channel Analog-to-Digital Converter (ADC) for microphone applications with typical SNR at 90dB. This Analog-to-Digital Converter has a built-in PGA (-12dB ~ +33dB), BOOST (0 ~ +30dB) and true AGC control. It supports 8/12/16/22.05/24/32/44.1/48KHz sample rates.

10.2 Audio DAC

In SNC7001A, we provide 2 types DAC outputs for different applications. One is a 16-bit DAC + Class AB embedded, and its typical SNR is 80dB. It can drive L/R channel Earphone. The other one is thermal DAC, and its typical SNR is 65dB. A 16x16 FIFO is used to prevent the sound glitch when CPU is busy. They all support 8/12/16/ 22.05/24/32/44.1/48KHz sample rates.

11. 10-bit SAR ADC

SNC7001A has a built-in SAR ADC, which has 4-input sources with up to 1024-step resolution to transfer analog signal into 10-bits digital data. The sequence of ADC operation is to select input source (AIN0 ~ AIN3) first, then set CHS and START bit to “1” to start conversion. When the conversion is complete, the ADC circuit will set START bit to “0” and final value output will reside in the ADR register. In SNC7001A, we provide an interrupt to inform user program that the ADC result is ready. However, the interrupt event is optional.

12. CMOS Image Sensor (CIS)

The CIS Interface communication is based on an advanced 12-pin interface - CIS Clock, VSYNC, HREF, Pixel Clock and eight Data Lines. Frequency of CIS Clock which output to CIS module can be chosen among 24MHz and 12MHz. VSYNC, HSYNC and Pixel Clock signals from the CIS Module can be set up for active timing at rising or falling edges. An interrupt flag will be issued after a line of data is transmitted to Working RAM which informs the system to access data that is stored at Working RAM.

- Support VGA/ CIF/ QVGA/ QCIF/ QQVGA resolution
- Support CMOS Image Sensor output 16bits RGB565/YUVand 8-bit RGB data formats
- Support Window Setting and Scaling

13. LCD Interface

The SNC7001A has a built-in LCD controller interface which supports up-to 320*240 LCD Panel and 1/4 bit data bus for monochrome/gray-scale LCD.

14. Communication Interface

14.1 USB Interface

The SNC7001A provides a USB 2.0 High Speed (480MHz) interface (includes 4 endpoint); user can download/upload data from/to PC through this USB interface. It supports control transfer, interrupt transfer and bulk transfer. SNC7001 provides twin 512byte buffers for bulk in/out transition, one 64byte buffer for control transition and one 16byte buffer for interrupt transition.

EP0: Control transfer
EP1: bulk-in (mass-storage, DSP→PC)
EP2: bulk-out (mass-storage, PC→DSP)
EP3: interrupt-in (HID, DSP→PC)

14.2 UART Interface

Users can download data from PC through this UART interface. The standard UART interface provides the below baud rates:
1200/2400/4800/9600/19200/38400/51200/57600/102400/115200 bps

14.3 I2S Interface

Built-in an I2S output that supports digital audio data to external audio DAC. Two L/R channel 16x16 FIFO is used to prevent sound glitches when the CPU is busy.

14.4 MSP Interface

The MSP (Main Serial Port) is a serial communication interface for data exchanging from one MCU to another MCU or other hardware peripherals. These peripheral devices may be serial EEPROM, A/D converters, Display device, etc. The MSP module can operate in one of two modes

- Full Master Mode
- Slave Mode (with general address call)

14.5 SPI Interface

The SPI (serial peripheral interface) is a synchronous serial bus that provides good support for communication with SPI-compatible peripheral devices. The SPI peripheral is a synchronous, 7-wire interface consisting of two data pins (SPITxD and SPIRxD); two additional pins (SPIED3 and SPIED2) for 4-bit mode access, two slave select pins (/SS1, /SS2); and a synchronous clock pin (SCLK). The two data pins permit full-duplex and half-duplex operation to other SPI-compatible devices. The SPI also includes programmable baud rates, clock phase (CPHA), and clock polarity (CPOL).

15. Multi function of I/O

PORT0	P0.0	INT	INT0						
	P0.1		INT0						
	P0.2		INT0						
	P0.3	PWM	PWMIO#0						
	P0.4		PWMIO#1						
	P0.5		PWMIO#2						
	P0.6		PWMIO#3						
	P0.7	Comm SPI	SPISCK						
	P0.8		SPIMISO						
	P0.9		SPIMOSI						
	P0.10		SPICS#1						
	P0.11		SPID2	I2S	WS				
	P0.12		SPID3		SCL				
	P0.13		SPICS#2		SD				
	P0.14				MCLK				
	P0.15	IR	IR_Out						
PORT1	P1.0	Program SPI	CS	E-Bus (CS1/CS2)	ECS1				
	P1.1		SCK		EA2				
	P1.2		MISO		EA3				
	P1.3		MOSI		EA4				
	P1.4		ED2		EA5				
	P1.5		ED3		EA6				
	P1.6				EA7				
	P1.7				EA8				
	P1.8				EA9				
	P1.9				EA10				
	P1.10				EA11				
	P1.11				ECS2				
	P1.12				EWR\				
	P1.13				ERD\				
	P1.14				EA0				
	P1.15				EA1				
PORT2	P2.0				ED0				
	P2.1				ED1				
	P2.2				ED2				
	P2.3				ED3				

	P2.4				ED4				
	P2.5				ED5				
	P2.6				ED6				
	P2.7				ED7				
	P2.8				ED8 (note1)				
	P2.9				ED9				
	P2.10				ED10				
	P2.11				ED11				
	P2.12				ED12				
	P2.13				ED13				
	P2.14				ED14				
	P2.15				ED15				
PORT3	P3.0				EA12				
	P3.1				EA13				
	P3.2				EA14				
	P3.3				EA15				
	P3.4				EA16				
	P3.5				EA17				
	P3.6				EA18				
	P3.7				EA19				
	P3.8				EA20				
	P3.9				EA21				
	P3.10				EA22				
	P3.11			NAND	NFCS				
	P3.12				R/B				
	P3.13				NFALE				
	P3.14				NFWE			CIS	VSYNC
	P3.15				NFRE				HSYNC
PORT4	P4.0				NFWP		SDCLK		MCLK
	P4.1				NFCLE		SDCMD		PCLK
	P4.2	LCDC	LCD0		NFD0	SD	SDD0		CISD0
	P4.3		LCD1		NFD1		SDD1		CISD1
	P4.4		LCD2		NFD2		SDD2		CISD2
	P4.5		LCD3		NFD3		SDD3		CISD3
	P4.6		LCDA		NFD4				CISD4
	P4.7		LCDCK		NFD5				CISD5
	P4.8		LCDLP		NFD6				CISD6

	P4.9		LCDFP		NFD7				CISD7
	P4.10	UART	TxD	MSP	CLK				
	P4.11		RxD		DAT				
	P4.12	SAR ADC	AIN0 (note2)						
	P4.13		AIN1						
	P4.14		AIN2						
	P4.15		AIN3						

Note1: P2.8~P2.15 (GPIO) are shared pin with 8080 IF high byte (ED8~ED15)

Note2: P4.12~P4.15 (input only) are shared pin with “SAR ADC” AIN0~AIN3.

16. Regulator

The SNC7001 built-in a linear regulator for core power (CVDD) apply. The accuracy output voltage is 1.8V±0.18V and it can be power downed by software.

17. Absolute Maximum Rating .

Items	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	-0.3	6.0	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}-0.3	V
Operating Temperature	T_{OP}	0	55.0	℃
Storage Temperature	T_{STG}	-55.0	125.0	℃

18. Electrical Characteristics

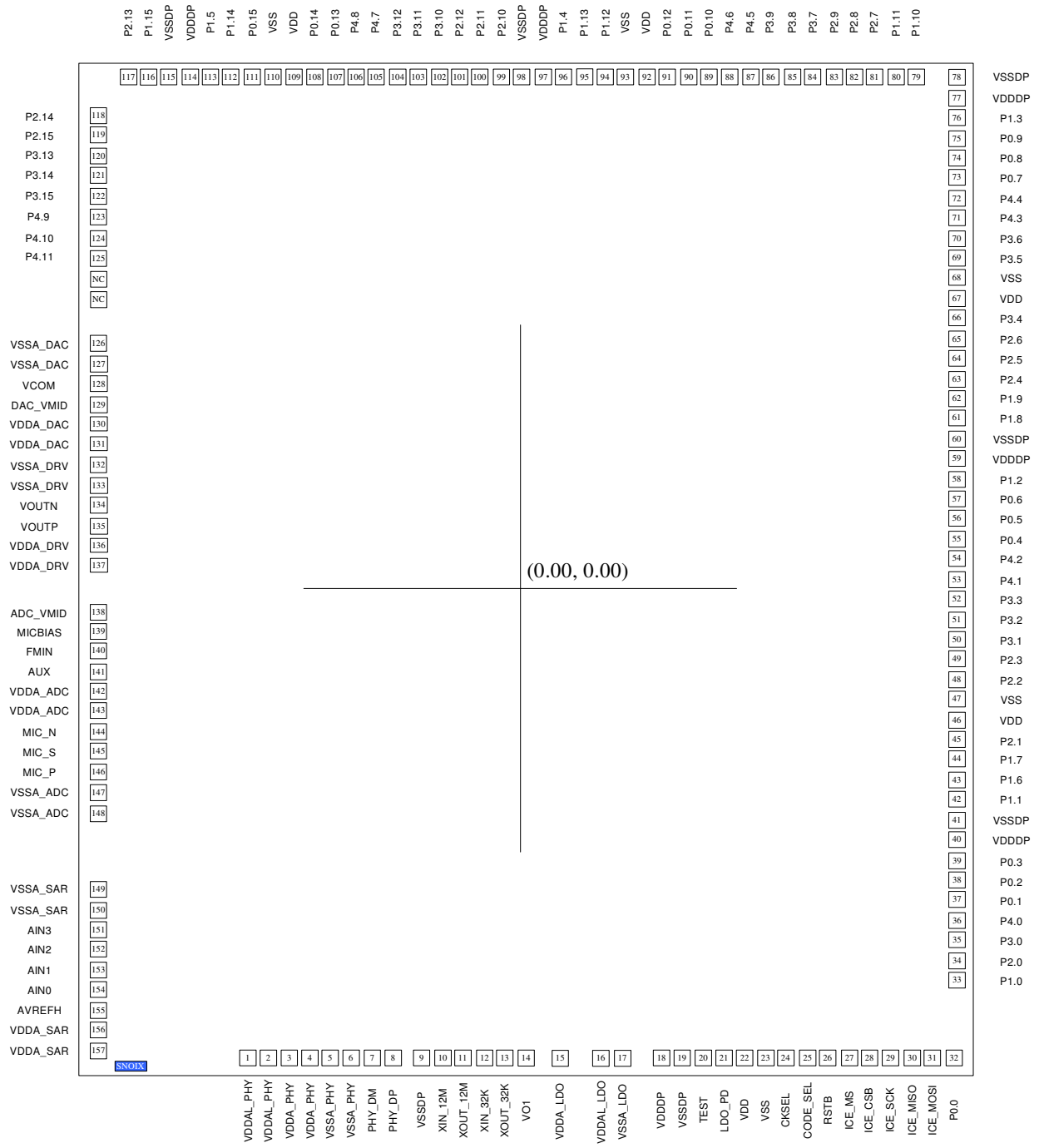
Item	Sym.	Min.	Typ.	Max.	Unit	Condition (TA=25 ℃)
Operating Voltage VDD	V_{DD}	2.7	3.3	3.6	V	
Operating Voltage CVDD	CV_{DD}	1.62	1.8	1.98	V	
Standby current	I_{SBY}	-	30	60	uA	V_{DD}=3.3V,No load
SAR ADC ENOB	ENOB		9		bit	
SAR ADC INL	INL		1		bit	
SAR ADC DNL	DNL		1		bit	
SD-ADC SNR	SNR		90		dB	
SD-DAC SNR	SNR		80		dB	
Drive current of P0,	I_{OD}	-	4	-	mA	V_O=2.4V

P1.6~P1.15, P2, P3, P4.0~P4.11						
Sink current of P0, P1.0, P1.6~P1.15, P2, P3, P4.0~P4.11	I_{OS}	-	4	-	mA	V_O=0.4V
Drive current of P1.1~P1.5	I_{OD}		16		mA	V_O=2.4V (note1)
Sink Current of P1.1~P1.5	I_{OS}		16		mA	V_O=0.4V (note1)
Sink Current of P4.12~P4.15	I_{OS}	-	4	-	mA	V_O=0.4V (note2)

Note1: P1.1~P1.5 own two option for drive / sink current (16 or 12mA), the default is 16mA

Note2: P4.12~P4.15 (input only) are shared pin with “SAR ADC” AIN0~AIN3.

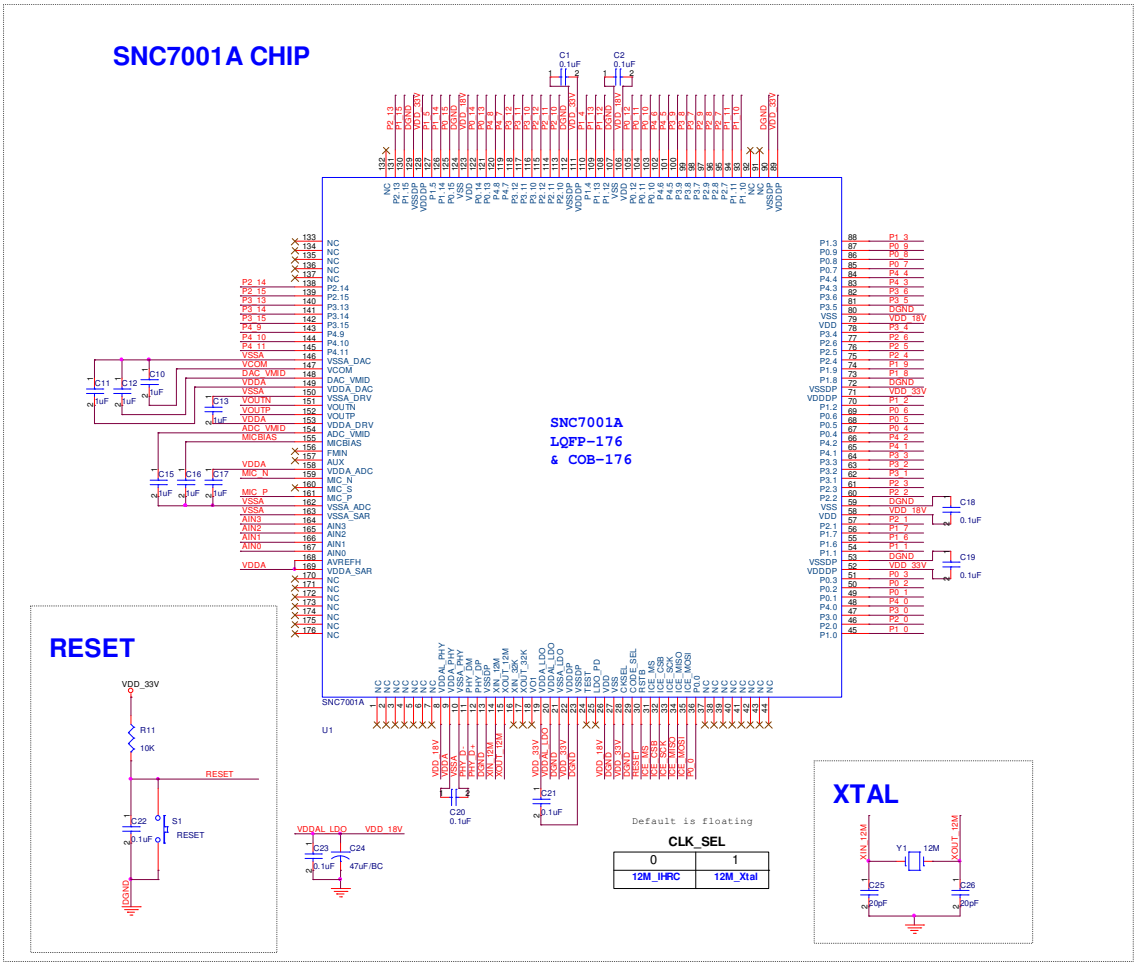
19. Bonding Information

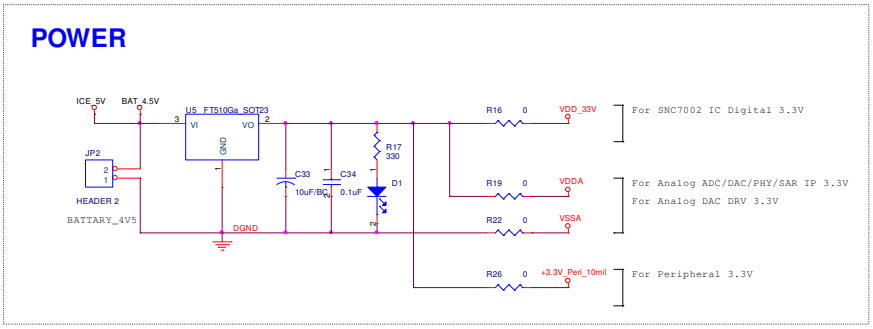


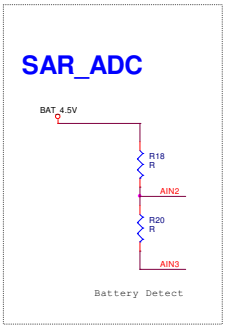
SNC7001A

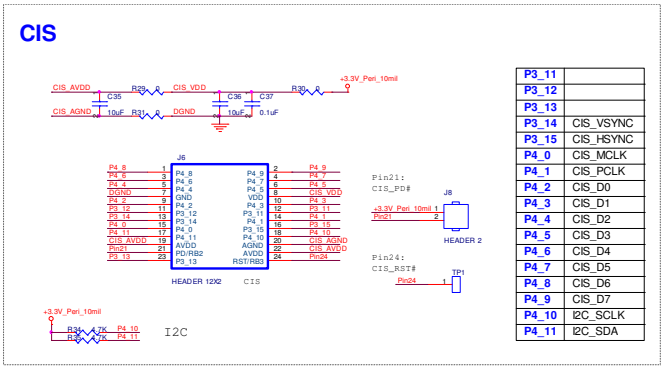
Note: The substrate MUST be connected to GND in PCB layout

20. Reference Schematic

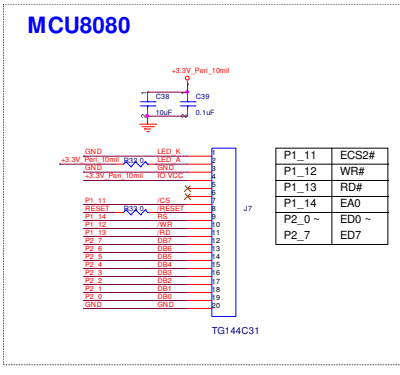






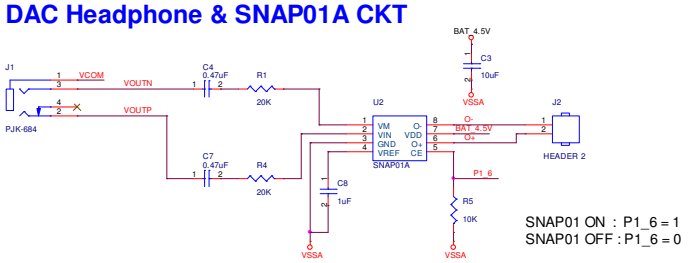


P3_11	
P3_12	
P3_13	
P3_14	CIS_VSYNC
P3_15	CIS_HSYNC
P4_0	CIS_MCLK
P4_1	CIS_PCLK
P4_2	CIS_D0
P4_3	CIS_D1
P4_4	CIS_D2
P4_5	CIS_D3
P4_6	CIS_D4
P4_7	CIS_D5
P4_8	CIS_D6
P4_9	CIS_D7
P4_10	I2C_SCLK
P4_11	I2C_SDA

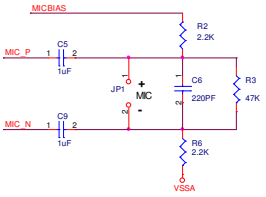


P1_11	ECS2#
P1_12	WR#
P1_13	RD#
P1_14	EA0
P2_0 ~	ED0 ~
P2_7	ED7

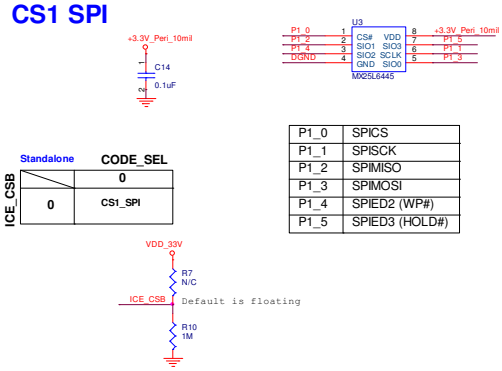
DAC Headphone & SNAP01A CKT



MIC & LINE_IN CKT

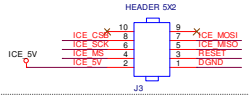


CS1 SPI



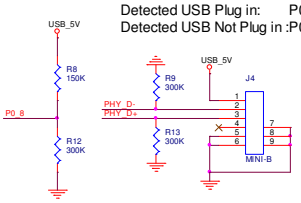
P1_0	SPICS
P1_1	SPISCK
P1_2	SPIMISO
P1_3	SPIMOSI
P1_4	SPIED2 (WP#)
P1_5	SPIED3 (HOLD#)

ICE Interface

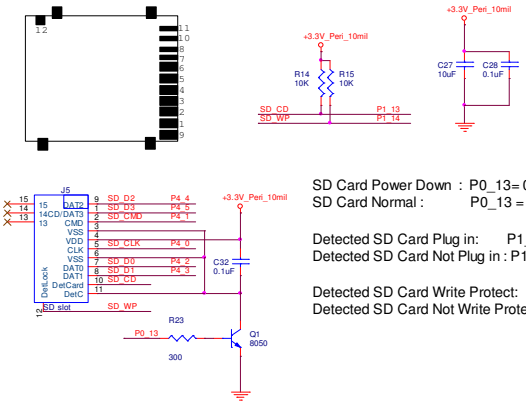


USB

Detected USB Plug in: P0_8=1
Detected USB Not Plug in :P0_8=0



SD CARD

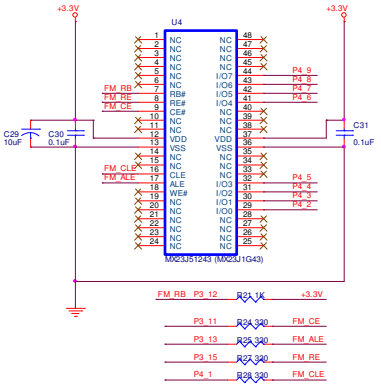


SD Card Power Down : P0_13= 0
SD Card Normal : P0_13 = 1

Detected SD Card Plug in: P1_13= 0
Detected SD Card Not Plug in : P1_13= 1

Detected SD Card Write Protect: P1_14= 0
Detected SD Card Not Write Protect :P1_14= 1

X-ROM IF



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