SN32F600 Series
USB Type-C Port Controller

1 Introduction

1.1 Features

- Memory configuration
  – 32 KB on-chip flash programming memory
  – 4 KB SRAM
- ARM® Cortex®-M0 with F_{CPU} up to 48 MHz
- Serial Wire Debug (SWD) interface
- Programmable Watchdog Timer (WDT)
- 24-bit System Tick (SysTick) timer
- Interrupt sources implemented by Nested Vectored Interrupt Controller (NVIC) including LVD, BMC, DPDMQC, ADC, OVP, UVP, SCP, OCP, OTP, CT16B0, CT16B1, and WDT
- 5V I/O pin configuration
  – Bi-directional
  – Wakeup I/Os
  – Pull-up resisters
  – 10 mA source and sink current
- High voltage I/O pin configuration
  – Gate driver control I/O for external MOS: VBUS_CTRL
  – Sink currents for discharge and monitor: DISC_MON
  – Cathode I/O for shunt regulator: CATH
- Type-C and USB-PD support
  – USB PD3.0 Version 1.2 specification including Programmable Power Supply (PPS) mode
  – Configurable resistors R_P and R_D
  – One USB Type-C port and one Type-A port
- Quick Charge™ (QC) protocol
  – Supports one set of DPDM QC I/Os and integrates all required terminations on DP/DM lines
  – Supports BC1.2, QC 2.0/3.0/4.0/4.0+
- Shunt regulator
  – Analog regulation of secondary side feedback node (optocoupler)
  – For VBUS control with step 20 mV, 14.6 mV or 10 mV ranging from 3V to 24.5V output
  – Constant current or constant voltage mode
  – Supports low-side current sensing for constant current feedback for the optocoupler
- Operating voltage and temperature
  – 3.0V to 24.5V operation from VCC with 30V tolerance
  – Working temperature range: -40°C to 105°C
- Internal 5V regulator output
  – Power input from VCC
  – Driving current 20 mA output with external 1 µF capacitor
- Low-side Current Sense Amplifier (LSCSA)
  – Programmable gain control: 20, 40, 60, 80, and 100
  – Built-in offset cancellation
- Built-in 12-bit SAR ADC with 4-level internal reference
  – Up to five channels of ADC input
  – Internal reference voltage: 2V, 3V, 4.5V, and VDD
- Two 16-bit timers: CT16B0 and CT16B1 with 16-bit timer counter, PWM, and CAP
- 2.6V LVD for VDD
- System clocks
  – Internal high clock: RC type 48 MHz
  – Internal low clock: RC type 16 KHz
- Three operating modes
  – Normal mode: Both high and low clocks are active
  – Sleep mode: Wakeup by interrupts
  – Deep sleep mode: Wakes up by I/O, DPDM QC, and CC-PHY
- Packages
  – SOP14L
  – TSSOP24L
  – QFN32L
- Certification
  – USB IF TID: 1298
  – Qualcomm® Quick Charge: QC2019092495

1.2 Description

The SN32F600 Series is a highly integrated USB Type-C port controller that complies with the latest USB Type-C and Power Delivery (PD) standards. With Sonix's proprietary M0 technology, the SN32F600 Series consists of a 32-bit ARM Cortex-M0 processor, a 32KB on-chip flash program memory, a complete Type-C USB-PD transceiver, an integrated feedback control circuit for voltage (VBUS) regulation, and all termination resistors required for a Type-C port. Featuring multiple I/Os, well-integrated BOM, and system-level ESD protection, the SN32F600 Series is well-suited for power adapter applications.

1.3 Selection Table[1]

Name	Flash ROM	RAM	BMC PHY	DPDM QC IO	Shunt LDO	LSCSA	ADC	Timer	IO	Operating Voltage	Package
SN32F601E	32 KB	4 KB	✓	✓	✓	✓	✓	3	0	3–24.5V	SOP14
SN32F602K	32 KB	4 KB	✓	✓	✓	✓	✓	3	6	3–24.5V	TSSOP24
SN32F603M	32 KB	4 KB	✓	✓	✓	✓	✓	3	10	3–24.5V	QFN32

1.4 Functional Block Diagram

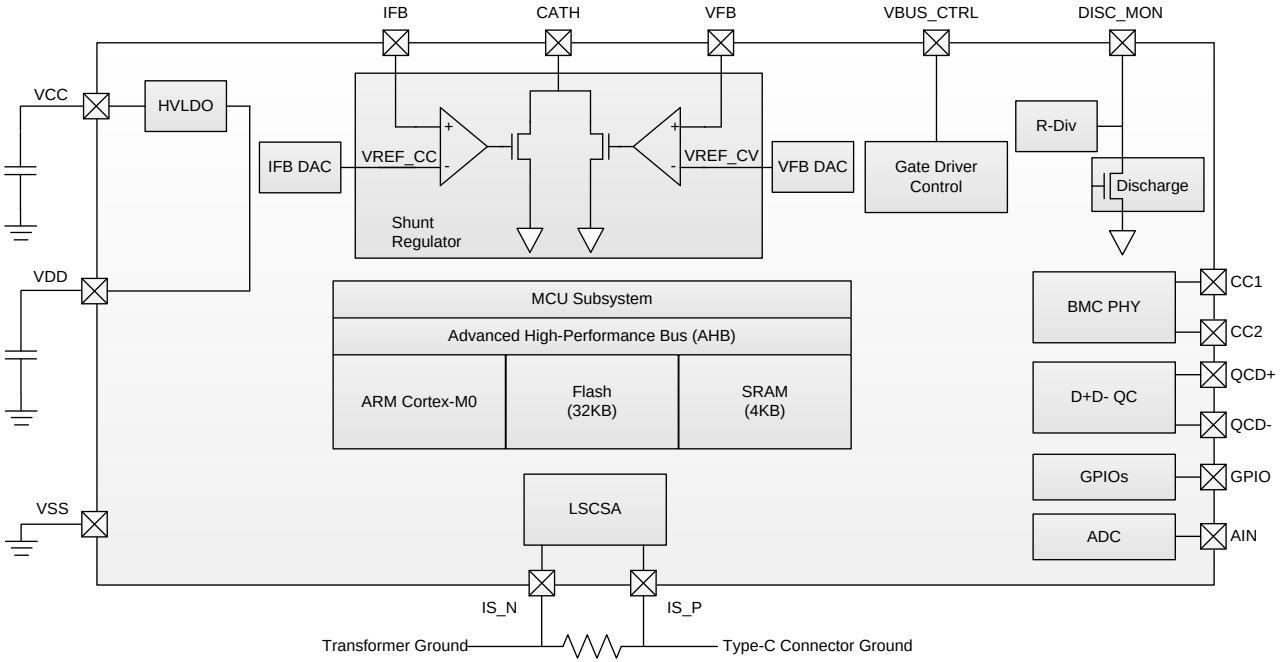

Figure 1–1 Functional Block Diagram

[1] All models of the SN32F600 Series support SCP/OCP/OVP/UVP/OTP protection.

Revision History

Date	Revision	Description
06-Nov-2019	Version 1.0	Official release

Convention

ⓘ **WARNING**	Indicates a hazard with a medium or low level of risk that, if not avoided, could result in minor or moderate injury.
🛠 **TIP**	Indicates a tip that may help you solve a problem or save time.
🕮 **NOTE**	Provides additional information to emphasize or supplement important points of the main text.

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2 Pin Assignment

The SN32F600 Series are available in three package types, SOP14L, TSSOP24L, and QFN32L. Refer to the subsections below for detailed pin assignment and pin descriptions of each package.

2.1 SN32F601E

2.1.1 Pin Assignment

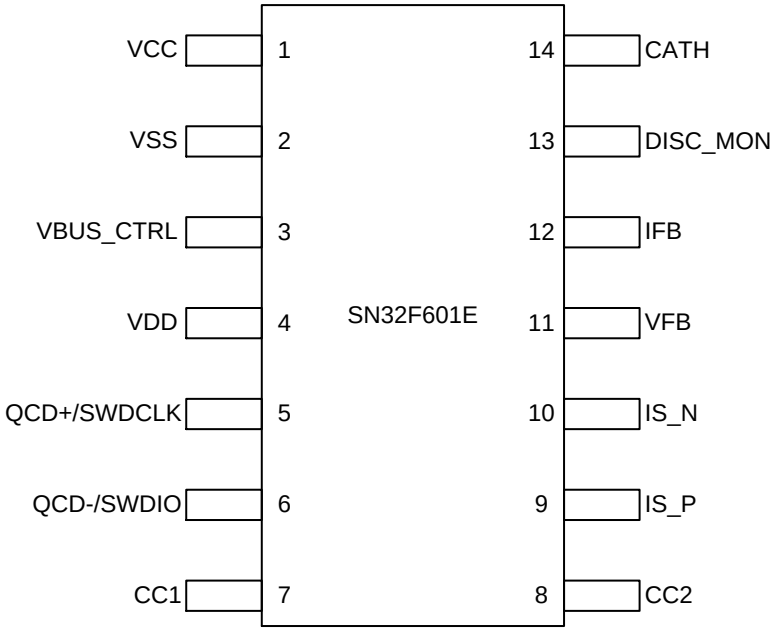


Figure 2–1 SN32F601E Pin Assignment

2.1.2 Pin Description

Table 2–1 SN32F601E Pin Description

Name	Pin No.	Type[2]	Description
VCC	1	P	Power supply input voltage
VSS	2	GND	Power supply ground
VBUS_CTRL	3	I/O	External MOSFET control
VDD	4	P	HV LDO output for digital and analog circuit
QCD+	5	I/O	USB D+ channel
SWDCLK			SWD serial wire clock
QCD-	6	I/O	USB D- channel
SWDIO			SWD serial wire debug input/output
CC1	7	I/O	Type-C connector configuration channel 1
CC2	8	I/O	Type-C connector configuration channel 2
IS_P	9	AI	Positive input of a current sense amplifier for output current sensing
IS_N	10	AI	Negative input of a current sense amplifier for output current sensing
VFB	11	AI	Feedback input for the constant-voltage loop
IFB	12	AI	Feedback input for the constant-current loop
DISC_MON	13	AO	Type-C VBUS monitor with internal discharge FET
CATH	14	AI	Cathode of voltage regulation and compensation for other applications

[2] Signal Types:
I = Input
O = Output
A = Analog signal
P = Power
GND = Ground

2.2 SN32F602K

2.2.1 Pin Assignment

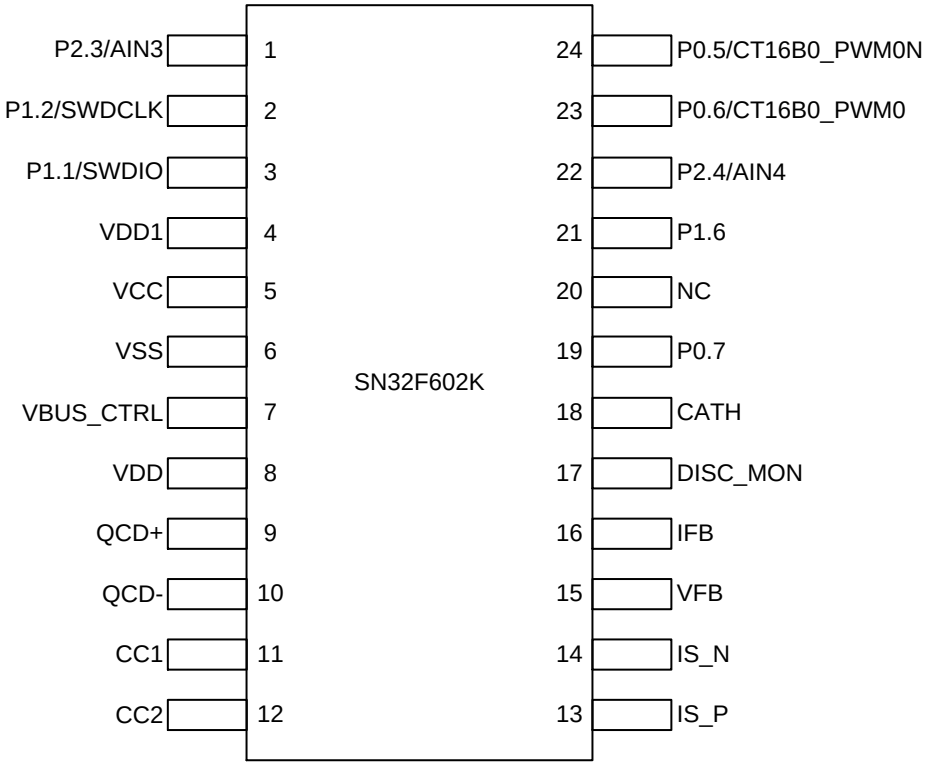


Figure 2–2 SN32F602K Pin Assignment

2.2.2 Pin Description

Table 2–2 SN32F602K Pin Description

Name	Pin No.	Type[2]	Description
P2.3	1	I/O	General purpose digital input/output pin
AIN3		AI	ADC channel input 3
P1.2	2	I/O	General purpose digital input/output pin
SWDCLK			SWD serial wire clock
P1.1	3	I/O	General purpose digital input/output pin
SWDIO			SWD serial wire debug input/output
VDD1	4	P	Power supply input voltage for digital circuit
VCC	5	P	Power supply input voltage
VSS	6	GND	Power supply ground
VBUS_CTRL	7	I/O	External MOSFET control
VDD	8	P	HV LDO output for digital and analog circuit
QCD+	9	I/O	USB D+ channel
QCD-	10	I/O	USB D- channel
CC1	11	I/O	Type-C connector configuration channel 1
CC2	12	I/O	Type-C connector configuration channel 2
IS_P	13	AI	Positive input of a current sense amplifier for output current sensing
IS_N	14	AI	Negative input of a current sense amplifier for output current sensing
VFB	15	AI	Feedback input for the constant-voltage loop
IFB	16	AI	Feedback input for the constant-current loop
DISC_MON	17	AO	Type-C VBUS monitor with internal discharge FET
CATH	18	AI	Cathode of voltage regulation and compensation for other applications
P0.7	19	I/O	General purpose digital input/output pin
NC	20	–	No connection should be made to this pin
P1.6	21	I/O	General purpose digital input/output pin
P2.4	22	I/O	General purpose digital input/output pin
AIN4		AI	ADC channel input 4
P0.6	23	I/O	General purpose digital input/output pin
CT16B0_PWM0			PWM output 0 for CT16B0
P0.5	24	I/O	General purpose digital input/output pin
CT16B0_PWM0N			Negative PWM output 0 for CT16B0

2.3 SN32F603M

2.3.1 Pin Assignment

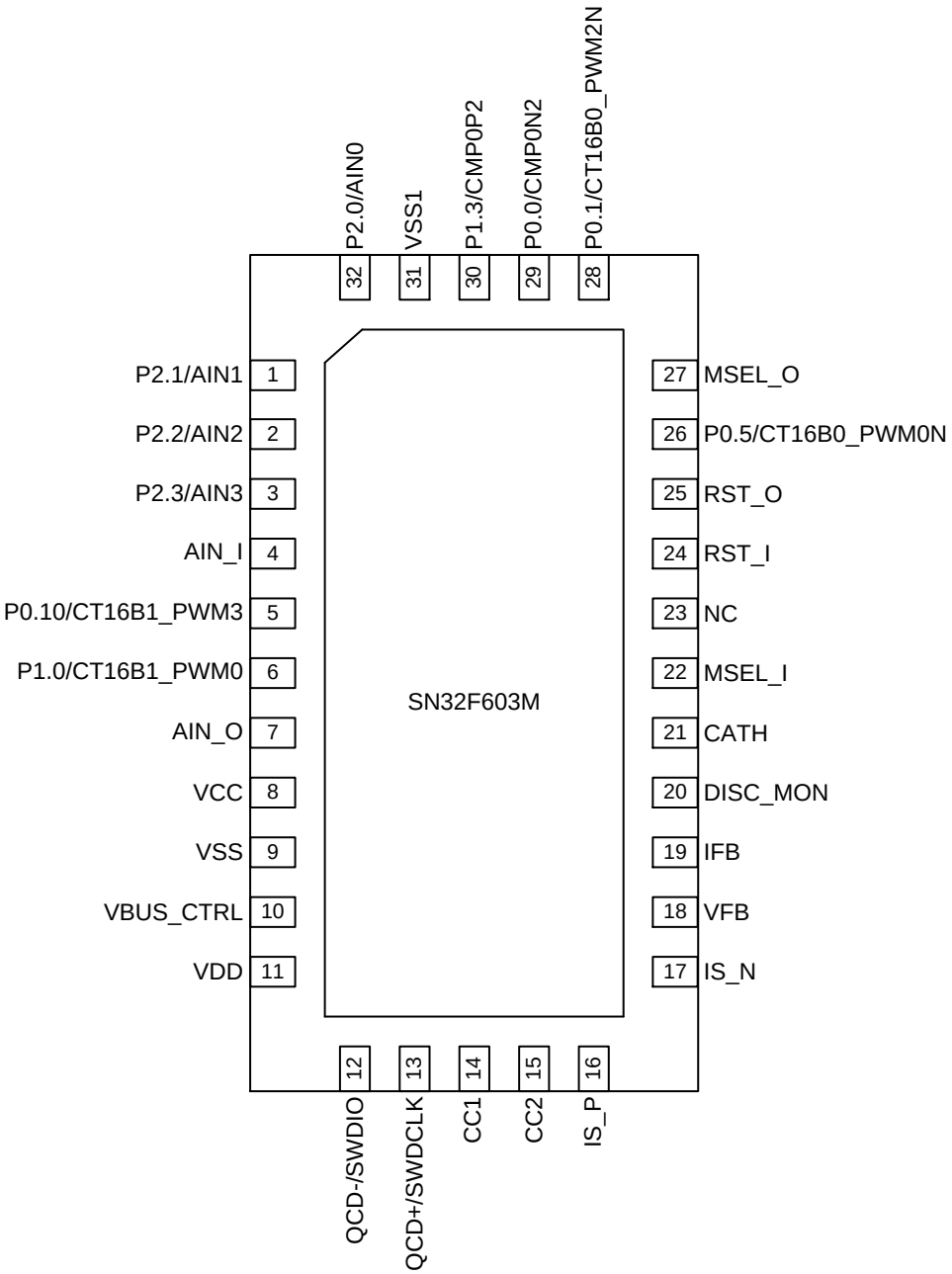


Figure 2–3 SN32F603M Pin Assignment

2.3.2 Pin Description

Table 2–3 SN32F603M Pin Description

Name	Pin No.	Type[2]	Description
P2.1	1	I/O	General purpose digital input/output
AIN1		AI	ADC channel input 1
P2.2	2	I/O	General purpose digital input/output
AIN2		AI	ADC channel input 2
P2.3	3	I/O	General purpose digital input/output
AIN3		AI	ADC channel input 3
AIN_I	4	AI	ADC channel input
P0.10	5	I/O	General purpose digital input/output
CT16B1_PWM3			PWM output 3 for CT16B1
P1.0	6	I/O	General purpose digital input/output
CT16B1_PWM0			PWM output 0 for CT16B1
AIN_O	7	AO	ADC channel output
VCC	8	P	Power supply input voltage
VSS	9	GND	Power supply ground
VBUS_CTRL	10	I/O	External MOSFET control
VDD	11	P	HV LDO output for digital and analog circuit
QCD-	12	I/O	USB D- channel
SWDIO			SWD serial wire debug input/output
QCD+	13	I/O	USB D+ channel
SWDCLK			SWD serial wire clock
CC1	14	I/O	Type-C connector configuration channel 1
CC2	15	I/O	Type-C connector configuration channel 2
IS_P	16	AI	Positive input of a current sense amplifier for output current sensing
IS_N	17	AI	Negative input of a current sense amplifier for output current sensing
VFB	18	AI	Feedback input for the constant-voltage loop
IFB	19	AI	Feedback input for the constant-current loop
DISC_MON	20	AO	Type-C VBUS monitor with internal discharge FET
CATH	21	AI	Cathode of voltage regulation and compensation for other applications
MSEL_I	22	I	Mode select input for SPI or I^2C
NC	23	–	No connection should be made to this pin
RST_I	24	I	System external reset input
RST_O	25	O	System external reset output

Name	Pin No.	Type[2]	Description
P0.5	26	I/O	General purpose digital input/output
CT16B0_PWM0N			Negative PWM output 0 for CT16B0
MSEL_O	27	O	Mode select output for SPI or I^2C
P0.1	28	I/O	General purpose digital input/output pin
CT16B0_PWM2N			Negative PWM output 2 for CT16B0
P0.0	29	I/O	General purpose digital input/output pin
CMP0N2			Negative input pin 2 of comparator 0
P1.3	30	I/O	General purpose digital input/output pin
CMP0P2			Positive input pin 2 of comparator 0
VSS1	31	GND	Digital ground
P2.0	32	I/O	General purpose digital input/output
AIN0		AI	ADC channel input 0

3 System

3.1 MCU Subsystem

The SN32F600 Series has a 32-bit MCU subsystem, which integrates an ARM Cortex-M0 processor. The MCU subsystem includes a 32 KB flash ROM, a 4 KB RAM, a Nested Vectored Interrupt Controller (NVIC), and two 16-bit timers consisted of 48 MHz RC oscillators and 16 KHz RC oscillators to achieve high efficiency with low power consumption.

3.2 USB-PD Subsystem

3.2.1 USB-PD Physical Layer

The USB-PD Physical Layer consists of a transmitter and receiver that communicate BMC-encoded data over the CC channel based on the PD 3.0 standard. All communication is half-duplex. The Physical Layer or PHY provides collision avoidance to minimize communication errors on the channel.

The USB-PD block includes all termination resistors (R_P and R_D) and their switches as required by the USB-PD specification. R_P and R_D resistors are required to implement connection detection, plug orientation detection, and for establishing USB DFP/UFP roles. The R_P resistor is implemented as a current source.

According to the USB Type-C specification, a Type-C controller such as the SN32F600 Series must present certain termination resistors depending on its role in its unpowered state. The Sink role in a power bank application requires R_D resistors to be present on the CC pins whereas the DFP role, as in a power adapter, requires both CC pins to be open. To be flexible for such applications, the SN32F600 Series includes the resistors required in the unpowered state on separate pads or pins.

3.2.2 ADC

The high precision 12-bit SAR ADC is used to detect and monitor analog signals of the peripherals such as the signals of the voltage detection circuit at CC1/CC2 and QCD+/QCD-, output voltage and current of VBUS, and internal thermal sensor and signals for external NTC thermal detection.

3.2.3 Charger Detection (QCD+/QCD-)

The D+/D- detection and charging protocol are compliant with conventional battery charging protocol (BC1.2) and Qualcomm QuickCharge 2.0/3.0/4.0/4.0+ charging protocols.

3.2.4 VBUS Overcurrent and Overvoltage Protection

The VBUS voltage sensing circuit and the shunt regulator of the SN32F600 Series form an integrated hardware protection circuit with fast response and adjustability for VBUS overvoltage and overcurrent protection.

3.2.5 Low-side Current Sense Amplifier (LSCSA)

The SN32F600 Series has a built-in current sensing circuit with input offset cancellation and programmable gain selections including 20, 40, 60, 80 and 100 V/V. With an external 5 mΩ precision resistor, the accuracy of the sensing circuit is 50 mA. The LSCSA also supports constant current mode in a power adapter application as a source.

3.2.6 MOSFET of Gate Driver on VBUS Path

A built-in gate driver controls the external MOS switch on the VBUS. The MOS switch is turned on when the Type-C sink side is attached. The MOS switch is turned off when the Type-C sink side is detached or an error (i.e. overcurrent, short circuit...) occurs.

3.2.7 VBUS Discharger FETs

The VBUS discharge circuit of the SN32F600 Series discharges secondary-side bulk capacitor voltage when a device is removed or during voltage decrease (i.e. from 20V to 12V) to achieve the time requirement of the USB-PD specification. The typical value of the sink current is 16 mA.

3.2.8 Shunt Regulator

Two regulators are parallel and connected to an open-drain output, CATH pin. The operation of each feedback loop is similar to that of a typical TL431 shunt regulator except that VCATH operating range is wider, from -0.3V to VCC+0.3V, which enables simple designs of the converters with a wider output range.

The VFB DAC and IFB DAC convert the signals from the 32-bit MCU subsystem to reference voltage and current (VREF_CV and VREF_CC) for the voltage and current feedback loops (VFB and IFB) respectively. The analog output range of the 11-bit DAC is from 0 to VDAC_MAX (typically 3V), which makes output voltage resolution as small as 10 mV, 14.6 mV, or 20 mV to achieve high-precision CV regulation.

3.3 Power System

The SN32F600 Series can operate from single external supply source, VCC (3.0V to 24.5V). When powered through VCC, the internal regulator generates a VDD of 5V for chip operation. The regulated supply is either used directly inside some analog blocks or further regulated VDD1 (5V), which powers the majority of the core using the regulators. The SN32F600 Series has three different power modes: normal, sleep, and deep sleep.

Transitions between these power modes are managed by the power system. When powered through the VCC pin, the VDD cannot be used to power external devices and should be connected to a 1 µF capacitor for regulator stability. These pins are not supported as power supplies. Figure 4–1 and Figure 4–2 show the application diagrams for capacitor connections.

Table 3–1 Power Mode

Name	Description
POR (Power on Reset)	Power is valid and an internal reset source is asserted or the sleep controller is sequencing the system out of reset.
Normal Mode	Power is valid and the CPU is executing instructions.
Sleep Mode	Power is valid and the CPU is not executing instructions. All logic that is not operating is clock gated to save power.
Deep Sleep Mode	The main regulator and most blocks are shut off. The deep sleep regulator powers logic, but only the low-frequency clock is available.

3.4 Programming Mode

The SN32F600 Series devices are programmed over the SWD interface only during development or during the manufacturing process of the end product. Sonix provides a programming kit called SN-Link PD and SN-Link ISP Tool which can be used to program the flash as well as debug firmware. The flash is programmed by downloading the information from a hex file. This hex file is a binary file generated as an output of building the firmware project in SN-Link ISP Tool Creator Software. There are many third party programmers that support mass programming in a manufacturing environment.

The SN-Link PD connects with a device through a switching board. Figure 3–1 shows the pin relationship between the SN-Link and the device. The device enters debug mode through a CC pin and enables the SN32F600 Series SWDCLK and SWDIO pin functions while QCD+ and QCD- functions are disabled. When a firmware is loaded to the device, the pins of the SN32F600 Series return to the functions as before the power-on. The device will activate the firmware upon the completion of reloading.

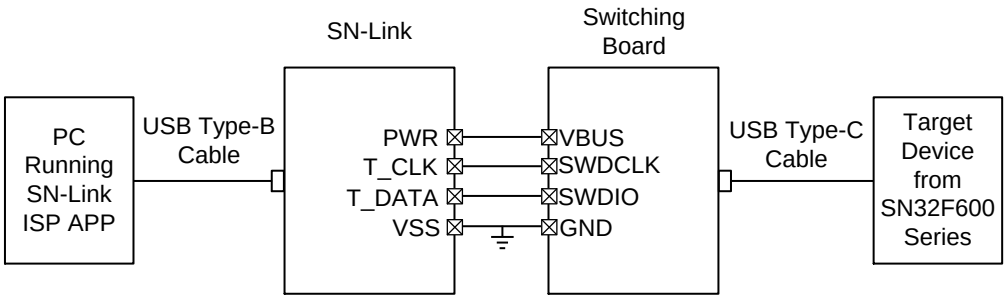


Figure 3–1 Connecting the Programmer

4 Application – Power Adapter

The SN32F600 Series controls the power supply to the device according to the response of the device from the handshake when the power adapter, the device, and the AC power supply are connected. In the power converter application, the shunt regulator of the SN32F600 Series forms a feedback path with an optocoupler. The feedback voltage from the VCC divider voltage and the CATH signal are combined and transmitted to the voltage comparator of the Shunt regulator through VFB to compare with VREF_CV from VFB DAC. The feedback current, IS_N and IS_P, from the low side current sense amplifier and the CATH signal are combined and transmitted to the voltage comparator of the Shunt regulator through IFB to compare with VREF_CC from IFB DAC. The Shunt regulator connects to CATH with optocoupler to feedback signals to the primary-side that has a converter, and to regulate the output voltage and current from the secondary-side where a device is connected depending on the feedback signals. When the power is supplied through VBUS, the SN32F600 Series precisely charges various devices using the USB-PD or the QC protocol. Figure 4–1 and Figure 4–2 illustrate power adapter application with PMOS and NMOS control respectively.

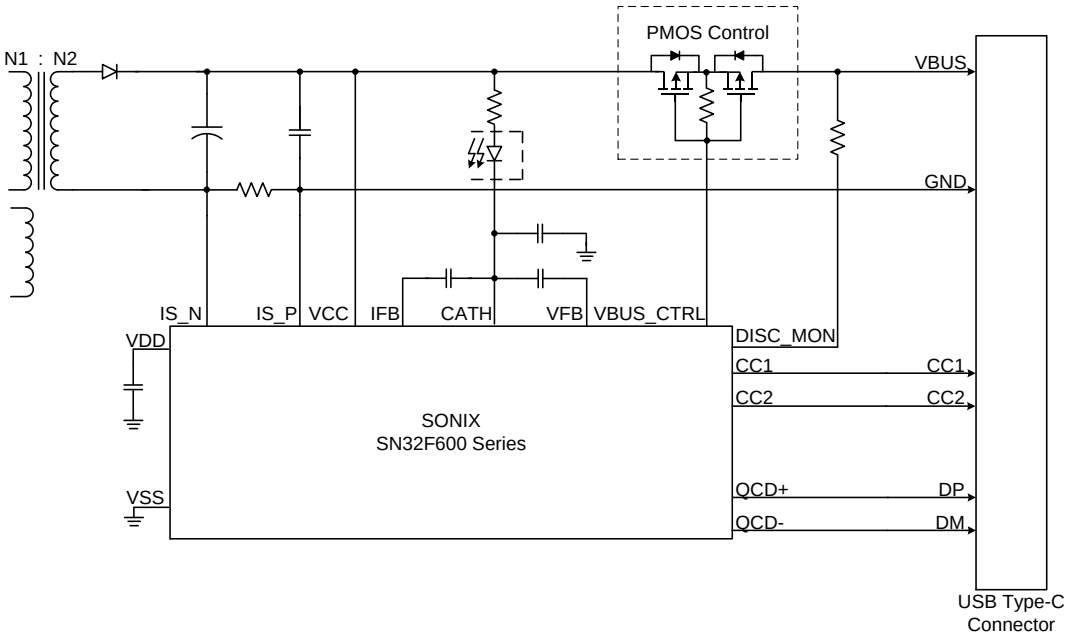


Figure 4–1 Power Adapter Application with PMOS Control

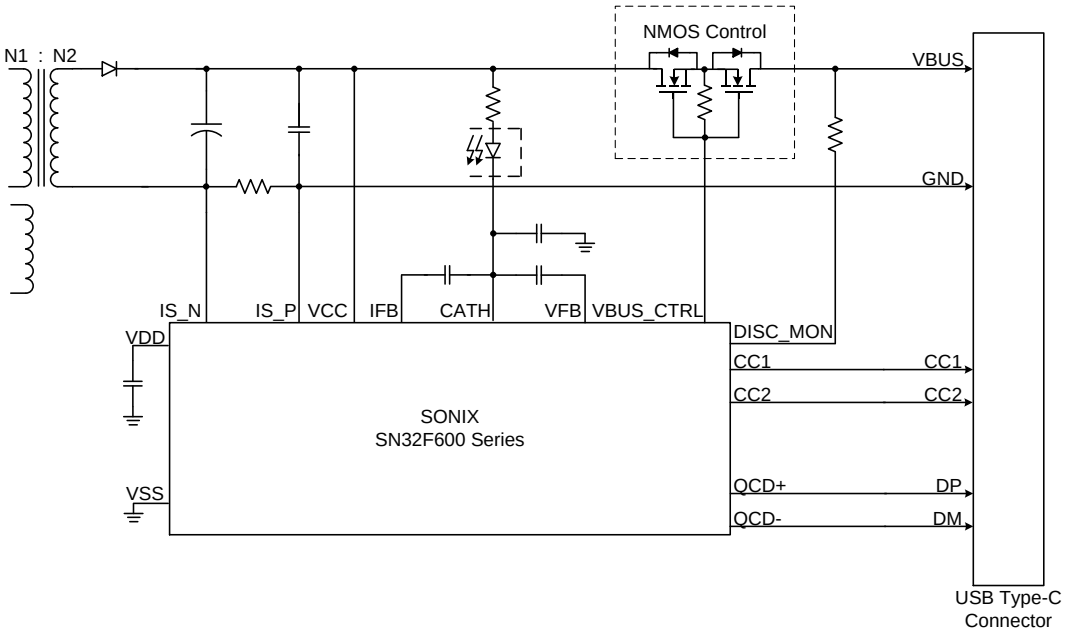


Figure 4–2 Power Adapter Application with NMOS Control

5 Device Operating Conditions

5.1 Absolute Maximum Ratings

Table 5–1 Absolute Maximum Ratings[3] [4] [5]

Parameter		Rating	Unit
Supply Voltage Ranges	VCC	-0.3 to 30	V
Input Voltage Ranges	CC1, CC2, QCD+,QCD-, VBUS_CTRL, DISC_MON, CATH	-0.3 to VCC + 0.3 (Max. 30V)	
	IS_P, IS_N, VFB, IFB, GPIO, ADC	-0.3 to 5.5	
Output Voltage Ranges	VBUS_CTRL	-0.3 to VCC + 8 (Max. 30V)	
	CC1, CC2, QCD+, QCD-, IS_P, IS_N, DISC_MON, GPIO, VDD	-0.3 to 5.5	
Ambient Temperature Ranges (T_A)		-40 to 105	°C
Operating Junction Temperature Ranges (T_J)		-40 to 105	
Storage Temperature Ranges (T_{STG})		-40 to 150	

5.2 Recommended Operating Conditions

Table 5–2 Recommended Operating Conditions

Parameter	MIN.	TYP.	MAX.	Unit
Supply Voltage, VCC	3.0	–	24.5	V
Supply Ground, Thermal pad	0	0	0	V

Table 5–3 Electrical Characteristics for DC Specifications

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
Input Voltage	V_{CC}	–	3.0	–	24.5	V
Output Voltage	V_{DD}	V_{CC} > 5.4V	4.9	5.0	5.1	V
Input Capacitance	C_{VCC}	–	–	1	–	µF
Output Capacitance for VDD	C_{VDD}	–	–	1	–	µF
Supply Current for VCC	I_{VCC}	–	–	–	20	mA

[3] Long-term exposure to absolute maximum ratings may affect device reliability, and permanent damage may occur if the operation exceeds the maximum ratings.
[4] All voltage values are with respect to VSS.
[5] The ratings are measured based on reference design.

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
Normal Mode						
VCC Power Consumption in the Normal Mode	I_{VCC_A}	V_{CC} = 5V, T_A = 25°C, CC1/CC2 in Tx or Rx, no I/O sourcing current, QCD+/QCD- output voltage, HVLDO/Shunt Regulator/DAC/LS CSA/ NMOS Gate Driver/ADC ON, CPU at 24 MHz.	–	12	–	mA
Sleep Mode						
VCC Power Consumption in the Sleep Mode	I_{VCC_S}	V_{CC} = 5V, T_A = 25°C, all blocks sleep except for CPU, CC/QCD+/QCD-, and Shunt Regulator/DAC/LS CSA/ADC ON	–	5.5	–	mA
Deep-sleep Mode						
VCC Power Consumption in the Deep-sleep Mode	I_{VCC_DS}	V_{CC} = 5V, T_A = 25°C, Type-C not attached. CC/QCD+/QCD- attach function enabled for wakeup	–	450	–	uA

Table 5–4 Electrical Characteristics for I/O DC Specifications[6]

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
Input Voltage HIGH Threshold	V_{IH}	–	0.7 x V_{DD}	–	V_{DD}	V
Input Voltage LOW Threshold	V_{IL}	–	V_{ss}	–	0.3 x V_{DD}	V
Output Voltage HIGH Threshold	V_{OH}	–	V_{DD} - 0.5V	–	–	V
Output Voltage LOW Threshold	V_{OL}	–	–	–	V_{SS} + 0.5V	V
Internal Pull-up Resistance	R_{PU}	V_{DD} = 5V	–	50	–	kΩ
Output Source Current	I_{OH}	V_{OP} = V_{DD} - 0.5V	–	10	–	mA
Output Sink Current	I_{OL}	V_{OP} = V_{SS} + 0.5V	–	10	–	mA
Input Leakage Current	I_{LC}	–	–	–	2.0	uA

Table 5–5 Electrical Characteristics for ADC DC Specifications

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
ADC Reference Voltage	V_{ADC_REF}	–	2.0	–	V_{DD}	V
ADC Clock Frequency	F_{ADCCLK}	–	–	–	12	MHz
ADC Sampling Rate	F_{ADCSMP}	V_{DD} = 5V	–	–	200	kHz

[6] The parameters below apply to P0.1, P0.5, P0.6, P0.7, P0.10, P1.0, P1.3, P1.6, P2.0, P2.2, P2.3, and P2.4.

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
ADC Offset Voltage	V_{ADC_Offset}	–	-5.0	–	5.0	mV
No Missing Code	NMC	–	10	–	12	Bits

Table 5–6 Electrical Characteristics for Current Sense Amplifier

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
CSA Accuracy	V_{CM_ACC1}	5 mV < Vsense < 10 mV	-15	–	15	%
	V_{CM_ACC2}	10 mV < Vsense < 15 mV	-10	–	10	%
	V_{CM_ACC3}	15 mV < Vsense < 20 mV	-6.0	–	6.0	%
Register-programmable Current Sense Voltage Gain	G_{vv}	+20/Step	20	–	100	V/V
Unit Gain Bandwidth	U_{BW}	–	–	250	–	kHz

Table 5–7 Electrical Characteristics for DISC_MON

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
VBUS Discharger Sinking Current	I_{DISC_MON}	V_{DISC_MON} = 20V	–	16	–	mA

Table 5–8 Electrical Characteristics for VCC_DISC

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
VCC Discharger Sinking Current	I_{VCC_DISC1}	V_{CC} = 20V	–	20	–	mA
	I_{VCC_DISC2}		–	40	–	mA
	I_{VCC_DISC3}		–	60	–	mA
	I_{VCC_DISC4}		–	80	–	mA
	I_{VCC_DISC5}		–	100	–	mA
	I_{VCC_DISC6}		–	120	–	mA

Table 5–9 Electrical Characteristics for QCD+/QCD- Specifications

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
QCD+ Pull-down Resistance	R_{L_D+}	–	300	–	1500	kΩ
QCD- Pull-down Resistance	R_{L_D-}	–	14.25	–	24.80	kΩ
Register-programmable Output High Voltage	$V_{OH\_3.0V}$	–	2.70	3.00	3.30	V
	$V_{OH\_1.8V}$	–	1.62	1.80	1.98	V
	$V_{OH\_0.6V}$	–	0.5	0.60	0.7	V
	V_{OH_APPLE}	Apple 2.4A mode	2.43	2.70	2.97	V
Register-programmable Input Trip Voltage	V_{IH_D+D-}	–	1.90	2.00	2.10	V
		–	0.90	1.00	1.10	V
		–	0.25	0.325	0.40	V
QCD+ QCD- Switch On-Resistance	R_{ON_D+D-}	–	–	20	40	Ω
Output Low Voltage	V_{OL_3V}	R_{LOAD} = 6kΩ	–	–	0.20	V
	$V_{OL\_1.8V}$					
	$V_{OL\_0.6V}$					

Table 5–10 Electrical Characteristics for CC1/CC2 Specifications

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
Output High Voltage	V_{OH}	–	1.04	–	1.20	V
Output Low Voltage	V_{OL}	–	-0.075	–	0.075	V
Rise Time/Fall Time	T_{RISE}/T_{FALL}	–	300	–	675	ns
DFP CC Termination for Default USB Power	$I_{CC\_default}$	–	68	80	92	µA
DFP CC Termination for 1.5A power	$I_{CC\_1.5A}$	–	165	180	194	µA
DFP CC Termination for 3.0A power	I_{CC_3A}	–	303	330	356	µA
UFP CC Termination	Rd	–	4.59	5.10	5.61	kΩ
Power Cable Termination	Ra	–	800	1000	1200	Ω

Table 5–11 Electrical Characteristics for Shunt Regulator Specifications

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
Off-State CATH Current	I_{CATH_OFF}	Open-circuited CATH pin	–	–	2.0	µA
Maximum CATH Sinking Current	I_{CATH_MAX}	–	2.0	–	20	mA

Table 5–12 Electrical Characteristics for Gate Driver Specifications

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
Gate to Source voltage driving external FETs	V_{GS}	–	4.5	–	8	V
Resistance when pull-down enable	R_{PD}	–	–	–	4	kΩ

5.3 AC Characteristics

Table 5–13 AC Specifications

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
Main oscillator frequency	F_{CPU}	–	–	–	48	MHz
Low frequency oscillator	F_{ILRC}	–	–	16	–	kHz
Wakeup from sleep mode	T_{SLEEP}	–	–	30	–	µs
Wakeup from deep-sleep mode	$T_{DEEPSLEEP}$	–	–	64	–	µs
Power-on I/O Initialization Time	T_{POR}	–	–	6.25	–	ms

6 Mechanical Data

6.1 Thermal Data

The permissible operating temperature range for the bearing is -40°C to 105°C.

6.2 Package Information

6.2.1 Nomenclature

The product ID and symbols shown in the figure below are examples and may vary according to different packages.

LOGO
Product ID
DATECODE + (SONIX) + e3 (Eco-friendly Products)

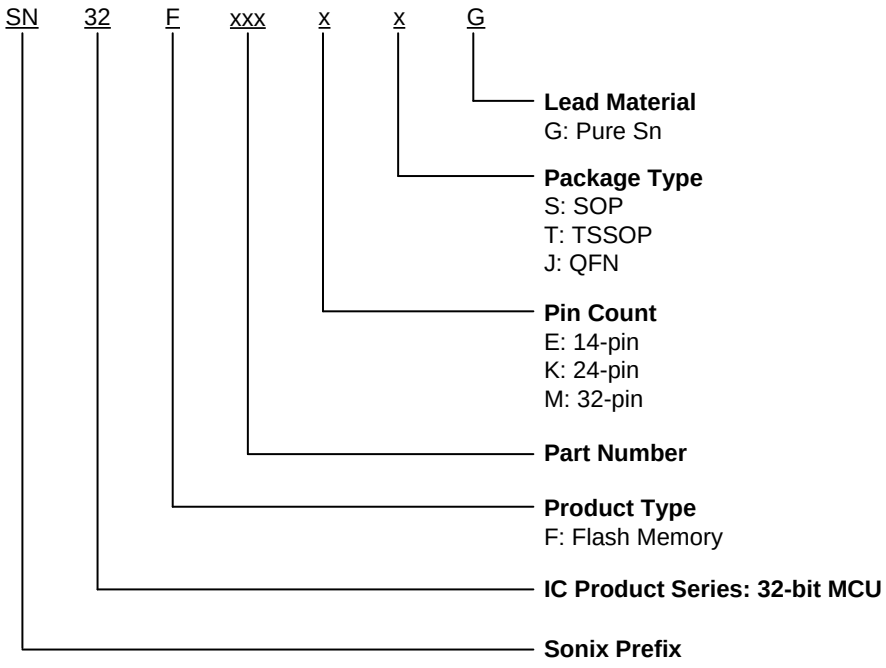
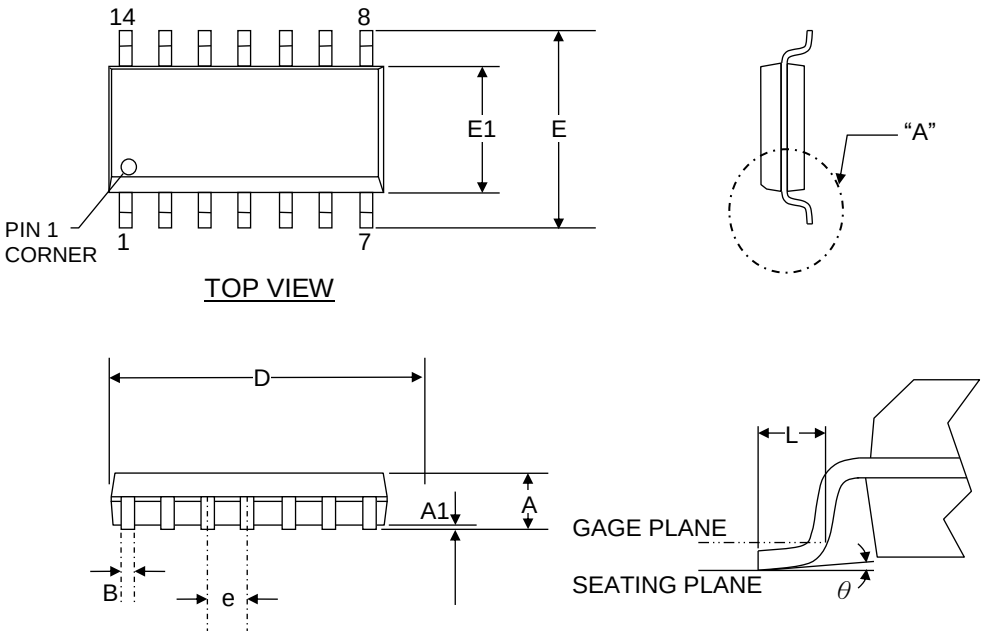


Figure 6–1 Device Nomenclature

6.2.2 Package Dimensions

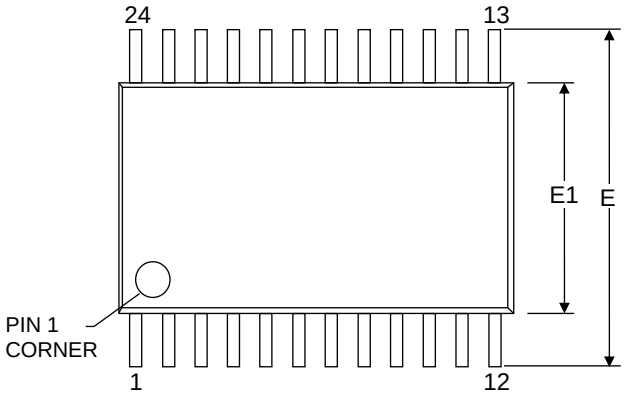
I. SOP14L (150 MIL)



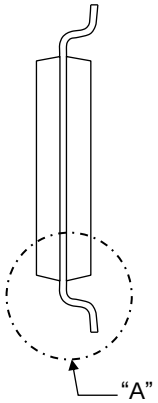
Symbols	Dimension in mm[7]			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	–	1.75	–	–	0.069
A1	0.05	–	0.25	0.002	–	0.010
B	0.31	–	0.51	0.012	–	0.020
D	8.65 BSC			0.340 BSC		
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
L	0.40	–	1.27	0.015	–	0.050
θ	0˚	4˚	8˚	0˚	4˚	8˚

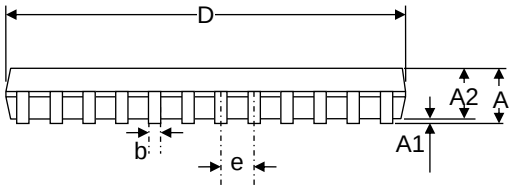
[7] Controlling dimension: mm

II. TSSOP24L (173 MIL)

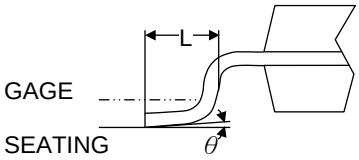


TOP VIEW





SIDE VIEW

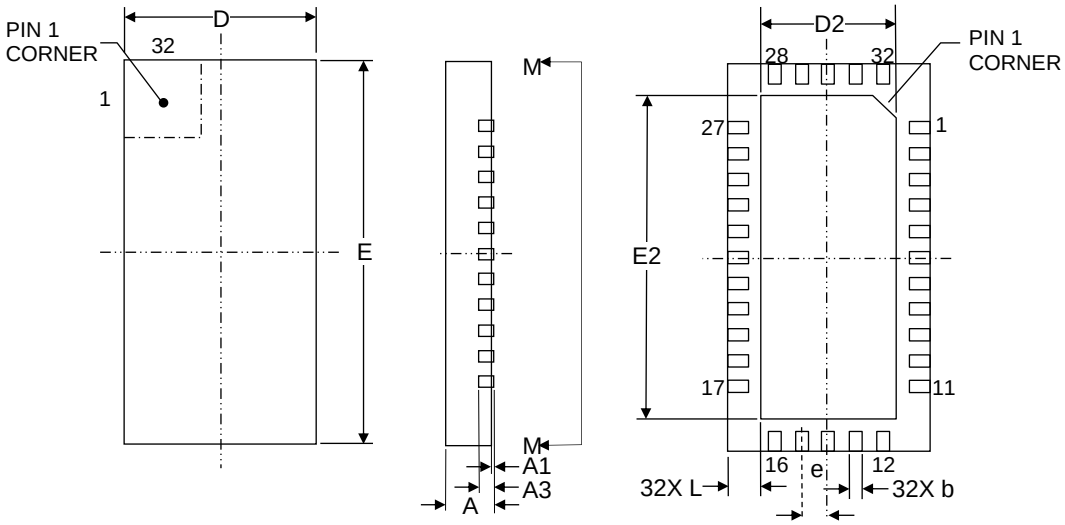


DETAIL "A"

Symbols	Dimension in mm[7]			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	–	1.20	–	–	0.047
A1	0.00	–	0.15	0.000	–	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b[8]	0.19	–	0.30	0.007	–	0.012
D[9]	7.70	7.80	7.90	0.303	0.307	0.311
E	6.40 BSC			0.252 BSC		
E1[10]	4.30	4.40	4.50	0.169	0.173	0.177
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
θ	0˚	–	8˚	0˚	–	8˚

[8] Dimension "b" does not include dambar protrusion.
[9] Dimension "D" does not include mold flash, protrusions or gate berres.
[10] Dimension "E1" does not include interlead flash or protrusion.

III. QFN32L (3 x 6 x 0.8 mm, Pitch: 0.4 mm)



TOP VIEW SIDE VIEW BOTTOM VIEW
VIEW M—M

Symbols	Dimension in mm[7]			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.028	0.031	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.203 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	3.00 BSC			0.118 BSC		
E	6.00 BSC			0.236 BSC		
e	0.40 BSC			0.016 BSC		
D2	1.90	2.00	2.05	0.075	0.079	0.081
E2	4.90	5.00	5.05	0.193	0.197	0.199
L	0.20	0.30	0.40	0.008	0.012	0.016

6.3 Packaging Appearance and Storage Information

6.3.1 Packing Quantity

Table 6–1 Packing Quantity Information

Type	Pin Count	Carry Type	Package Size	IC Q'ty per Tube or Tray or Reel	Tube or Tray or Reel Q'ty per Inner Box	Total Q'ty in One Inner Box	Inner Box Q'ty per Carton	IC Q'ty per Carton
SOP	14	Tube	150 MIL	58	100	5800	6	34800
TSSOP	24	Tube	173 MIL	60	100	6000	6	36000
QFN	32	Tray	3 x 6	490	10	4900	6	29400

6.3.2 Packing Dimension

Table 6–2 Inner Box/Carton Dimension

Inner Box/Carton	Carry Type	Dimension in mm
Inner box	Tray	358 x 159 x 88
	Tube	610 x 170 x 100
Carton	Tray	555 x 435 x 280
	Tube	630 x 360 x 345

6.3.3 Temperature and Humidity Environmental Control Requirements in Storage

Table 6–3 Store Condition

Control Requirement	Specification
Temp (°C)	24 ± 6
Humid. (%RH)	60 ± 20

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