SNAUD01
Mono/Stereo Audio Codec

1 Introduction

1.1 Features

System
- Operation voltage: 3.3V–5.5V
- Single/Dual-channel Sigma Delta ADC
- Dual-channel Sigma Delta DAC
- Built-in speaker driver
  – Current: 300 mA
  – Power: 0.72W at 8 ohm load
- On-chip PLL
- Audio sample rates: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 kHz
- Standard audio interface: I^2S
- Power-down and wake-up key

Sigma Delta ADC
- 24-bit resolution
- 100 dB Signal-to-Noise Ratio (SNR)
- Programmable microphone bias
- Microphone preamplifier
  – Programmable boost gain: 0 to +50 dB
  – Programmable PGA gain: -12 to +35.25 dB
  – Step = 0.75 dB
- Mute attenuation: -85 dB
- Zero-crossing gain control
- Anti-aliasing filter
- Single-ended or differential microphone inputs

Sigma Delta DAC
- 24-bit resolution
- 100 dB Signal-to-Noise Ratio (SNR)
- Integrated headphone driver: 200 mW into 16 ohm
- Programmable digital volume control from -96 to 0 dB, step = -0.375 dB
- Mute attenuation: 85 dB
- Digital high-pass filter (HPF)

Class-AB Audio Amplifier
- Mono audio amplifier with differential output
- Output driver: 300 mA at 3V
- Power: 0.72W at 8 ohm load
- 32-level volume control

LDO33 Regulator
- Input voltage: 3.3V to 5.5V
- Output voltage: 3.3V ± 0.1V
- Output current: Up to 150 mA
- Low quiescent current: 3.0 μA typically

Voltage
- Analog: 1.7V–1.9V
- Digital core: 1.7V–1.9V
- Digital I/O: 1.7V–3.6V
- SPK: 3.3V–5.5V

Package
- QFN32L (5 x 5 x 0.8 mm)
- SSOP24L (150 MIL)

1.2 Description

The SNAUD01 is a low-power mono/stereo audio codec with ADCs, DACs, and a speaker driver. The device integrates a headphone driver, preamplifiers for single-ended or differential microphone, and LDO regulators. The ADC provides high quality audio at numerous sample rates. The class-AB amplifier provides flexibility for designs by driving 8 ohm speakers with single 5V supply. The two LDO regulators supply 3.3V and 1.85V power to provide continuous current for the backend main chip. A programmable fractional PLL is provided for flexible clock generation from an external master clock.

With a larger boost gain, 24-bit precision ADCs and DACs, a mono class-AB amplifier driver, and power regulators, the SNAUD01 is suitable for applications with microphone recording and audio playback features such as voice telephony, protable personal audio devices, and digital video camcorders.

1.3 Functional Block Diagram

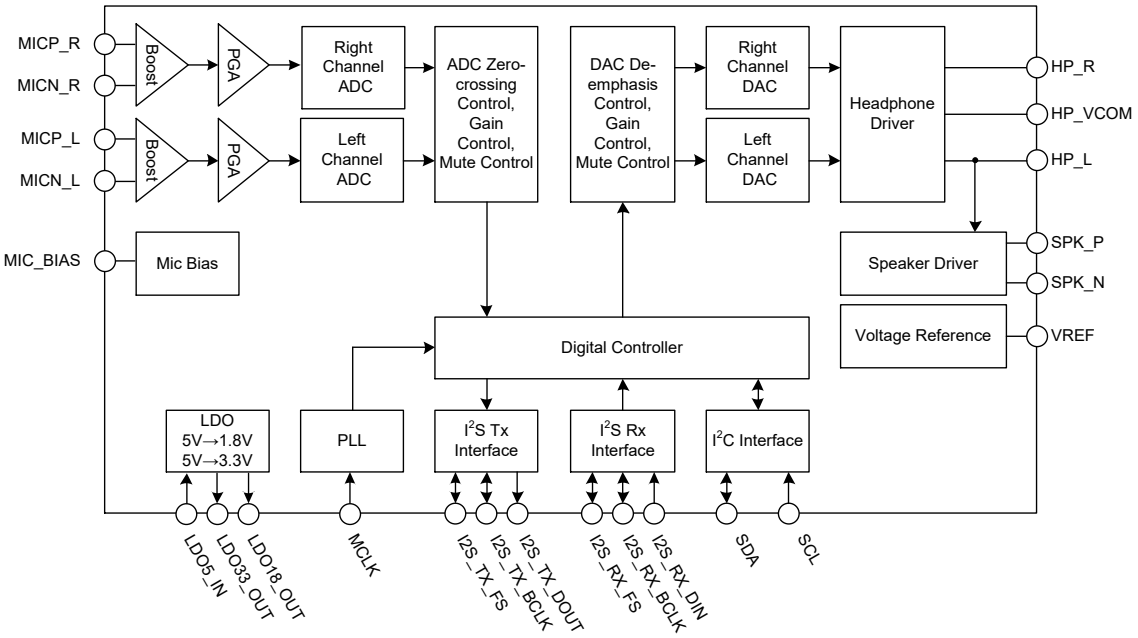

Figure 1–1 Functional Block Diagram

1.4 Selection Table

Table 1–1 Selection Table

Device	Package	Microphone	Headphone	Speaker
SNAUD01BMJG	QFN32L	Dual-channel	✓	✓
SNAUD01BKXG	SSOP24L	Single-channel	–	✓

Revision History

Date	Revision	Description
24-Feb-2022	1.0	Initial release
20-May-2022	1.1	Updated regulator and voltage information in Features Added high pass filter frequency response related information and ADC Adjustment Register in Section 3.5 Updated Figure 3–44, Figure 3–45, and Figure 3–46 Updated description of V2 in Table 5–4
26-Oct-2022	1.2	Added SNAUD01KXG and all related information Added Section 6.2.1 Nomenclature Updated Appendix A
30-May-2023	1.3	Removed SNAUD01KXG and all related information Updated the nomenclature
05-Jul-2023	1.4	Added SNAUD01BKXG and all related information Added 1.4 Selection Table
31-Jul-2023	1.5	Updated Figure 3–45 and Figure 3–46
12-Sep-2023	1.6	Updated pin #11 and pin #12 of SNAUD01BKXG Updated Section 3.4.2 Scenario Updated Appendix A
24-Jan-2024	1.7	Updated operation voltage and SPK voltage in Features, LDO Regulator (LDO_CTRL), Recommended Operating Conditions, and Electrical Characteristics

Convention

ⓘ **WARNING**	Indicates a hazard with a medium or low level of risk that, if not avoided, could result in minor or moderate injury.
🛠 **TIP**	Indicates a tip that may help you solve a problem or save time.
🕮 **NOTE**	Provides additional information to emphasize or supplement important points of the main text.

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2.1 SNAUD01BMJG

2.1.1 Pin Assignment

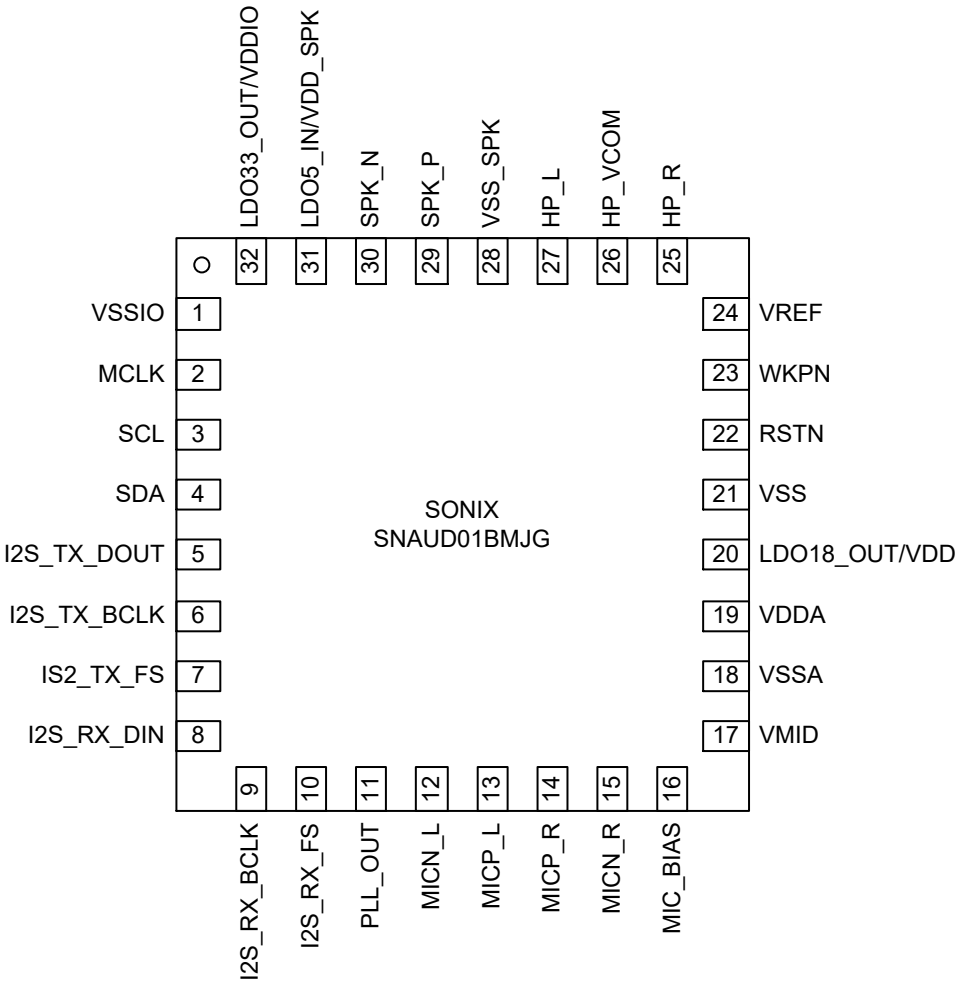


Figure 2–1 SNAUD01BMJG Pin Assignment

2.1.2 Pin Description

Table 2–1 SNAUD01BMJG Pin Description

No.	Name	Type[1]	Description
1	VSSIO	G	Ground for digital input/output
2	MCLK	I	Master clock
3	SCL	I	I^2C serial clock
4	SDA	I/O	I^2C serial data
5	I2S_TX_DOUT	O	I^2S transmitter data output
6	I2S_TX_BCLK	I/O	I^2S transmitter bit clock
7	I2S_TX_FS	I/O	I^2S transmitter frame sync
8	I2S_RX_DIN	I	I^2S receiver data input
9	I2S_RX_BCLK	I/O	I^2S receiver bit clock
10	I2S_RX_FS	I/O	I^2S receiver frame sync
11	PLL_OUT	O	Internal PLL output pin
12	MICN_L	AI	Microphone left channel negative input
13	MICP_L	AI	Microphone left channel positive input
14	MICP_R	AI	Microphone right channel positive input
15	MICN_R	AI	Microphone right channel negative input
16	MIC_BIAS	AO	Microphone bias voltage output
17	VMID	AO	ADC VMID pin
18	VSSA	G	Ground for ADC and DAC
19	VDDA	P	Power supply for ADC and DAC
20	LDO18_OUT / VDD	P	LDO 1.8V output / General power supply
21	VSS	G	General ground
22	RSTN	I	Reset pin
23	WKPN	I	Wake-up pin
24	VREF	AO	Speaker driver voltage reference
25	HP_R	AO	Headphone right channel output
26	HP_VCOM	AO	Headphone VCOM output for capless headphone jack
27	HP_L	AO	Headphone left channel output
28	VSS_SPK	G	Ground for speaker driver
29	SPK_P	AO	Speaker positive output
30	SPK_N	AO	Speaker negative output
31	LDO5_IN / VDD_SPK	P	LDO 5V input / Power supply for speaker driver
32	LDO33_OUT / VDDIO	P	LDO 3.3V output / Power supply for digital input/output

[1] Signal Types:
I = Input
O = Output
A = Analog signal
P = Power
G = Ground

2.2 SNAUD01BKXG

2.2.1 Pin Assignment

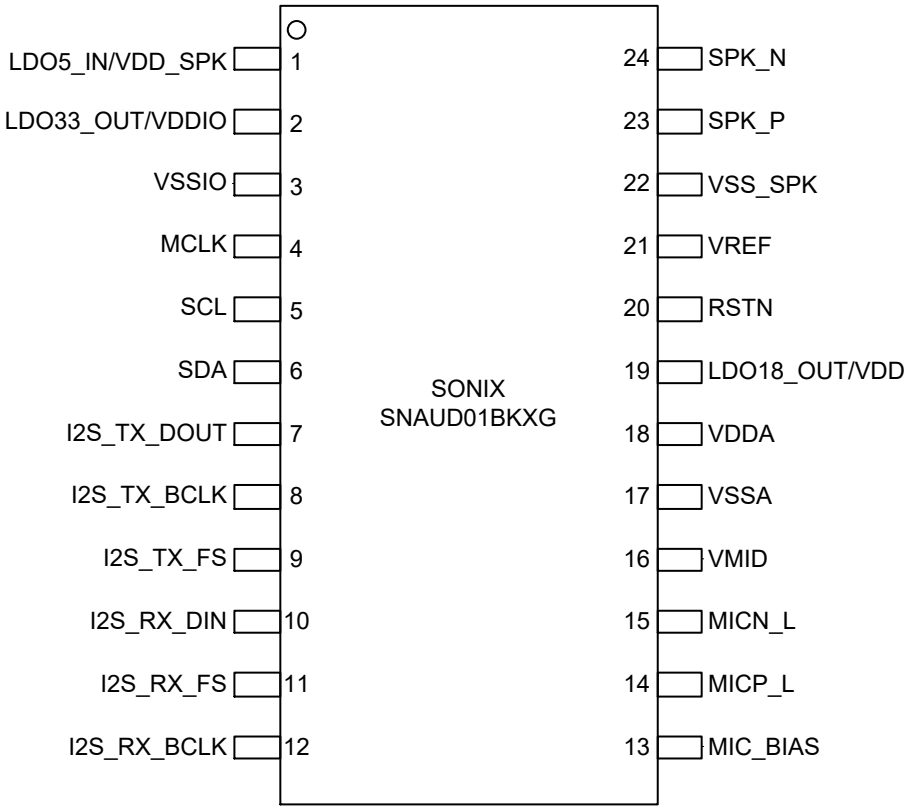


Figure 2–2 SNAUD01BKXG Pin Assignment

2.2.2 Pin Description

Table 2–2 SNAUD01BKXG Pin Description

No.	Name	Type[2]	Description
1	LDO5_IN / VDD_SPK	P	LDO 5V input / Power supply for speaker driver
2	LDO33_OUT / VDDIO	P	LDO 3.3V output / Power supply for digital input/output
3	VSSIO	G	Ground for digital input/output
4	MCLK	I	Master clock
5	SCL	I	I^2C serial clock
6	SDA	I/O	I^2C serial data
7	I2S_TX_DOUT	O	I^2S transmitter data output
8	I2S_TX_BCLK	I/O	I^2S transmitter bit clock
9	I2S_TX_FS	I/O	I^2S transmitter frame sync
10	I2S_RX_DIN	I	I^2S receiver data input
11	I2S_RX_FS	I/O	I^2S receiver frame sync
12	I2S_RX_BCLK	I/O	I^2S receiver bit clock
13	MIC_BIAS	AO	Microphone bias voltage output
14	MICP_L	AI	Microphone left channel positive input
15	MICN_L	AI	Microphone left channel negative input
16	VMID	AO	ADC VMID pin
17	VSSA	G	Ground for ADC
18	VDDA	P	Power supply for ADC
19	LDO18_OUT / VDD	P	LDO 1.8V output / General power supply
20	RSTN	I	Reset pin
21	VREF	AO	Analog middle voltage reference
22	VSS_SPK	G	Ground for speaker driver
23	SPK_P	AO	Speaker positive output
24	SPK_N	AO	Speaker negative output

[2] Signal Types:
I = Input
O = Output
A = Analog signal
P = Power
G = Ground

3 Register

Table 3–1 lists the function of the register corresponding to each offset.

Table 3–1 Registers Summary

Address: 0x0000_0000

Offset	Name	Description
0x00	MCLK_CTRL	Clock/FPLL/low pass filter control
0x01	FPLL_CTRL	FPLL control
0x02	LDO_CTRL	Regulator control
0x03	–	Reserved
0x04	FPLL_FRA0	FPLL fraction[19:16]
0x05	FPLL_FRA1	FPLL fraction[15:8]
0x06	FPLL_FRA2	FPLL fraction[7:0]
0x07	–	Reserved
0x08	I2S_TX_CTRL0	I²S transmitter control 0
0x09	I2S_TX_CTRL1	I²S transmitter control 1
0x0A	I2S_RX_CTRL0	I²S receiver control 0
0x0B	I2S_RX_CTRL1	I²S receiver control 1
0x0C–0x0E	–	Reserved
0x0F	I2C_ALTET_ADDR	I²C device alternate address
0x10	ADC_MIC_CTRL	ADC microphone bias control
0x11	ADC_CTRL0	ADC control 0
0x12	ADC_CTRL1	ADC control 1
0x13	ADC_CTRL2	ADC control 2
0x14	ADC_ZCU_CTRL	ADC zero-crossing control
0x15	ADC_Gain_CTRL_R	ADC right channel gain control
0x16	ADC_FILTER_R	ADC right channel digital filter
0x17	ADC_Gain_CTRL_L	ADC left channel gain control
0x18	ADC_FILTER_L	ADC left channel digital filter
0x19	ADC_ADJ	ADC adjustment
0x1A–0x2F	–	Reserved
0x30	DAC_CTRL0	DAC control 0
0x31	DAC_CTRL1	DAC control 1
0x32	DAC_PD	DAC power-down
0x33	DAC_GAIN	DAC gain

Offset	Name	Description
0x34	DAC_DEEMP	DAC de-emphasis
0x35	DAC_MUTE	DAC mute
0x36–0x3F	–	Reserved
0x40	AMP_CTRL	Audio amplifier control
0x41–0x5F	–	Reserved
0x60	DAC_ISO0	DAC ISO control 0
0x61	DAC_ISO1	DAC ISO control 1
0x62	DAC_ISO2	DAC ISO control 2

3.1 Phase-lock Loop (PLL)

The SNAUD01 accepts an MCLK input of 12 MHz that passes through a PLL to get a proper internal audio master clock required by the device. A highly programmable PLL supports proper operation of the codec at various sample rates with the limited MCLK frequencies available in the system.

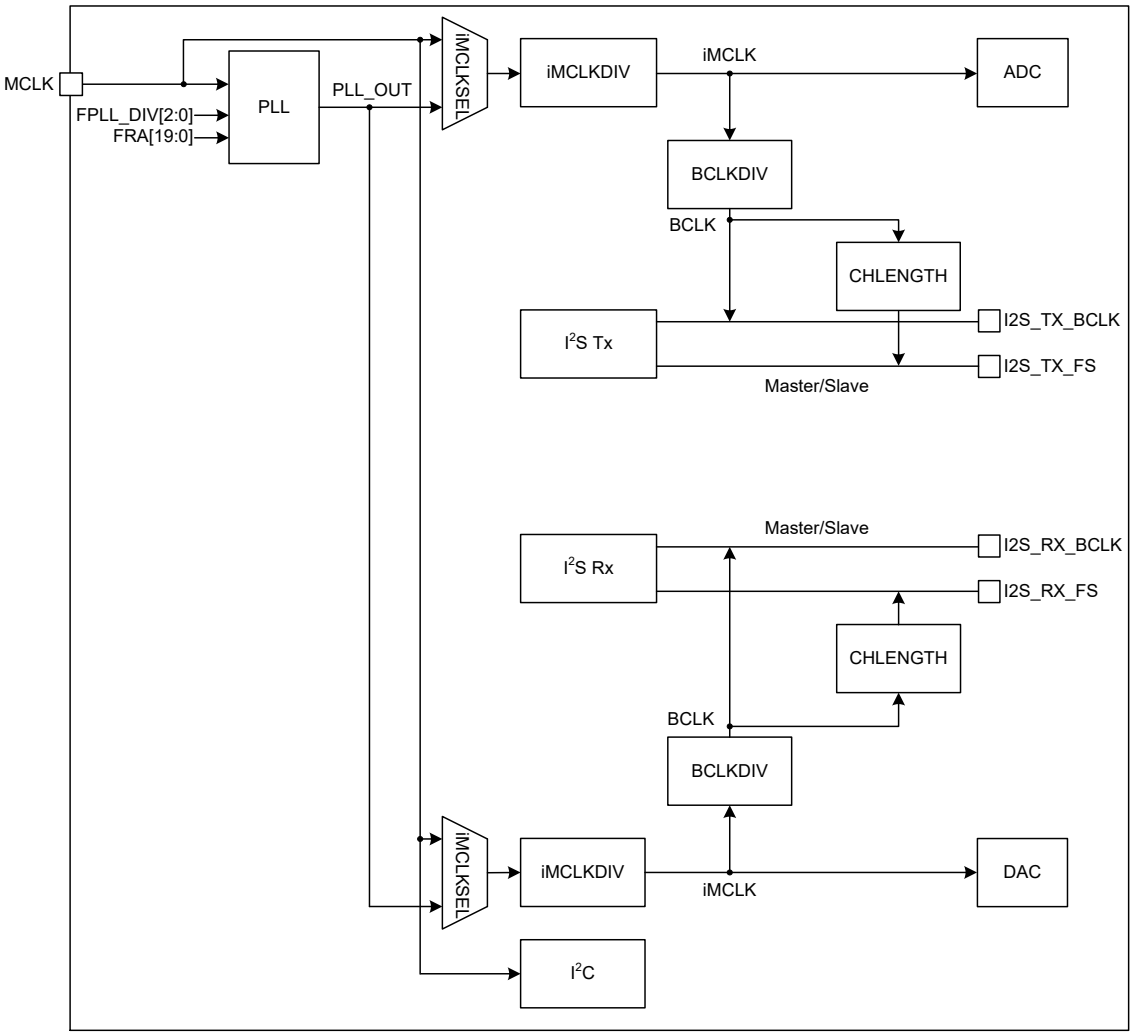


Figure 3–1 System Clock Block Diagram

The SNAUD01 supports standard audio sample rates of 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, and 48 kHz. FPLL_FRA, FPLL_DIV, iMCLKDIV, and BCLKDIV are register programmable. The formula for sample rate calculation is:

Sample Rate = (MCLK x ($FPLL_{INT\_FRA}$ / FPLL_DIV)) / (iMCLKDIV x BCLKDIV x CHLENGTH)

where

- MCLK = 12 MHz
- FPLL_INT = 9
- FPLL_FRA = 00000, 00001, …, FFFFE, or FFFFF
- $FPLL_{INT\_FRA}$ = FPLL_INT.FPLL_FRA
- FPLL_DIV = 9, 10, or 14
- iMCLKDIV = 1, 2, 4 ,6 ,8, 10, 12, or 14
- BCLKDIV = 2, 4, 6,…., or 512
- CHLENGTH = 64

The FPLL_INT is the integer portion of the $FPLL_{INT\_FRA}$ (the numbers to the left of the decimal point), and the FPLL_FRA is the fractional portion of the $FPLL_{INT\_FRA}$ (the numbers to the right of the decimal point, five digits of precision). CHLENGTH is the I^2S channel length.
Example 1:
For $FPLL_{INT\_FRA}$ = 9.216, FPLL_INT = 9, set FPLL_FRA = 374BC
FRA: $3 \times 16^{-1} + 7 \times 16^{-2} + 4 \times 16^{-3} + B \times 16^{-4} + C \times 16^{-5} = 0.216$

Example 2:
MCLK = 12 MHz for sample rate of 48 kHz
Refer to Table 3–3, the corresponding PLL_OUT for sample rate of 48 kHz is 12.288 MHz.
Refer to Table 3–2, for PLL_OUT = 12.288 MHz, FPLL_INT = 9, set FPLL_FRA = 374BC and FPLL_DIV = 9.
Set iMCLKDIV = 1 and BCLKDIV = 4; BCLK = 12288 / 4

The tables provide examples of a typical MCLK rate followed by different ways to program the PLL for different sample rates.

Table 3–2 PLL Settings for Output Frequency

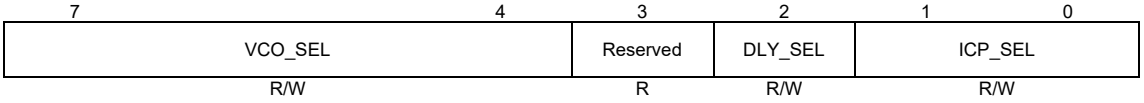
MCLK (MHz)	FPLL_INT (Hex)	FPLL_FRA (Hex)	FPLL_DIV	PLL_OUT (MHz)
12	9	374BC	9	12.288
12	9	6872B	10	11.2896

Table 3–3 Frequency Support for Sampling Rate

Sample Rate (kHz)	PLL_OUT (MHz)	iMCLKDIV	BCLKDIV	BCLK (kHz)
48	12.288	1	4	3072
32			6	2048
24			8	1536
16			12	1024
12			16	768
8			24	512
44.1	11.2896		4	2822.4
22.05			8	1411.2
11.025			16	705.6

3.1.1 FPLL Control (FPLL_CTRL)

Initial Value: 0x46



LEGEND: R = Read only; R/W = Read/Write

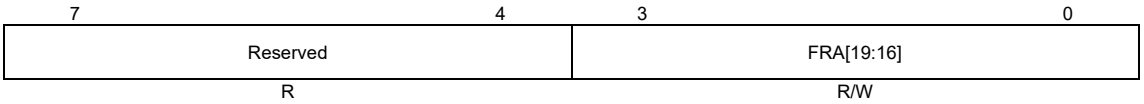
Figure 3–2 FPLL Control Register Map

Table 3–4 FPLL Control Register Description

Offset: 0x01		
Bit	**Field**	**Description**
7:4	VCO_SEL	Voltage control oscillator gain tuning. 0000: Low gain 1000: High gain Others: Reserved
3	–	Reserved
2	DLY_SEL	Phase frequency detector pulse delay. 0: Short pulse, 350 ps 1: Long pulse, 650 ps (default)
1:0	ICP_SEL	Charge pump current select. 00: ICP = 2.5 µA 01/10 (default): ICP = 5.0 µA 11: ICP = 7.5 µA

3.1.2 FPLL Fraction0 (FPLL_FRA0)

Initial Value: 0x03



LEGEND: R = Read only; R/W = Read/Write

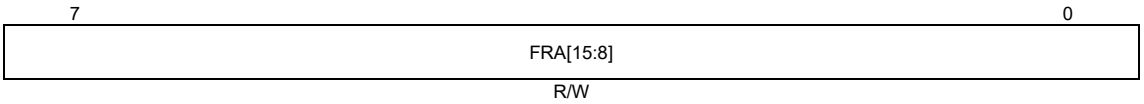
Figure 3–3 FPLL Fraction0 Register Map

Table 3–5 FPLL Fraction0 Register Description

Offset: 0x04		
Bit	**Field**	**Description**
7:4	–	Reserved
3:0	FRA[19:16]	Values of FPLL fraction[19:16]

3.1.3 FPLL Fraction1 (FPLL_FRA1)

Initial Value: 0x74



LEGEND: R = Read only; R/W = Read/Write

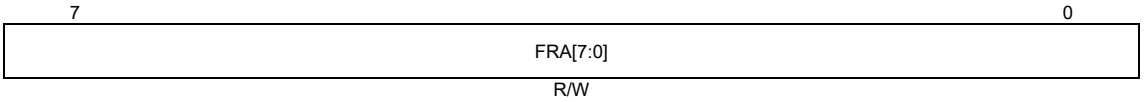
Figure 3–4 FPLL Fraction1 Register Map

Table 3–6 FPLL Fraction1 Register Description

Offset: 0x05		
Bit	**Field**	**Description**
7:0	FRA[15:8]	Values of FPLL fraction[15:8]

3.1.4 FPLL Fraction2 (FPLL_FRA2)

Initial Value: 0xBC



LEGEND: R = Read only; R/W = Read/Write

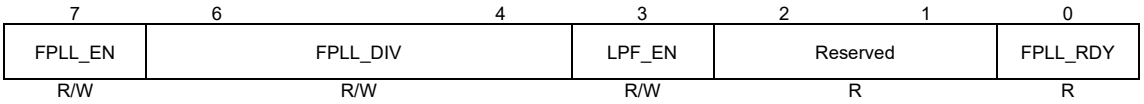
Figure 3–5 FPLL Fraction2 Register Map

Table 3–7 FPLL Fraction2 Register Description

Offset: 0x06		
Bit	**Field**	**Description**
7:0	FRA[7:0]	Values of FPLL fraction[7:0]

3.1.5 Master Clock Control (MCLK_CTRL)

Initial Value: 0x08



LEGEND: R = Read only; R/W = Read/Write

Figure 3–6 Master Clock Control Register Map

Table 3–8 Master Clock Control Register Description

Offset: 0x00		
Bit	**Field**	**Description**
7	FPLL_EN	FPLL enable. 0: Disable 1: Enable
6:4	FPLL_DIV	FPLL fraction denominator. 000: 9 001: 10 010: 14 Others: None
3	LPF_EN	Low pass filter enable (cut-off frequency at 20 MHz to filter input system clock). 0: Disable 1: Enable
2:1	–	Reserved
0	FPLL_RDY	FPLL ready; 1 represents FPLL ready.

3.2 LDO Regulator (LDO_CTRL)

The 3.3V regulator can deliver up to 150 mA of current while consuming 3.0 μA of quiescent current (typical). The input operating voltage range is specified from 3.3V to 5.5V, making it a suitable choice for two to three primary cell battery-powered applications. Figure 3–7 and Figure 3–8 show the curve charts of the regulator output voltage corresponding to each input operating voltage with different load currents.

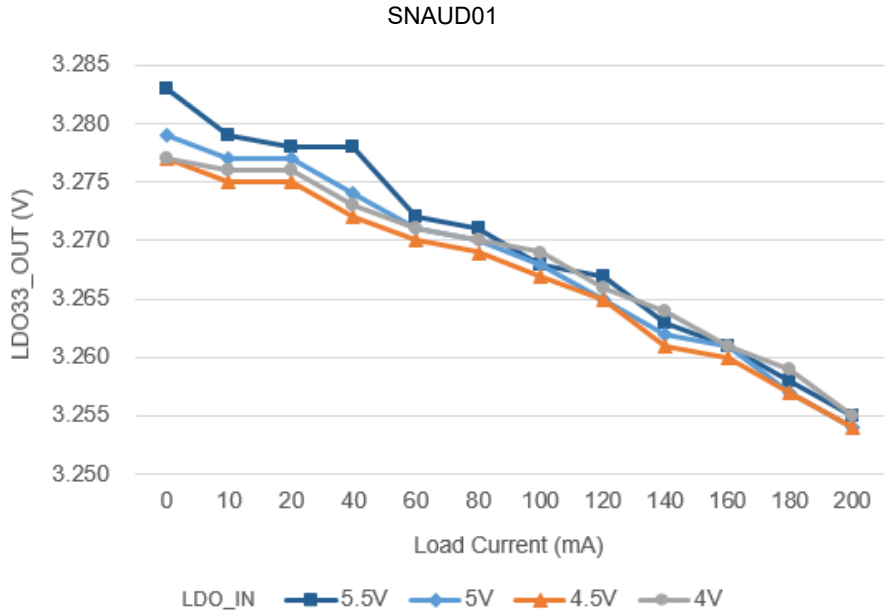


Figure 3–7 Regulator Output Curve Chart for 4–5.5V Input

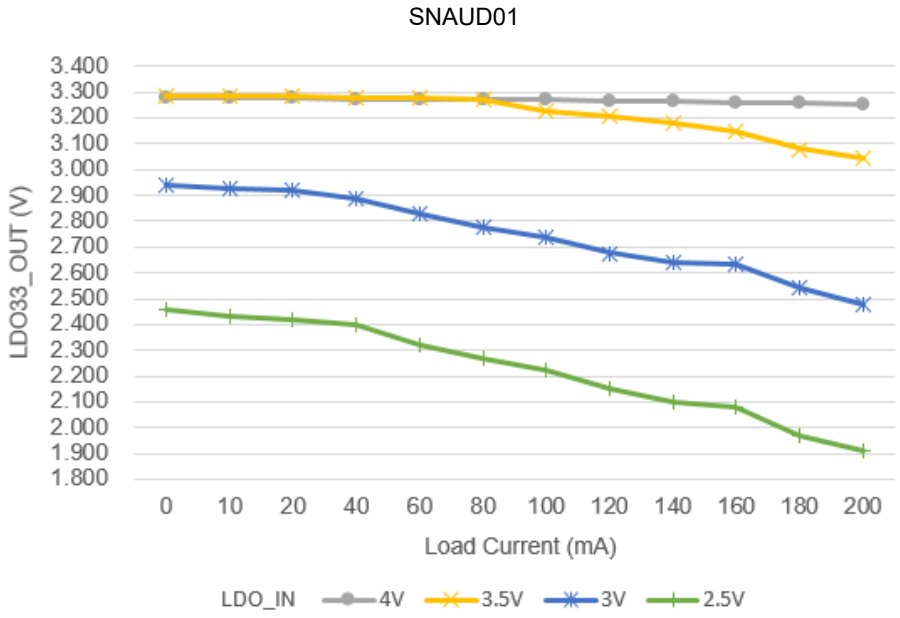


Figure 3–8 Regulator Output Curve Chart for 2.5–4V Input

The LDO output is dedicated for the I/O interface and able to share the output to the host. The 1.8V regulator with the driver current of 30 mA is dedicated for the ADC/digital logic circuit, and not allowed to share the output of the 1.8V regulator due to the sensitivity of the ADC.

Initial Value: 0x00

7	2	1	0
Reserved		LDO18_ Chopper_Sel	LDO18_ Chopper_En
R		R/W	R/W

LEGEND: R = Read only; R/W = Read/Write

Figure 3–9 LDO Regulator Control Register Map

Table 3–9 LDO Regulator Control Register Description

Offset: 0x02		
Bit	**Field**	**Description**
7:2	–	Reserved
1	LDO18_Chopper_Sel	LDO18 chopper select for frequency around 500 kHz. 0: /24 if the system clock = 12 MHz, 12.288 MHz, or 11.2896 MHz 1: /16 if the system clock = 8.192 MHz
0	LDO18_Chopper_En	LDO18 chopper enable. 0: Disable 1: Enable

TIP Enabling the LDO18 chopper offers a more stabilized LDO18 output.

3.3 I²S (I2S)

The I²S interface is configurable as the master or the slave by register setting, I2S_TX_CTRL0 and I2S_RX_CTRL0. In the master mode, the setting interface outputs the Frame Sync (FS), also known as Word Select (WS), and the audio data bit clock (BCLK) to control the data transfer. In the slave mode, an external controller is necessary to provide BCLK and FS/WS to SNAUD01. Data are latched on the rising edge of BCLK.

When not transmitting data, the I2S_TX_DOUT is pulled high by default. When the time slot function is enabled as shown below, there are additional output state modes such as the controlled tri-state capability. The features of the I²S includes:

- Operates as the master or the slave
- Handles up to 32-bit data length
- Standard I²S
- Stereo audio data

The figure below shows the block diagrams of the I²S interface in master mode and slave mode.

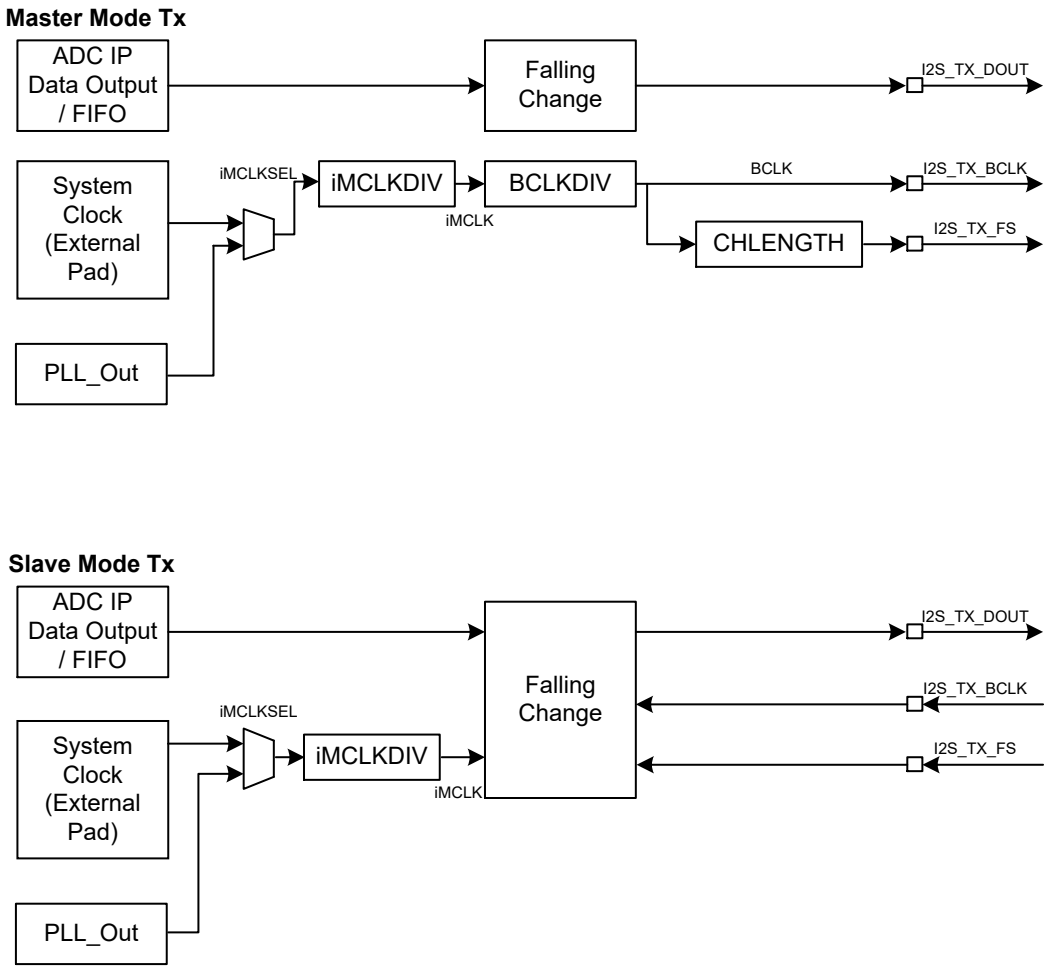


Figure 3–10 I²S Transmitter Block Diagram

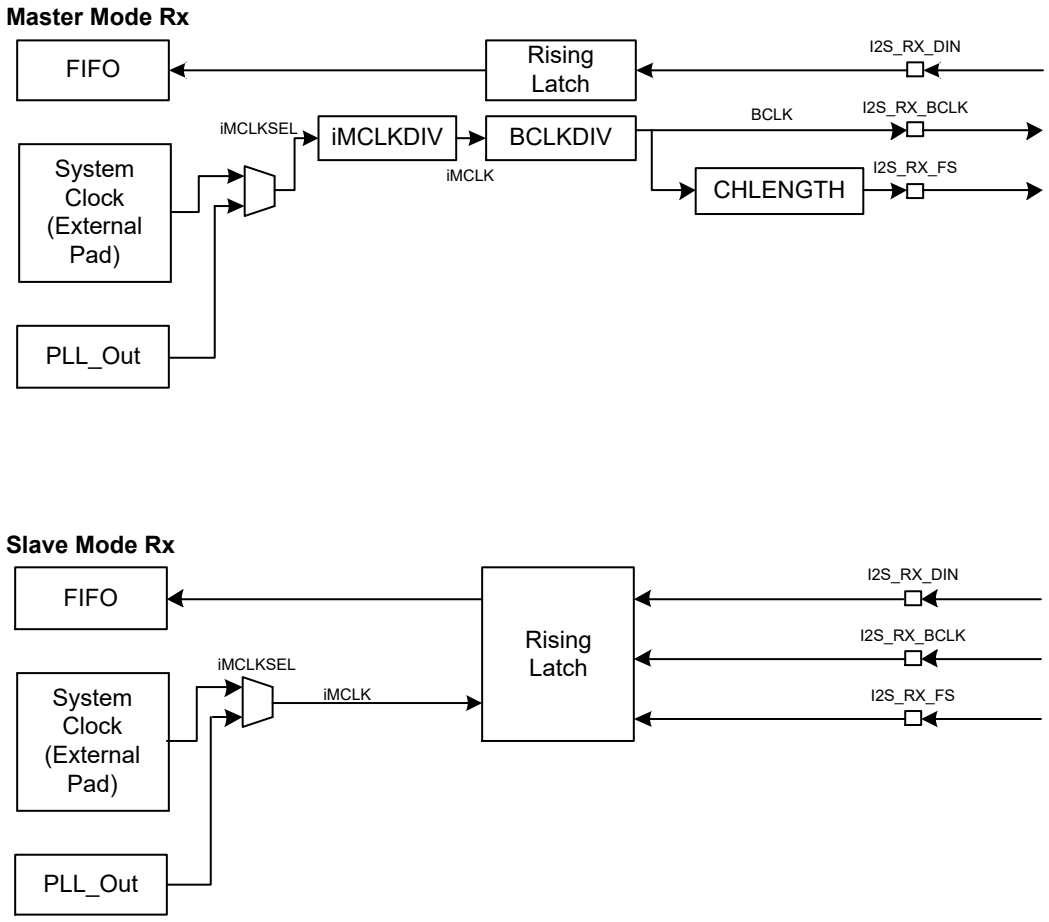


Figure 3–11 I²S Receiver Block Diagram

3.3.1 I²S Tx Control 0 (I2S_TX_CTRL0)

Initial value: 0x00

7	5	4	2	1	0
iMCLKDIV		Reserved		iMCLKSEL	MS
R/W		R		R/W	R/W

LEGEND: R = Read only; R/W: Read/Write

Figure 3–12 I²S Tx Control 0 Register Map

Table 3–10 I²S Tx Control 0 Register Description

Offset: 0x08		
Bit	**Field**	**Description**
7:5	iMCLKDIV[2:0]	iMCLK divider (only MS = 0 is valid). 0: iMCLK = iMCLK select source 1: iMCLK = iMCLK select source / 2 2: iMCLK = iMCLK select source / 4 … 7: iMCLK = iMCLK select source / 14
4:2	–	Reserved
1	iMCLKSEL	iMCLK select.

Offset: 0x08		
Bit	**Field**	**Description**
		0: iMCLK of I2S_ TX from the external MCLK Pad 1: iMCLK of I2S_ TX from the internal PLL output
0	MS	I^2S Tx mode select. 0: Slave mode 1: Master mode

3.3.2 I^2S Tx Control 1 (I2S_TX_CTRL1)

The settings in I^2S Tx Control 1 is effective in master mode only.

Initial value: 0x00

7							0
BCLKDIV							
R/W							

LEGEND: R = Read only; R/W: Read/Write

Figure 3–13 I^2S Tx Control 1 Register Map

Table 3–11 I^2S Tx Control 1 Register Description

Offset: 0x09		
Bit	**Field**	**Description**
7:0	BCLKDIV	BCLK divider (for master mode only). 0: BCLK = iMCLK / 2 1: BCLK = iMCLK / 4 2: BCLK = iMCLK / 6 3: BCLK = iMCLK / 8 … *n*: BCLK = iMCLK / (2**n* + 2); 0 ≦ *n* ≦ 255

3.3.3 I^2S Rx Control 0 (I2S_ RX _CTRL0)

Initial value: 0x00

7	6	5	4	3	2	1	0
iMCLKDIV			Reserved			iMCLKSEL	MS
R/W			R			R/W	R

LEGEND: R = Read only; R/W: Read/Write

Figure 3–14 I^2S Rx Control 0 Register Map

Table 3–12 I^2S Rx Control 0 Register Description

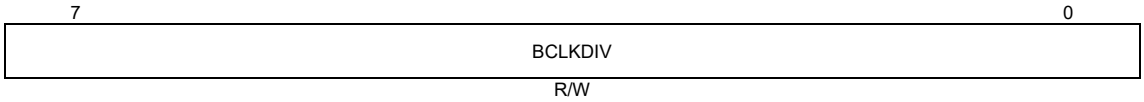
Offset: 0x0A		
Bit	**Field**	**Description**
7:5	iMCLKDIV[2:0]	iMCLK divider (only MS = 0 is valid). 0: iMCLK = iMCLK select source 1: iMCLK = iMCLK select source / 2 2: iMCLK = iMCLK select source / 4 … 7: iMCLK = iMCLK select source / 14
4:2	–	Reserved
1	iMCLKSEL	iMCLK select. 0: From external MCLK pad

Offset: 0x0A		
Bit	**Field**	**Description**
		1: From internal PLL output
0	MS	Mode select. 0: Slave mode 1: Master mode

3.3.4 I²S Rx Control 1 (I2S_RX_CTRL1)

The settings in I²S Rx Control 1 is effective in master mode only.

Initial value: 0x00



LEGEND: R = Read only; R/W: Read/Write

Figure 3–15 I²S Rx Control 1 Register Map

Table 3–13 I²S Rx Control 1 Register Description

Offset: 0x0B		
Bit	**Field**	**Description**
7:0	BCLKDIV	BCLK divider; BCLK = iMCLK / BCLKDIV. 0: 2 1: 4 2: 6 3: 8 … *n*: 2**n* + 2, 0 ≦ n ≦ 255

3.3.5 Audio Format

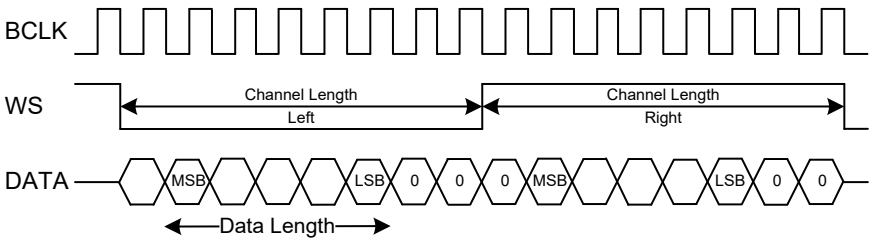


Figure 3–16 I²S Timing when Channel Length > Data Length

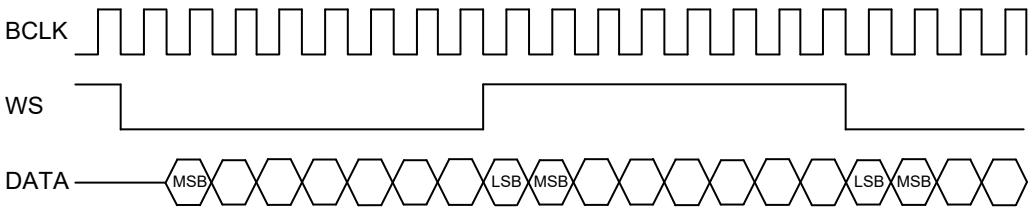


Figure 3–17 I²S Timing when Channel Length = Data Length

3.4 I²C (I2C_ALTET_ADDR)

The inter-integrated circuit (I²C) interface of the SNAUD01 implements the standard I²C slave function and complies with the I²C-bus Specification. It serves as a slave to respond to requests. The I²C is a two-wire bidirectional serial bus that provides a simple and efficient method of data exchange while minimizing the interconnection requirements between devices.

The SNAUD01 I²C communicates with external I²C devices with two pins, serial clock (SCL) and serial data (SDA). It supports bit rates of up to 800 kbps. The SNAUD01 I²C has one set of I²C controller with two pins, SCL and SDA, and is at base address 0x32.

Features of the I²C include:

- Slave transmit/receive functionality
- Arbitration handled between simultaneously transmitting masters without corruption of serial data on the bus
- Programmable clock allowing adjustment of I²C transfer rates
- Bidirectional data transfer
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization as a handshake mechanism to suspend and resume serial transfer
- Generation and detection of 7-bit addressing and general call
- Timeout function will reset I²C if the system is under operation and don't receive 9 clocks in 90ms.

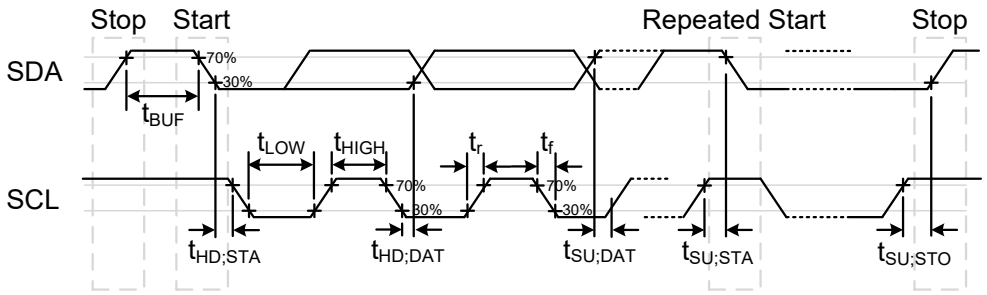


Figure 3–18 I²C Receive Timing

Table 3–14 Timing Requirements for I²C

Symbol	Parameter	Device				Unit
		Standard Mode		Fast Mode		
		MIN.	MAX.	MIN.	MAX.	
$t_{SU;STA}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7	–	0.6	–	µs
$t_{HD;STA}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4	–	0.6	–	
t_{LOW}	Pulse duration, SCL low	4.7	–	1.3	–	
t_{HIGH}	Pulse duration, SCL high	4	–	0.6	–	
$t_{SU;DAT}$	Setup time, SDA valid before SCL high	250	–	100	–	
$t_{HD;DAT}$	Hold time, SDA valid after SCL low	0	3.45	0	0.9	
t_{BUF}	Pulse duration, SDA high between STOP and START conditions	4.7	–	1.3	–	
t_r	Rise time, SCL	–	1000	20 + 0.1C_b	300	ns
t_f	Fall time, SCL	–	300	20 + 0.1C_b	300	
$t_{SU;STO}$	Setup time, SCL high before SDA high (for STOP condition)	4	–	0.6	–	µs

An acknowledge (ACK), a software convention, is used to indicate a successful data transfer. To allow for the ACK response, the transmitting device releases the SDIO bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDIO line LOW to acknowledge the reception of the eight bits of data.
Following a START condition, the master must output a device address byte. This consists of a 7-bit device address, and the LSB of the device address byte is the R/W (Read/Write) control bit. When R/W = 1, this indicates the master is initiating a read operation from the slave device, and when R/W = 0, the master is initiating a write operation to the slave device. If the device address matches the address of the slave device, the slave will output an ACK during the period when the master allows for the ACK signal.

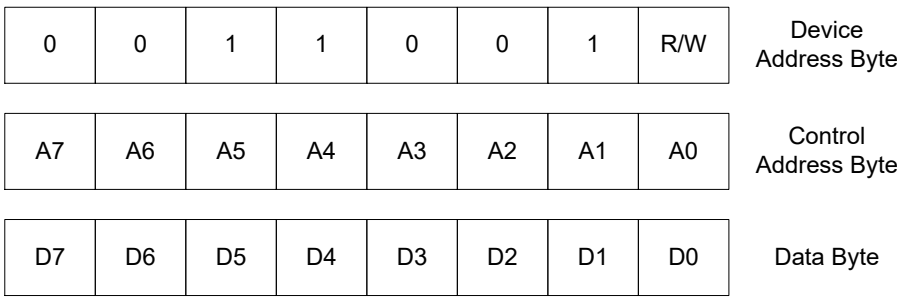


Figure 3–19 I²C Address/Data Format

Initial value: 0x00

7	1	0
Device Address ID		Alter_ ID_TRG
R		R/W

LEGEND: R = Read only; R/W: Read/Write

Figure 3–20 Alternate I²C Address ID Register (0x0F)

Table 3–15 Alternate I²C Address ID Register Description

Offset: 0x0F		
Bit	**Field**	**Description**
7:1	Device Address ID	I²C device address ID.
0	Alter_ID_TRG	I²C alternate device ID trigger; set 1 to trigger.

3.4.1 Alternate I²C Address Register Trigger (I2C_ALT_ID_TRG)

The I²C of the SNAUD01 operates only in slave mode. The device address value is 0x32 by default. An alternate address becomes available with settings of six I/O pins (high or low). After setting the trigger bit, I2C_ALT_ID_TRG (0x0F) as 1, the alternate ID register latches six I²S pins as its 6-bit address data.

I2S_TX_ DOUT	I2S_TX_ BLCK	I2S_TX_ FS	I2S_RX_ DIN	I2S_RX_ BLCK	I2S_RX_ FS	1	0

Figure 3–21 Setting Pins of Alternate 6-bit Address Data

3.4.2 Scenario

Use two SNAUD01BMJGs (SNAUD01BMJG-1 and SNAUD01BMJG-2) for surround sound multi-channel recording by following the steps below. Fine-tune the gain of the PGA corresponding to different acoustic environment. Set the value of the gain inversely proportional to the noise decibels of the environment. The louder the environment is, the lower the gain should be.

STEP 1 Change the ID for at least one of the SNAUD01BMJG.
Avoid the setting of I²C command causing the two SNAUD01BMJGs operating at the same time, set the alternate IDs as 0x02 (00000010h) and 0x06 (00000110h).

STEP 2 Connect GPO1 and I2S_RX_FS from SNAUD01BMJG-2 as shown in the figure below.

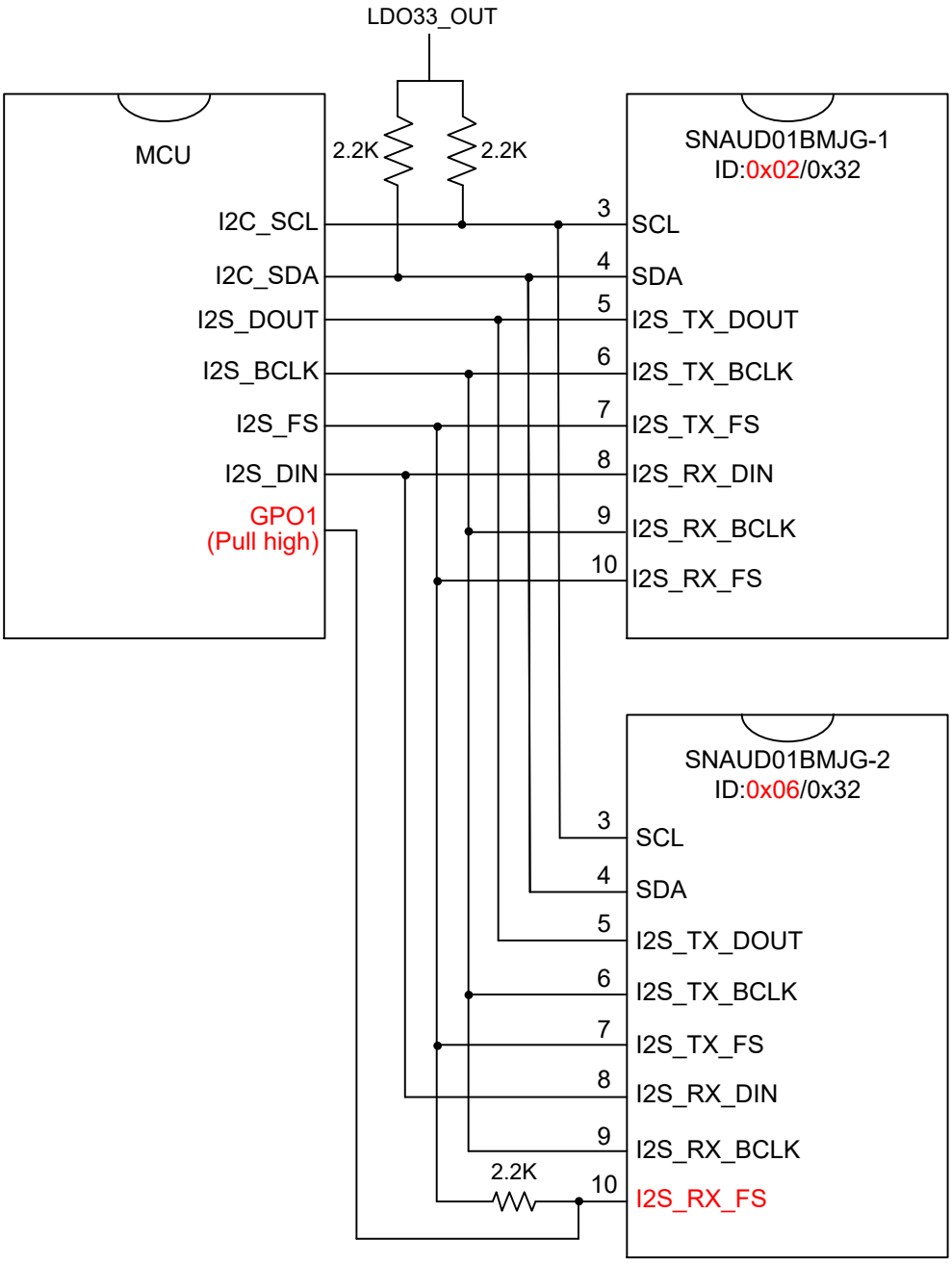


Figure 3–22 Connection of I²S pins for I²C ID Rename

STEP 3 Set GPO1 high and trigger the alternate I²C address register (Reg 0x0F = 0x01). The ID of SNAUD01BMJG-1 is 0x02/0x32 and the ID of SNAUD01BMJG-2 is 0x06/0x32.

STEP 4 Set the gain of the PGA of the SNAUD01BMJG-1 (Reg 0x15) by using the new ID 0x02 (or the default ID, 0x32).

STEP 5 Set the gain of the PGA of the SNAUD01BMJG-2 (Reg 0x17) by using the new ID 0x06.

STEP 6 Connect the I²S pins of the MCU and the I²S pins of the SNAUD01BMJG-1 and SNAUD01BMJG-2.

3.5 Sigma Delta ADC

3.5.1 ADC MIC Bias Control (ADC_MIC_CTRL)

Initial value: 0xD8

7	6	5	3	2	1	0
SEL_IB		SEL_MICB		CHOPPER_SEL		MICBIAS_EN
R/W		R/W		R/W		R/W

LEGEND: R = Read only; R/W: Read/Write

Figure 3–23 ADC MIC Bias Control Register Map

Table 3–16 ADC MIC Bias Control Register Description

Offset: 0x10		
Bit	**Field**	**Description**
7:6	SEL_IB	ADC reference bias current select for left and right channel. 00: 2.5 µA 01: 3.3 µA 10: 3.3 µA 11: 5 µA (default)
5:3	SEL_MICB	Microphone bias output select. 000: 1.83 x VMID 001: 2.2 x VMID 010: 2.38 x VMID 011: 2.56 x VMID (default) 100: 2.75 x VMID 101: 3.12 x VMID 110: 3.3 x VMID 111: High impedance VMID = LDO18 / 2
2:1	CHOPPER_SEL	Channel chopper frequency select for left and right channel. 00: Divide by 2 (default) 01: Divide by 4 10: Divide by 8 11: Disable chopper
0	MICBIAS_EN	Microphone bias enable output for left and right channel, active high. 0: Disable 1: Enable

3.5.2 ADC Control 0 (ADC_CTRL0)

Initial value: 0x00

7	6	5	4	3	2	1	0
ADC_EN_L	MICBT_EN_L	PGA_EN_L	DEMPD_L	ADC_EN_R	MICBT_EN_R	PGA_EN_R	DEMPD_R
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R = Read only; R/W: Read/Write

Figure 3–24 ADC Control 0 Register Map

Table 3–17 ADC Control 0 Register Description

Offset: 0x11		
Bit	**Field**	**Description**
7	ADC_EN_L	Left channel of ADC power-on enable, active high. 0: Disable 1: Enable When ADC is on, VMID is enabled.
6	MICBT_EN_L	Left channel of microphone boost power-on enable, active high. 0: Disable

Offset: 0x11		
Bit	**Field**	**Description**
		1: Enable
5	PGA_EN_L	Left channel of PGA power-on enable, active high. 0: Disable 1: Enable
4	DEMPD_L	Left channel of dynamic element matching[3] (DEM) disable, active high. 0: Disable 1: Enable
3	ADC_EN_R	Right channel of ADC power-on enable, active high. 0: Disable 1: Enable When ADC is on, VMID is enabled.
2	MICBT_EN_R	Right channel of microphone boost power-on enable, active high. 0: Disable 1: Enable
1	PGA_EN_R	Right channel of PGA power-on enable, active high. 0: Disable 1: Enable
0	DEMPD_R	Right channel of DEM disable, active high. 0: Disable 1: Enable

3.5.3 ADC Control 1 (ADC_CTRL1)

Initial value: 0x11

7	6	5	4	3	2	1	0
IREF_EN_L	VREF_EN_L	CK_EN_L	PGA_L_Mute	IREF_EN_R	VREF_EN_R	CK_EN_R	PGA_R_Mute
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R = Read only; R/W: Read/Write

Figure 3–25 ADC Control 1 Register Map

Table 3–18 ADC Control 1 Register Description

Offset: 0x12		
Bit	**Field**	**Description**
7	IREF_EN_L	Left channel of IREF circuit enable, active high. 0: Disable 1: Enable
6	VREF_EN_L	Left channel of VREF circuit enable, active high. 0: Disable 1: Enable
5	CK_EN_L	Left channel of CKGEN enable, active high. 0: Disable 1: Enable
4	PGA_L_Mute	Left channel of PGA mute enable. 0: Disable 1: Enable
3	IREF_EN_R	Right channel of IREF circuit enable, active high. 0: Disable 1: Enable
2	VREF_EN_R	Right channel of VREF circuit enable, active high. 0: Disable 1: Enable
1	CK_EN_R	Right channel of CKGEN enable, active high. 0: Disable 1: Enable
0	PGA_R_Mute	Right channel of PGA mute enable.

[3] Improves the signal-to-noise ratio (SNR)

Offset: 0x12		
Bit	**Field**	**Description**
		0: Disable 1: Enable

3.5.4 ADC Control 2 (ADC_CTRL2)

Initial value: 0x20

7	6	5	4	3	1	0
GAIN_SYNC	FS_SET	SOFT_RSTN	I_SEL_MIX_MIC_L	Reserved		I_SEL_MIX_MIC_R
R/W	R/W	R/W	R/W	R		R/W

LEGEND: R = Read only; R/W: Read/Write

Figure 3–26 ADC Control 2 Register Map

Table 3–19 ADC Control 2 Register Description

Offset: 0x13		
Bit	**Field**	**Description**
7	GAIN_SYNC	Left and right channel of PGA gain sync enable. 0: Disable 1: Enable
6	FS_SET	Full scale setting, compensate digital/analog attenuated gain to meet the full scale requirement. 0: No compensation 1: Compensate
5	SOFT_RSTN	Software reset digital circuit; low reset. One MCLK pulse trigger. Default = 1
4	I_SEL_MIX_MIC_L	Left channel microphone input path to mixer enable. 0: Disable 1: Enable
3:1	–	Reserved
0	I_SEL_MIX_MIC_R	Right channel microphone input path to mixer enable. 0: Disable 1: Enable

3.5.5 ADC Zero-crossing Control (ADC_ZCU_CTRL)

Initial value: 0x00

7	6	5	4	3	2	1	0
Reserved	ZCU_TO_L	ZCU_TRI_L	ZCU_L	Reserved	ZCU_TO_R	ZCU_TRI_R	ZCU_R
R	R/W	R	R/W	R	R/W	R	R/W

LEGEND: R = Read only; R/W: Read/Write

Figure 3–27 ADC Zero-crossing Control Register Map

Table 3–20 ADC Zero-crossing Control Register Description

Offset: 0x14		
Bit	**Field**	**Description**
7	–	Reserved
6	ZCU_TO_L	Left channel zero-crossing update time out. 0: 20 Hz 1: 5 Hz
5	ZCU_TRI_L	Host polling this bit, check if the signal of left channel of ADC is in zero-crossing state. After the signal crossing zero state, the hardware sets this bit to “1”. When the host sets PGA gain, clear this bit to “0” (except for the

Offset: 0x14		
Bit	**Field**	**Description**
		boost gain). Since the default value is uncertain, set PGA first before reading this bit.
4	ZCU_L	Left channel zero-crossing update enable. 0: Disable 1: Enable
3	–	Reserved
2	ZCU_TO_R	Right channel zero-crossing update time out. 0: 20 Hz 1: 5 Hz
1	ZCU_TRI_R	Host polling this bit, check if the signal of right channel of ADC is in zero-crossing state. After the signal crossing zero state, the hardware sets this bit to "1". When the host sets PGA gain, clear this bit to “0” (except for the boost gain). Since the default value is uncertain, set PGA first before reading this bit.
0	ZCU_R	Right channel zero-crossing update enable. 0: Disable 1: Enable

3.5.6 ADC Right Channel Gain Control (ADC_Gain_CTRL_R)

Initial value: 0x10

7	6	5	0
BOOST_VAL_R		PGA_VAL_R	
R/W		R/W	

LEGEND: R = Read only; R/W: Read/Write

Figure 3–28 ADC Right Channel Gain Control Register Map

Table 3–21 ADC Right Channel Gain Control Register Description

Offset: 0x15		
Bit	**Field**	**Description**
7:6	BOOST_VAL_R	Boost amplifier gain adjust for right channel of ADC. 00: +0 dB 01: +20 dB 10: +40 dB 11: +50 dB
5:0	PGA_VAL_R	Programmable gain adjust for right channel of ADC, -12 dB to 35.25 dB, step = 0.75 dB. 000000: -12 dB 000001: -11.25 dB … 010000: 0 dB … 111110: +34.5 dB 111111: +35.25 dB

3.5.7 ADC Right Channel Digital Filter (ADC_FILTER_R)

Initial value: 0x00

7	6	5	4	3 ... 0
IIRHPF_OFF	Reserved	FILTER_OFF	ADCHPD	HPGAIN
R/W	R	R/W	R/W	R/W

LEGEND: R = Read only; R/W: Read/Write

Figure 3–29 ADC Right Channel Digital Filter Register Map

Table 3–22 ADC Right Channel Digital Filter Register Description

Offset: 0x16		
Bit	**Field**	**Description**
7	IIRHPF_OFF[4]	HPF function for DC cancellation. 0: Enable 1: Disable
6	–	Reserved
5	FILTER_OFF[5]	4 kHz low pass filter function for noise suppression. 0: Enable 1: Disable
4	ADCHPD[6]	High pass filter function for offset cancellation. 0: Enable 1: Disable
3:0	HPGAIN[7]	Value of high pass gain.

I. High Pass Filter Frequency Response

The frequency ranges of the high pass filter corresponding to the values of HPGAIN from 0 to 15 are shown in the figure below, and Table 3–23 lists the cutoff frequencies at minus 3 dB of the nominal passband value.

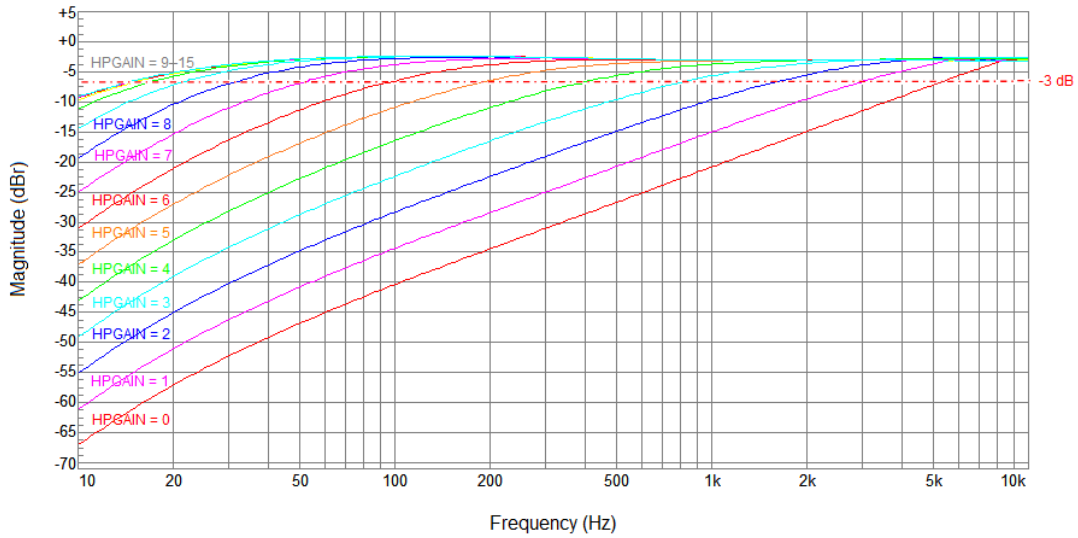


Figure 3–30 High Pass Filter Frequency Response Curve Chart

[4] Filters the DC gain generated during recording.
[5] For vocal recording
[6] Filters low frequency noises such as the sound of the wind.
[7] The louder the low frequency noise is, the lower the gain should be.

Table 3–23 Cutoff Frequency

High Pass Gain Value	Cutoff Frequency at -3 dB (Hz)
0	5376.7
1	3017.6
2	1619.6
3	829.7
4	403.7
5	194.7
6	97.3
7	52.4
8	31.6
9	21.7
10	17.3
11	15.6
12	15.0
13–15	14.9

3.5.8 ADC Left Channel Gain Control (ADC_Gain_CTRL_L)

Initial value: 0x10

7	6	5	0
BOOST_VAL_L		PGA_VAL_L	
R/W		R/W	

LEGEND: R = Read only; R/W: Read/Write

Figure 3–31 ADC Left Channel Gain Control Register Map

Table 3–24 ADC Left Channel Gain Control Register Description

Offset: 0x17		
Bit	**Field**	**Description**
7:6	BOOST_VAL_L	Boost amplifier gain adjust for left channel of ADC. 00: +0 dB 01: +20 dB 10: +40 dB 11: +50 dB
5:0	PGA_VAL_L	Programmable gain adjust for left channel of ADC, -12 dB to 35.25 dB, step = 0.75 dB. 000000: -12 dB 000001: -11.25 dB … 010000: 0 dB … 111110: +34.5 dB 111111: +35.25 dB

3.5.9 ADC Left Channel Digital Filter (ADC_FILTER_L)

Initial value: 0x00

7	6	5	4	3	0
IIRHPF_OFF	Reserved	FILTER_OFF	ADCHPD	HPGAIN	
R/W	R	R/W	R/W	R/W	

LEGEND: R = Read only; R/W: Read/Write

Figure 3–32 ADC Left Channel Digital Filter Register Map

Table 3–25 ADC Left Channel Digital Filter Register Description

Offset: 0x18		
Bit	**Field**	**Description**
7	IIRHPF_OFF[4]	HPF function for DC cancellation. 0: Enable 1: Disable
6	–	Reserved
5	FILTER_OFF[5]	4 kHz low pass filter function for noise suppression. 0: Enable 1: Disable
4	ADCHPD[6]	High pass filter function for offset cancellation. 0: Enable 1: Disable
3:0	HPGAIN[7]	Value of high pass gain.

I. High Pass Filter Frequency Response

Refer to High Pass Filter Frequency Response in 3.5.7.

3.5.10 ADC Adjustment (ADC_ADJ)

Initial value: 0x00

7	5	4	3	1	0
Reserved		FEEDBACK_R[0]	Reserved		FEEDBACK_L[0]
R		R/W	R		R/W

LEGEND: R = Read only; R/W: Read/Write

Figure 3–33 ADC Adjustment Register Map

Table 3–26 ADC Adjustment Register Description

Offset: 0x19		
Bit	**Field**	**Description**
7:5	–	Reserved
4	FEEDBACK_R[0]	Common-mode feedback ratio adjust for right channel of microphone boost. 0: Normal 1: Enhanced
3:1	–	Reserved
0	FEEDBACK_L[0]	Common-mode feedback ratio adjust for left channel of microphone boost. 0: Normal 1: Enhanced

3.6 DAC (DAC_CTRL)

3.6.1 DAC Control 0 (DAC_CTRL0)

Initial value: 0x00

7	6	5	4	3	2	1	0
SC_FLAG	SC_SEL[1:0]		SC_RST	SC_EN	HP_DRV_PERF[1:0]		ICK_INV
R	R/W		R/W	R/W	R/W		R/W

LEGEND: R = Read only; R/W: Read/Write

Figure 3–34 DAC Control 0 Register Map

Table 3–27 DAC Control 0 Register Description

Offset: 0x30		
Bit	**Field**	**Description**
7	SC_FLAG	Short circuit protect flag.
6:5	SC_SEL[1:0]	Short circuit protect select. 00: 6 ohm 01: 4 ohm 10: 2 ohm 11: 1 ohm
4	SC_RST	Short circuit protect flag reset; active high. Set this bit high for reset, then set to low.
3	SC_EN	Short circuit protect enable. 0: Disable 1: Enable
2:1	HP_DRV_PERF[1:0]	Headphone driver output buffer current select. 00: 0.84 mA 01: 3 mA 10: 5.1 mA 11: 7.24 mA
0	ICK_INV	Inverted I_CLK. 0: Normal 1: Inverted

3.6.2 DAC Control 1 (DAC_CTRL1)

Initial value: 0x01

7	6	5	4	3	2	1	0
LRCK_INV	BCK_INV	I2S_RL_SEL	Reserved		MUTE	DAC_EN_IN	SOFT_RSTN
R/W	R/W	R/W	R		R/W	R/W	R/W

LEGEND: R = Read only; R/W: Read/Write

Figure 3–35 DAC Control 1 Register Map

Table 3–28 DAC Control 1 Register Description

Offset: 0x31		
Bit	**Field**	**Description**
7	LRCK_INV	I^2S left right channel clock invert enable. 0: Disable 1: Enable
6	BCK_INV	I^2S bit clock invert enable. 0: Disable 1: Enable
5	I2S_RL_SEL	I^2S data reload select. 0: Channel clock rising edge 1: Channel clock falling edge
4:3	–	Reserved
2	MUTE	Mute control. 0: Mute off 1: Mute on
1	DAC_EN_IN	DAC enable. 0: Disable 1: Enable
0	SOFT_RSTN	Software reset digital circuit; low reset. One MCLK pulse trigger. Default: 1

3.6.3 DAC ISO Control 0 (DAC_ISO0)

Initial value: 0x01

7 5	4	3	2	1	0
ISO_NOPOP_HP_SEL	ISO_IN_SELB	ISO_FAST_VREFSPK	ISO_PDB_VREFSPK	ISO_PDB_VCOM_BUF	ISO_PDB_IREF_VCOM
R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R = Read only; R/W: Read/Write

Figure 3–36 DAC ISO Control 0 Register Map

Table 3–29 DAC ISO Control 0 Register Description

Offset: 0x60		
Bit	**Field**	**Description**
7:5	ISO_NOPOP_HP_SEL [2:0]	Headphone output POP noise elimination.
4	ISO_IN_SELB	Left/right/VCOM headphone driver input mode select, active low.
3	ISO_FAST_VREFSPK	VREF_SPK charge mode. 0: Normal mode 1: Fast start-up
2	ISO_PDB_VREFSPK	VREF_SPK power-down, active low.
1	ISO_PDB_VCOM_BUF	Capless headphone driver VCOM buffer, active low.
0	ISO_PDB_IREF_VCOM	IREF circuit VCOM power-down, active low.

3.6.4 DAC ISO Control 1 (DAC_ISO1)

Initial value: 0x00

7	6	5	4	3	2	1 0
PDB_IREF_L	PDB_IREF_R	PDB_DRV_R	PDB_DRV_L	NOPOP_VREFSPK_SEL	LDO18_IREF_PD	SEL_IB[1:0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R = Read only; R/W: Read/Write

Figure 3–37 DAC ISO Control 1 Register Map

Table 3–30 DAC ISO Control 1 Register Description

Offset: 0x61		
Bit	**Field**	**Description**
7	PDB_IREF_L	IREFL circuit power-down, active low.
6	PDB_IREF_R	IREFR circuit power-down, active low.
5	PDB_DRV_R	Right channel headphone driver circuit power-down, active low.
4	PDB_DRV_L	Left channel headphone driver circuit power-down, active low.
3	NOPOP_VREF-SPK_SEL	VREFSPK connects to headphone driver output. 0: Not connect 1: Connect
2	LDO18_IREF_PD	LDO18 bandgap control. 0: Turn on even if the PMU enters the power-down mode. 1: Power down
1:0	SEL_IB[1:0]	Internal bias current select. 00: 50 μA 01: 60 μA 10: 30 μA 11: 40 μA

3.6.5 DAC ISO Control 2 (DAC_ISO2)

Initial value: 0x00

7	...	2	1	0
Reserved			D2S_PD_R	D2S_PD_L
R			R/W	R/W

LEGEND: R = Read only; R/W: Read/Write

Figure 3–38 DAC_ISO Control 2 Register Map

Table 3–31 DAC_ISO Control 2 Register Description

Offset: 0x62		
Bit	**Field**	**Description**
7:2	–	Reserved
1	D2S_PD_R	Right channel of differential to singled-ended output buffer power-down enable, active low. 0: Enable 1: Disable
0	D2S_PD_L	Left channel of differential to singled-ended output buffer power-down enable, active low. 0: Enable 1: Disable

3.6.6 DAC Power-down Control (DAC_PD)

Initial value: 0xEE

7	6	5	4	3	2	1	0
PD_DACL	PD_ VMIDBUF_L	PD_CLK_L	PD_DEM_L	PD_DAC_R	PD_ VMIDBUF_R	PD_CLK_R	PD_DEM_R
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R = Read only; R/W: Read/Write

Figure 3–39 DAC Power-down Control Register Map

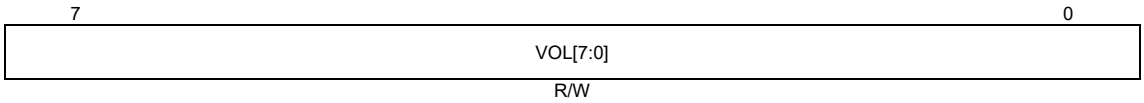
Table 3–32 DAC Power-down Control Register Description

Offset: 0x32		
Bit	**Field**	**Description**
7	PD_DACL	Left channel of DAC circuit power-down enable, active high. 0: Disable 1: Enable When DAC is on, VMID is enabled.
6	PD_VMIDBUF_L	Left channel of VMID buffer power-down enable, active high. 0: Disable 1: Enable
5	PD_CLK_L	Left channel of clock generator power-down enable, active high. 0: Disable 1: Enable
4	PD_DEM_L	Left channel of DEM power-down enable, active high. 0: Disable 1: Enable
3	PD_DAC_R	Right channel of DAC circuit power-down enable, active high. 0: Disable 1: Enable When DAC is on, VMID is enabled.
2	PD_VMIDBUF_R	Right channel of VMID buffer power-down enable, active high. 0: Disable 1: Enable
1	PD_CLK_R	Right channel of clock generator power-down enable, active high.

Offset: 0x32		
Bit	**Field**	**Description**
		0: Disable 1: Enable
0	PD_DEM_R	Right channel of DEM power-down enable, active high. 0: Disable 1: Enable

3.6.7 DAC Gain Control (DAC_GAIN)

Initial value: 0x00



LEGEND: R = Read only; R/W: Read/Write

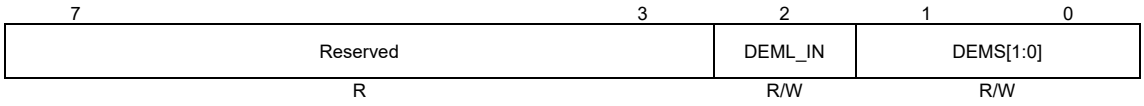
Figure 3–40 DAC Gain Control Register Map

Table 3–33 DAC Gain Control Register Description

Offset: 0x33		
Bit	**Field**	**Description**
7:0	VOL[7:0]	Digital volume control (hard macro) -96 dB to 0 dB, step = -0.375 dB. 00000000: 0 dB 00000001: -0.375 dB 00000010: -0.75 dB … 11111111: -96 dB

3.6.8 DAC De-emphasis Control (DAC_DEEMP)

Initial value: 0x00



LEGEND: R = Read only; R/W: Read/Write

Figure 3–41 DAC De-emphasis Control Register Map

Table 3–34 DAC De-emphasis Control Register Description

Offset: 0x34		
Bit	**Field**	**Description**
7:3	–	Reserved
2	DEML_IN	De-emphasis function enable. 0: Disable 1: Enable
1:0	DEMS[1:0]	DAC de-emphasis response curve select. 00: Reserved 01: De-emphasis for 48 kHz 10: De-emphasis for 44.1 kHz 11: De-emphasis for 32 kHz

3.6.9 DAC Mute Control (DAC_MUTE)

Initial value: 0x00

7	6	5	4	3	2	1	0
Reserved			MUTEB_L	Reserved			MUTEB_R
R			R/W	R			R/W

LEGEND: R = Read only; R/W: Read/Write

Figure 3–42 DAC Mute Control Register Map

Table 3–35 DAC Mute Control Register Description

Offset: 0x35		
Bit	**Field**	**Description**
7:5	–	Reserved
4	MUTEB_L	Left channel of headphone driver mute enable, active low. 0: Enable 1: Disable
3:1	–	Reserved
0	MUTEB_R	Right channel of headphone driver mute enable, active low. 0: Enable 1: Disable

3.7 Audio Amplifier (AMP_CTRL)

Initial value: 0x00

7	6	5	4	3	2	1	0
OPA_CE	OPA_VOL[4:0]					Reserved	OPA_Rdy
R/W	R/W					R	R

LEGEND: R = Read only; R/W: Read/Write

Figure 3–43 Audio Amplifier Control Register Map

Table 3–36 Audio Amplifier Control Register Description

Offset: 0x40		
Bit	**Field**	**Description**
7	OPA_CE	Operational amplifier enable. 0: Disable 1: Enable
6:2	OPA_VOL[4:0]	32-level volume control, -20 dB to +11 dB, step = 1 dB. 00000: -20 dB 00001: -19 dB … 10100: 0 dB … 11110: +10 dB 11111: +11 dB
1	–	Reserved
0	OPA_Rdy	Operational amplifier ready.

3.8 Configuration Sequence for Recording and Playback

The register configuration sequences for is to configure the PLL, LDO, and I²S registers to turn on the system first. The PLL register settings, FPLL_CRTL, FPLL_FRA0, FPLL_FRA1, and FPLL_FRA2, must be set before setting the MCLK_CTRL. Figure 3–44, Figure 3–45, and Figure 3–46 show the register control flow of the recording mode, AC-coupled playback mode, and capless playback mode using a 12 MHz clock source with sample rate of 48 kHz as an example.

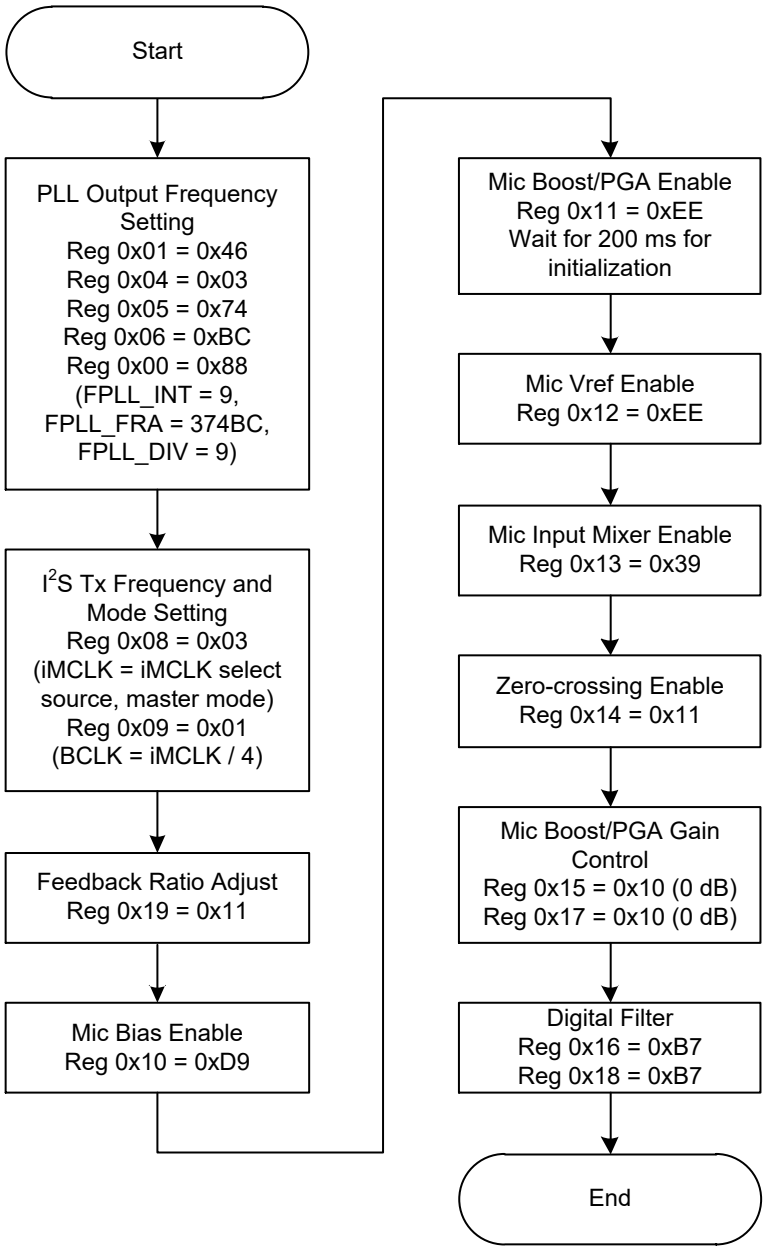


Figure 3–44 Recording Mode Register Control Flow

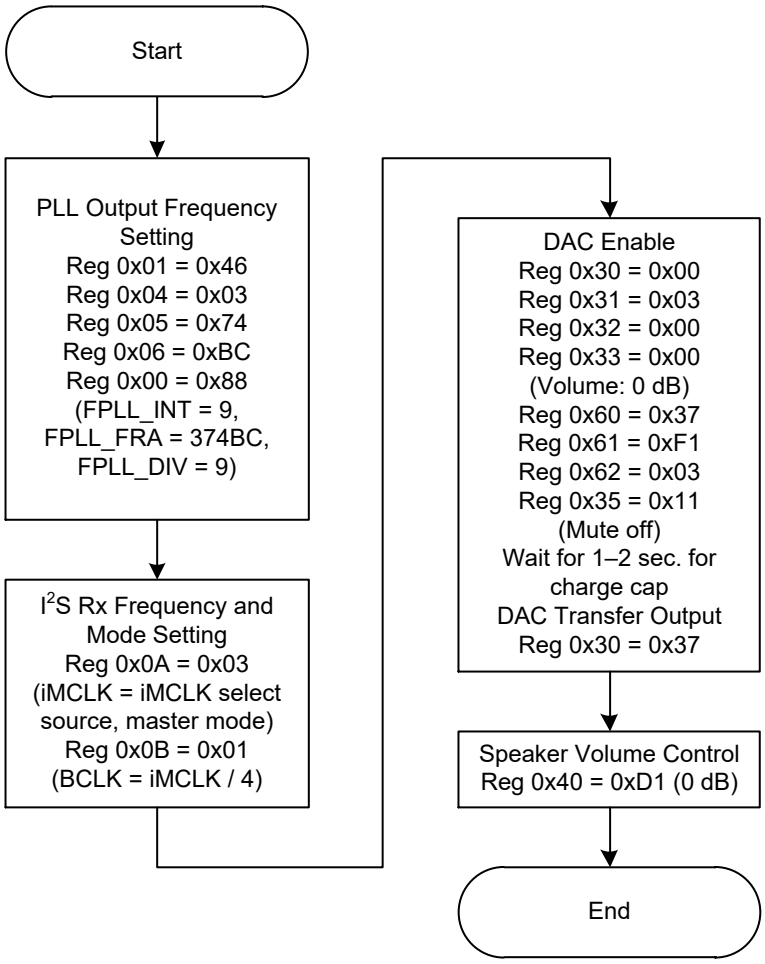


Figure 3–45 AC-coupled Playback Mode Register Control Flow

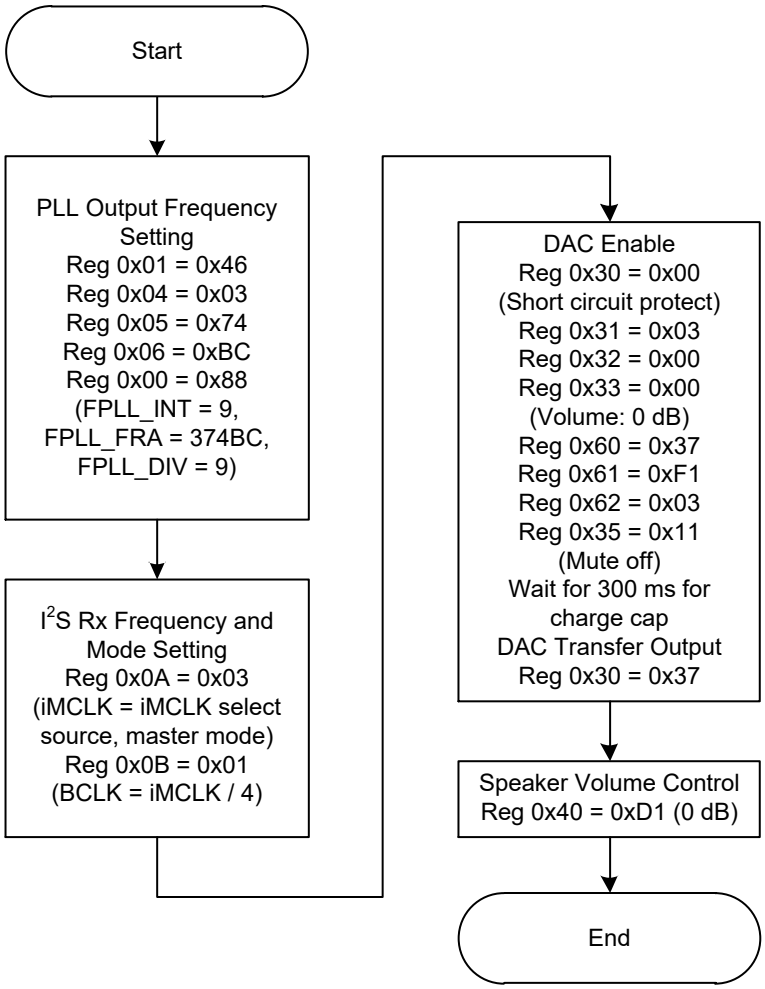


Figure 3–46 Capless Playback Mode Register Control Flow

4 Audio Precision Performance

4.1 Sigma Delta ADC

The table below shows the performance of the Sigma Delta ADC in differential and single-ended mode.

Table 4–1 THD + N of Sigma Delta ADC

Amplitude		Differential Mode	Single-ended Mode
THD + N	0 dB	-78.9	-77.5
	-3 dB	-91	-88.1
	-60 dB	-100.5	-90.875

4.2 Sigma Delta DAC

Table 4–2 and Table 4–3 show the performance of the Sigma Delta DAC in AC-coupled and capless mode.

Table 4–2 THD + N of Sigma Delta DAC in AC-coupled Mode

Load (ohm)		0	16	32	10k
THD + N	0 dB	-80.7	-72.6	-75.6	-80.2
	-3 dB	-84.9	-75.9	-79.3	-84.5
	-60 dB	-101.0	-100.9	-101.2	-101.1

Table 4–3 THD + N of Sigma Delta DAC in Capless Mode

Load (ohm)		0	16	32	10k
THD + N	0 dB	-80.5	-78.3	-78.7	-80.9
	-3 dB	-85.0	-82.9	-83.2	-85.0
	-60 dB	-100.2	-100.1	-101.3	-99.9

5 Device Operating Conditions

5.1 Absolute Maximum Ratings

Table 5–1 Absolute Maximum Ratings[8] [9]

Parameter		MIN.	MAX.	Unit
Analog supply voltage	V_{DDA} with respect to V_{SSA}	-0.3	1.9	V
Supply voltage	V_{DD} with respect to V_{SS}	-0.3	1.9	
	V_{DDIO} with respect to V_{SSIO}	-0.3	3.6	
	V_{DDSPK} with respect to V_{SSSPK}	-0.3	5.5	
Input voltage	V_{IN} (5V)	-0.3	5.5	
Storage temperature	T_{STG}	-40	125	°C

5.2 Recommended Operating Conditions

Table 5–2 Recommended Operating Conditions

Parameter	MIN.	TYP.	MAX.	Unit
Analog supply voltage, V_{DDA}	1.7	1.8	1.9	V
Digital core supply voltage, V_{DD}	1.7	1.8	1.9	
Digital I/O supply voltage, V_{DDIO}	1.7	3.3	3.6	
Speaker amplifier supply voltage, V_{DDSPK}	3.3	5	5.5	
Ground, V_{SSA}, V_{SS}, V_{SSIO}, V_{SSSPK}		0		
Ambient temperature, T_A	0	–	85	°C
Junction temperature, T_J	-40	–	125	

[8] Long-term exposure to absolute maximum ratings may affect device reliability, and permanent damage may occur if the operation exceeds the maximum ratings.
[9] All voltage values are with respect to VSS.

5.3 Electrical Characteristics

Table 5–3 Electrical Characteristics over Recommended Ranges

Parameter		Conditions (T_A = 25 °C)	MIN.	TYP.	MAX.	Unit
Analog to Digital Converter (ADC)						
Full scale input	V_{INFS}	PGABST = 0 dB PGAGAIN = 0 dB	–	1.0 0	–	Vrms dBV
Signal to noise ratio	SNR	Gain = 0 dB, A-weighted	–	100	–	dB
Total harmonic distortion + noise	THD + N	Input = -3 dBV	–	-85	–	
Microphone inputs and programmable gain control						
Programmable PGA gain	–	–	-12	–	35.25	dB
Programmable PGA gain step size	–	Guaranteed monotonic	–	0.75	–	
Programmable boost gain	–	–	0	20	50	
Microphone bias						
Middle voltage	V_{MID}	–	–	0.5* LDO18	–	V
Bias voltage	$V_{MICBIAS}$	–	–	2.56* V_{MID}	–	
Bias current source	$I_{MICBIAS}$	–	–	3	–	mA
Digital to Analog Converter (DAC) with 10k ohm load						
Full scale output	–	Gain = 0 dB	–	0.8	–	Vrms
Signal to noise ratio	SNR	Gain = 0 dB	–	100	–	dB
Total harmonic distortion + noise	THD + N	Input = -3 dBFS	–	-85	–	
Programmable gain control						
Programmable gain	–	–	-96	–	0	dB
Programmable gain step size	–	Guaranteed monotonic	–	0.375	–	
Speaker output (with 8 ohm bridge tied load)						
Full scale output	–	Gain = 0 dB	–	1.6	–	dB
Digital input/output						
Input low level	V_{IL}	–	–	1/3* V_{DDIO}	–	V
Input high level	V_{IH}	–	–	2/3* V_{DDIO}	–	
Input capacitance	–	–	–	10	–	pF
LDO33 Regulator						
Quiescent current	I_Q	–	–	3	8	µA
Output current	I_{OUT}	V_{IN} > 3.6V	–	–	150	mA
Power Consumption						
Power-on, idle	–	No 12 MHz MCLK input	–	3	–	µA
Input MCLK	–	–	–	2.5	–	mA
Turn on PLL	–	–	–	4.96	–	
Turn on ADC	–	Boost gain: 0 dB PGA gain: 0 dB	–	14.7	–	
Turn on DAC + HP + SPK	–	Gain: 0 dB SPK: 8 ohm HP:10k ohm	–	29.6	–	

5.4 Power Sequence

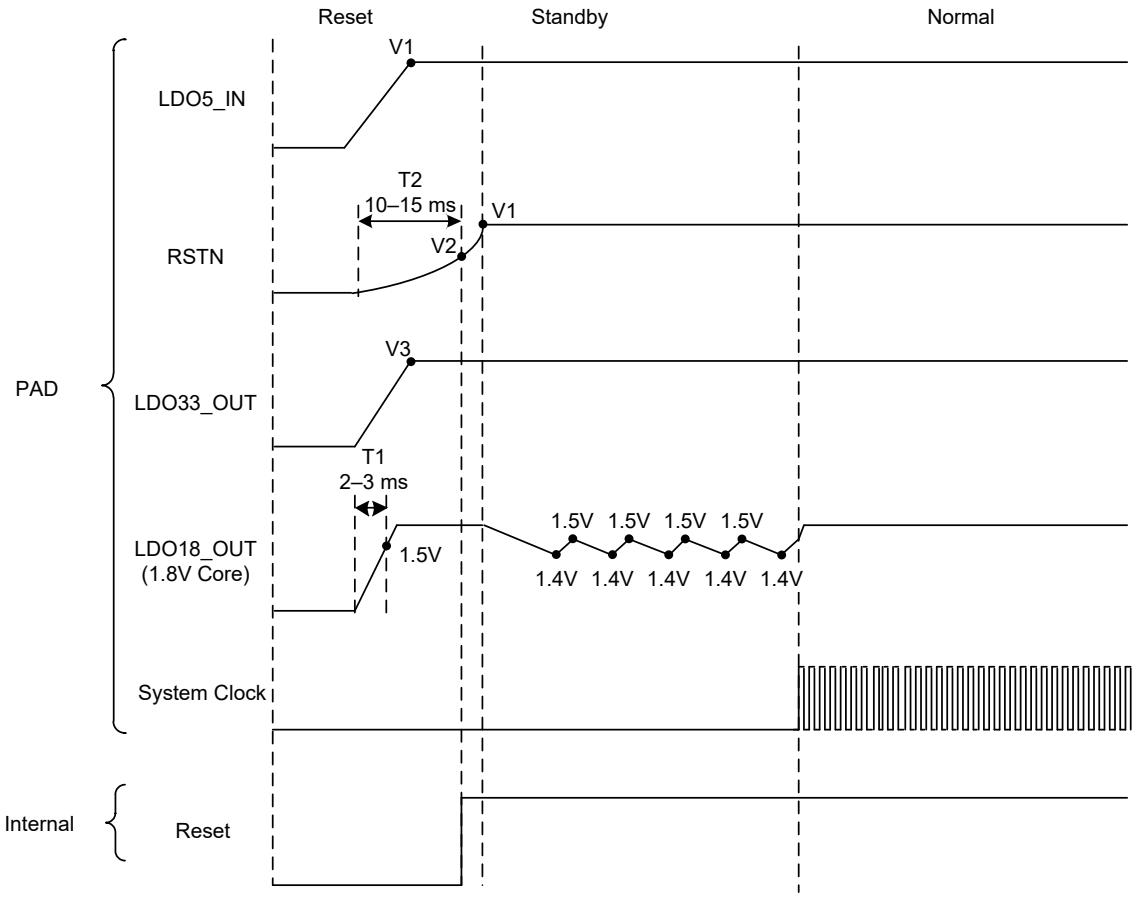


Figure 5–1 Power-on Sequence

Table 5–4 Power Sequence Voltage Range

Symbol	Description	MIN.	TYP.	MAX.	Unit
V1	Input voltage	3.3	5.0	5.5	V
V2	Reset threshold voltage (V1 x 0.7)	1.75	3.5	3.85	
V3	LDO33 regulator output voltage	2.46	3.28	3.28	

Designs of the SNAUD01 must comply with the power-on sequence guidelines below to ensure reliable operation of the device.

Conditions:
1. LDO18 capacitance = 4.7 µF
2. Reset capacitance = 1 µF

Requirement: LDO18_OUT must be over 1.5V before RSTN reaches V2 (T2 > T1).

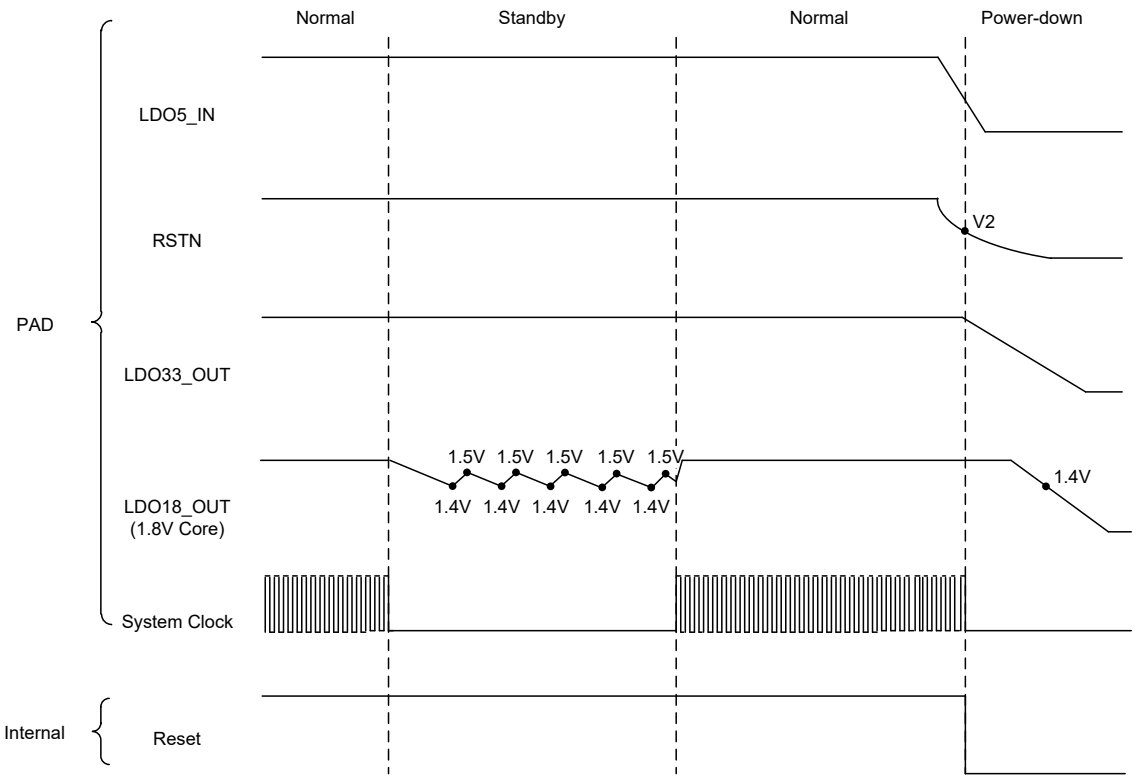


Figure 5–2 Power-down Sequence

The power-down sequence does not have any special requirements.

The host configures SNAUD01 between standby and normal mode by switching the MCLK.

Table 5–5 Power Mode Comparison

Mode / Item	Power-on/Reset (POR)	Standby	Normal
System Clock	–	Without MCLK	With MCLK
Register	Reset	Reset	Keep
Current	–	3 µA	2.5 mA

The two sources to reset the registers to the default values are:

- system power < 1.5V, such as power off
- MCLK removal, such as mode switch from normal to standby

6 Mechanical Data

6.1 Thermal Data

The permissible operating temperature range for the bearing is 0 °C to 85 °C.

6.2 Package Information

6.2.1 Nomenclature

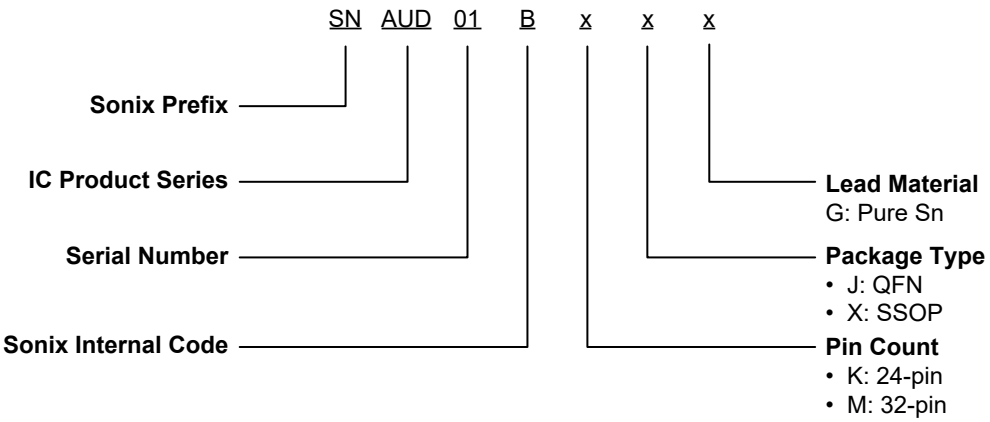


Figure 6–1 Nomenclature

6.2.2 Marking

The figure below is an example of the marking. Contents such as the product ID or symbol may vary according to different packages.

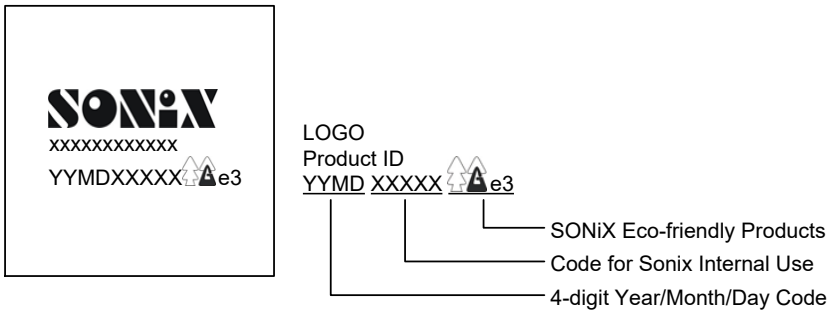
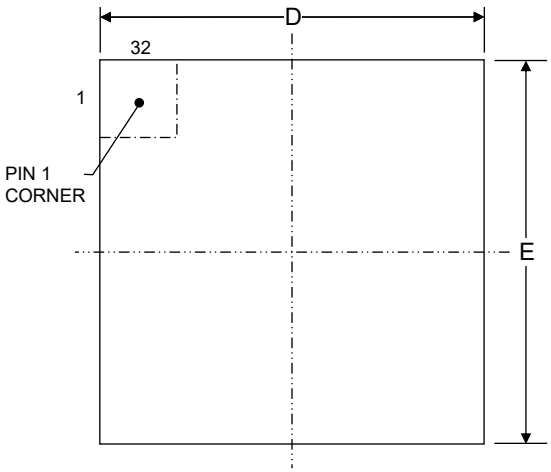


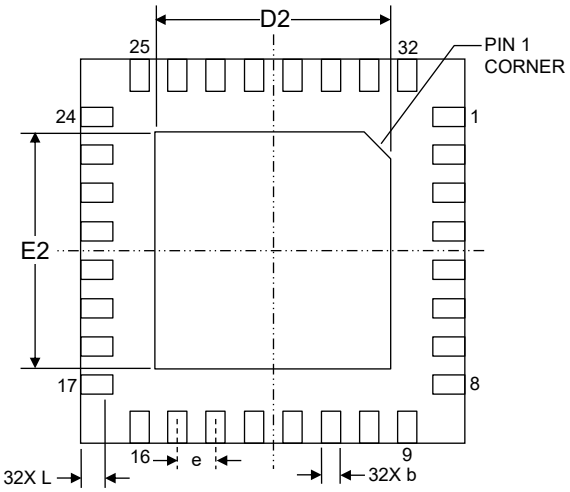
Figure 6–2 Example of Device Marking

6.2.3 Package Dimensions

I. QFN32L (5 x 5 x 0.8 mm/Pitch: 0.5)

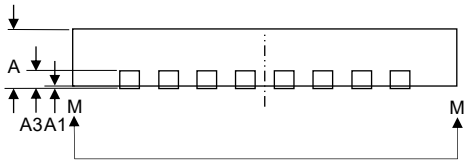


TOP VIEW



BOTTOM VIEW

VIEW M－M

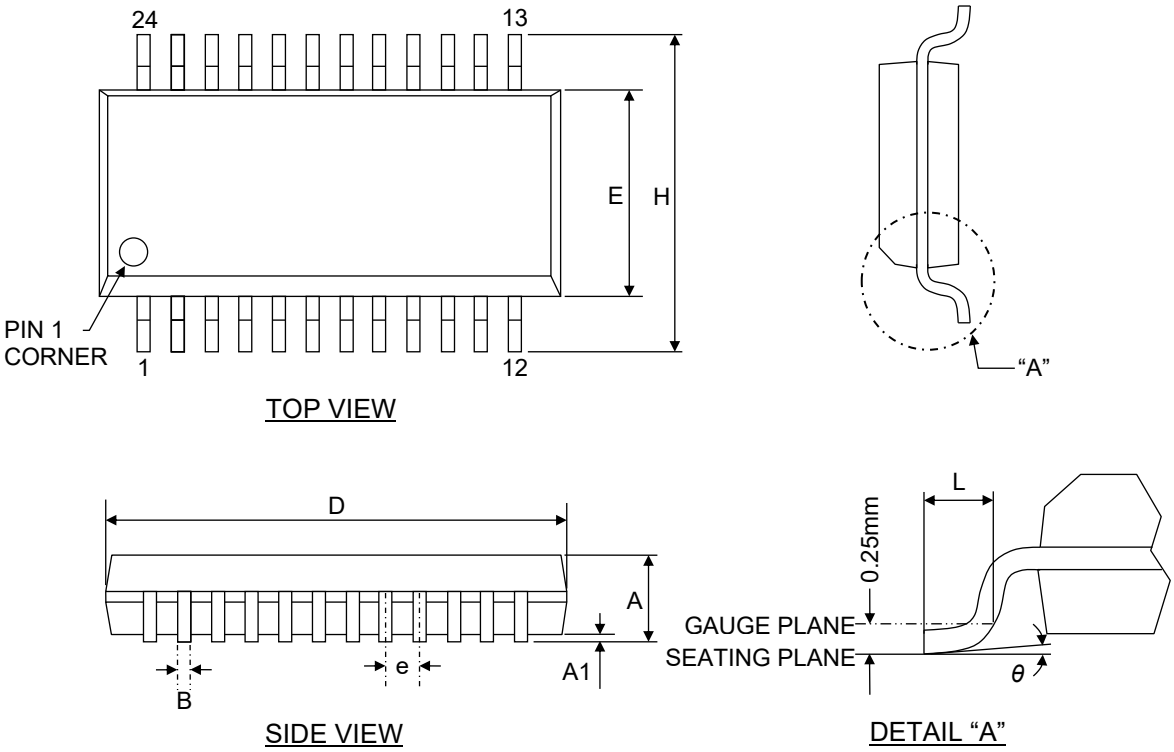


SIDE VIEW

Symbols	Dimension in mm[10]			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.028	0.031	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.203 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC			0.197 BSC		
E	5.00 BSC			0.197 BSC		
e	0.50 BSC			0.020 BSC		
D2	2.60	3.10	3.60	0.102	0.122	0.142
E2	2.60	3.10	3.60	0.102	0.122	0.142
L	0.30	0.40	0.50	0.012	0.016	0.020

[10] Controlling dimension: millimeter (mm)

II. SSOP24L (150 MIL)[11]



Symbols	Dimension in mm			Dimension in inch[12]		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	–	1.75	–	–	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
B	0.20	–	0.30	0.008	–	0.012
D	8.55	8.65	8.75	0.337	0.341	0.344
E	3.80	3.90	4.00	0.150	0.154	0.157
e	0.635 BSC.			0.025 BSC.		
H	5.80	6.00	6.20	0.228	0.236	0.244
L	0.41	0.64	1.27	0.016	0.025	0.050
θ	0°	–	8°	0°	–	8°

[11] JEDEC outline: MO-137 AE
[12] Controlling dimension: inch

6.3 Packaging Appearance and Storage Information

6.3.1 Packing Quantity Information

Table 6–1 Packing Quantity Information

Type	Pin Count	Carry Type	Package Size	IC Q'ty per Tube or Tray or Reel	Tube or Tray or Reel Q'ty per Inner Box	Total Q'ty in One Inner Box	Inner Box Q'ty per Carton	IC Q'ty per Carton
QFN	32L	Tray	5 x 5	490	10	4900	6	29400
SSOP	24L	Tube	150 MIL	50	100	5000	6	30000

6.3.2 Packing Box/Carton Dimension

Table 6–2 Packing Box/Carton Dimension for QFN32L

Inner Box/Carton	Dimension in mm
Inner Box	358 x 159 x 88
Carton	555 x 435 x 280

Table 6–3 Packing Box/Carton Dimension for SSOP24L

Inner Box/Carton	Dimension in mm
Inner Box	610 x 170 x 100
Carton	630 x 360 x 345

6.3.3 Temperature and Humidity Environmental Control Requirements in Storage

Table 6–4 Storage Condition

Control Requirement	Specification
Temp (°C)	24 ± 6
Humid. (%RH)	60 ± 20

6.3.4 Shelf-life

1. The shelf life for unopened vacuum pack products is four years after the date on the label.
2. Once the packaging is opened the product should be conducted SMT process within 168 hours and environmental control is under ≤ 30°C / 60 %RH.
3. If the product has been exposed to the room environment for more than 168 hours, it should be baked in an oven at 125°C for 10 hours and vacuum packed.

Appendix A – PCB Design for Microphone

Comply with the guidelines below to ensure reliable operation.

1. The negative circuit should be parallel to the positive circuit of each MIC channel on the PCB.
2. Keep the MIC path clear, do not place any clock traces around it.

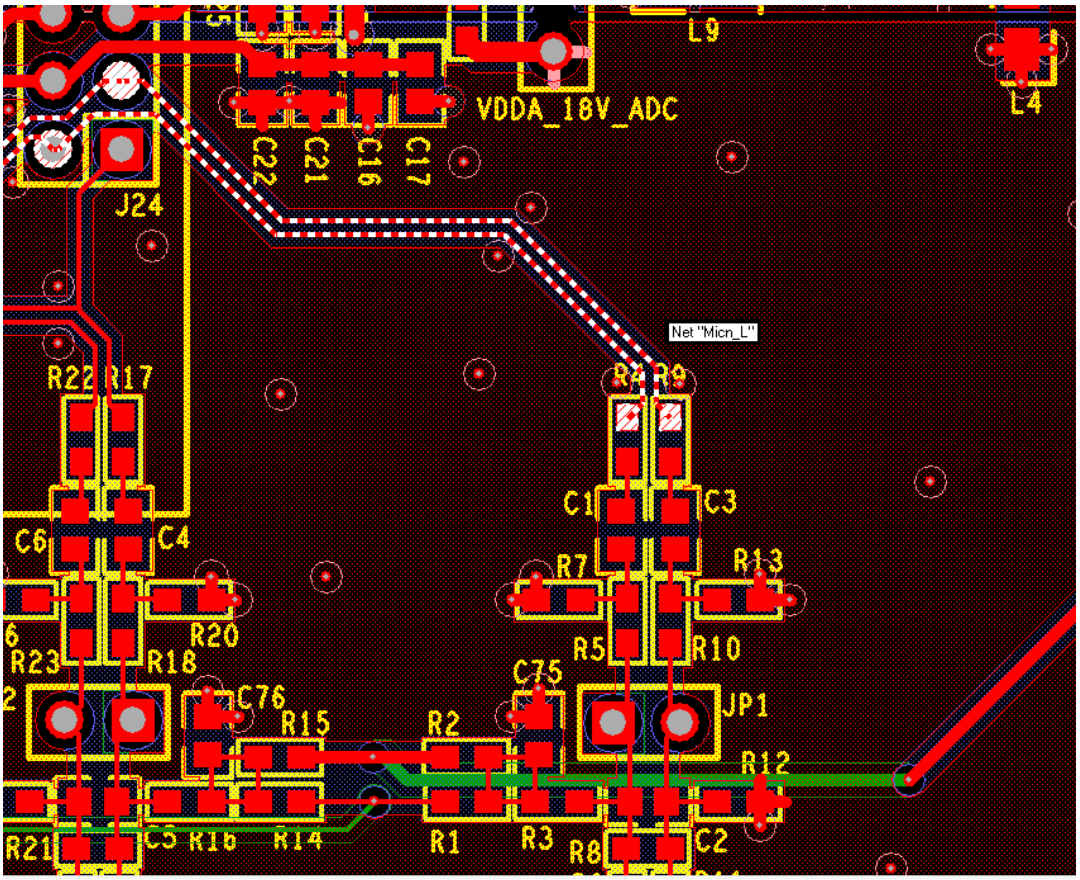


Figure A1 PCB Design Reference for Microphone

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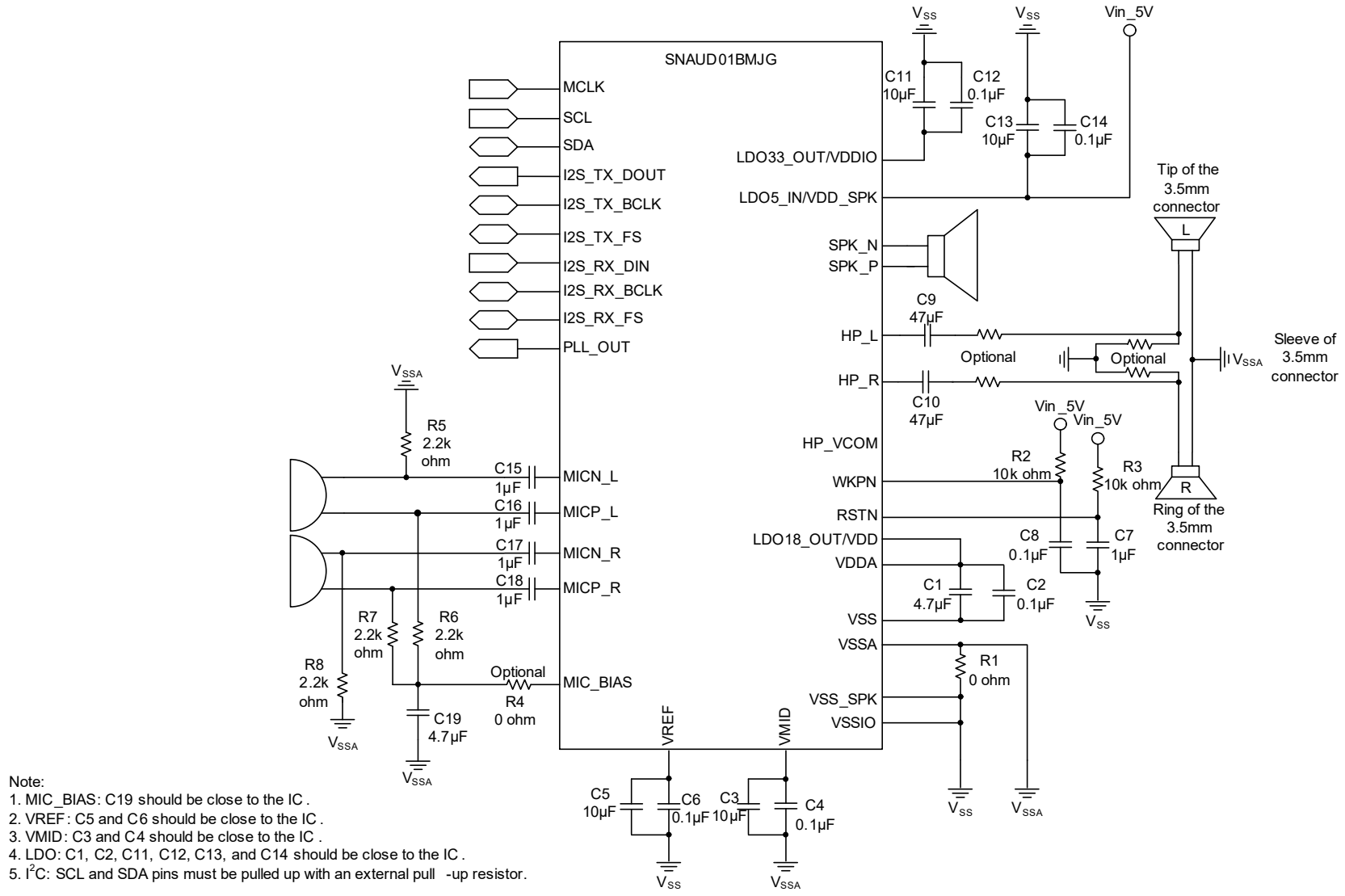
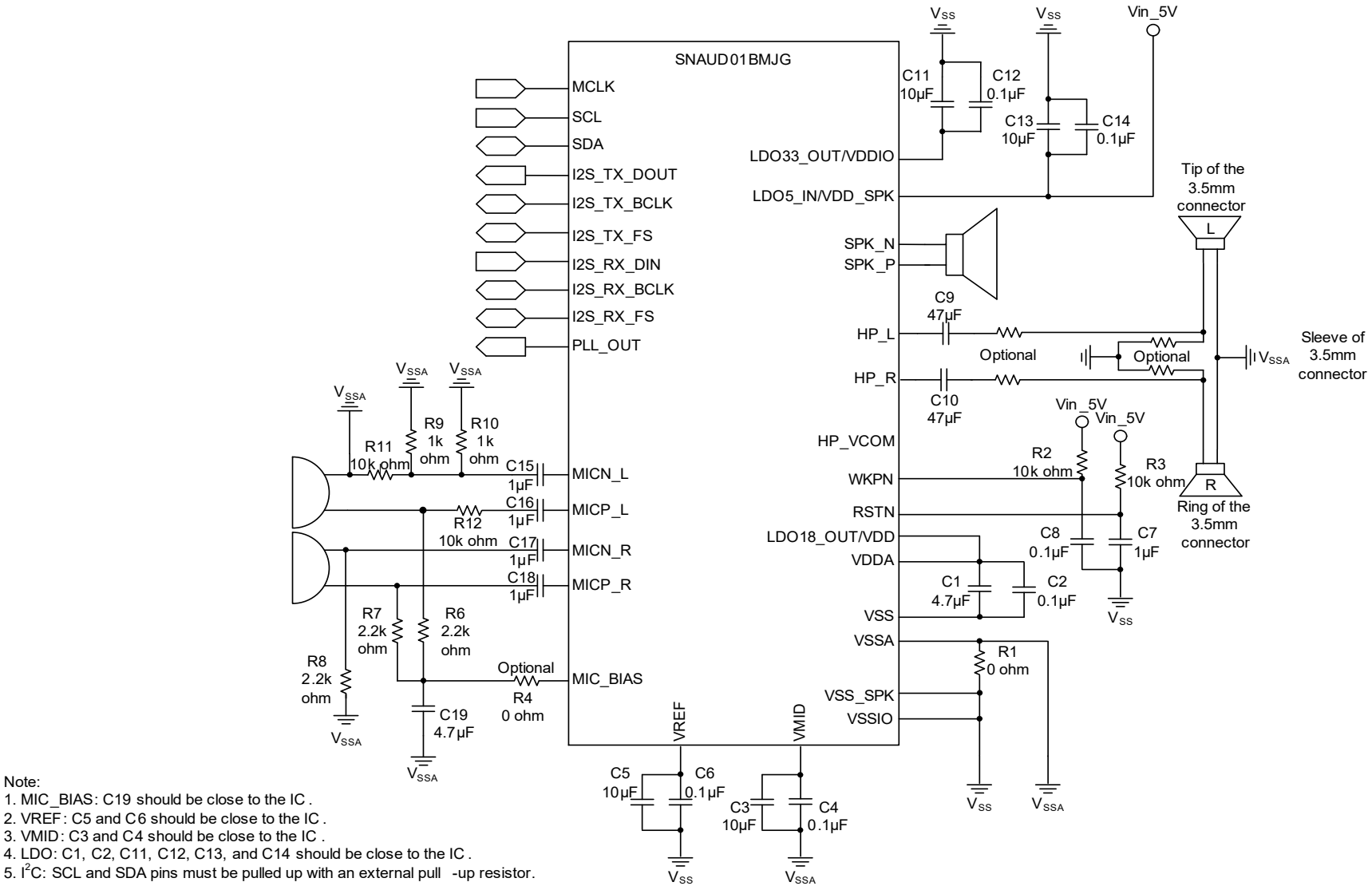


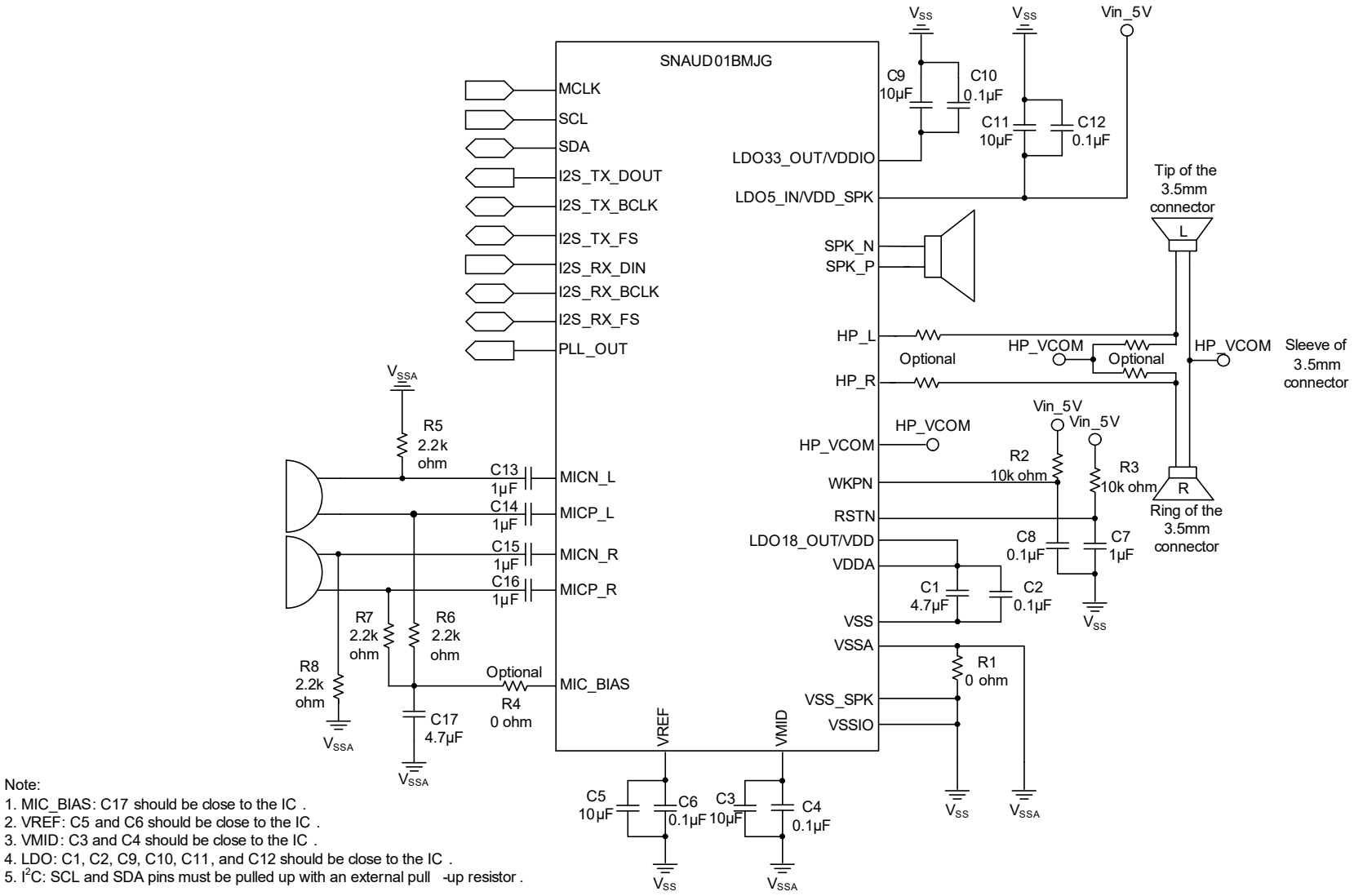
Note:
1. MIC_BIAS: C19 should be close to the IC .
2. VREF: C5 and C6 should be close to the IC .
3. VMID: C3 and C4 should be close to the IC .
4. LDO: C1, C2, C11, C12, C13, and C14 should be close to the IC .
5. I^2C: SCL and SDA pins must be pulled up with an external pull -up resistor.

Figure 1 SNAUD01BMJG with MIC in Differential Mode and Headphone in AC-coupled Mode



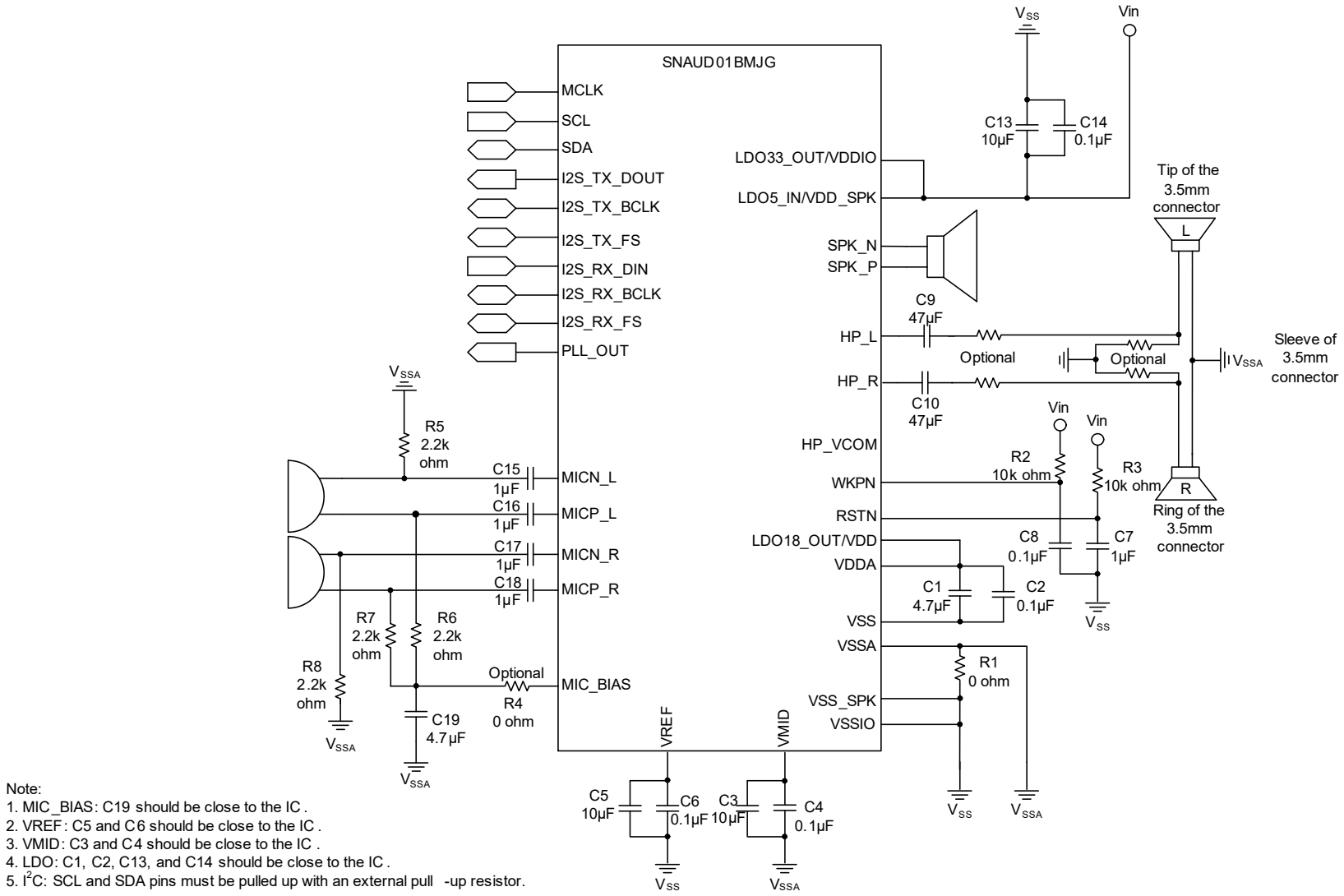
Note:
1. MIC_BIAS: C19 should be close to the IC .
2. VREF: C5 and C6 should be close to the IC .
3. VMID: C3 and C4 should be close to the IC .
4. LDO: C1, C2, C11, C12, C13, and C14 should be close to the IC .
5. I^2C: SCL and SDA pins must be pulled up with an external pull -up resistor.

Figure 2 SNAUD01BMJG with MIC in Single-ended Mode and Headphone in AC-coupled Mode



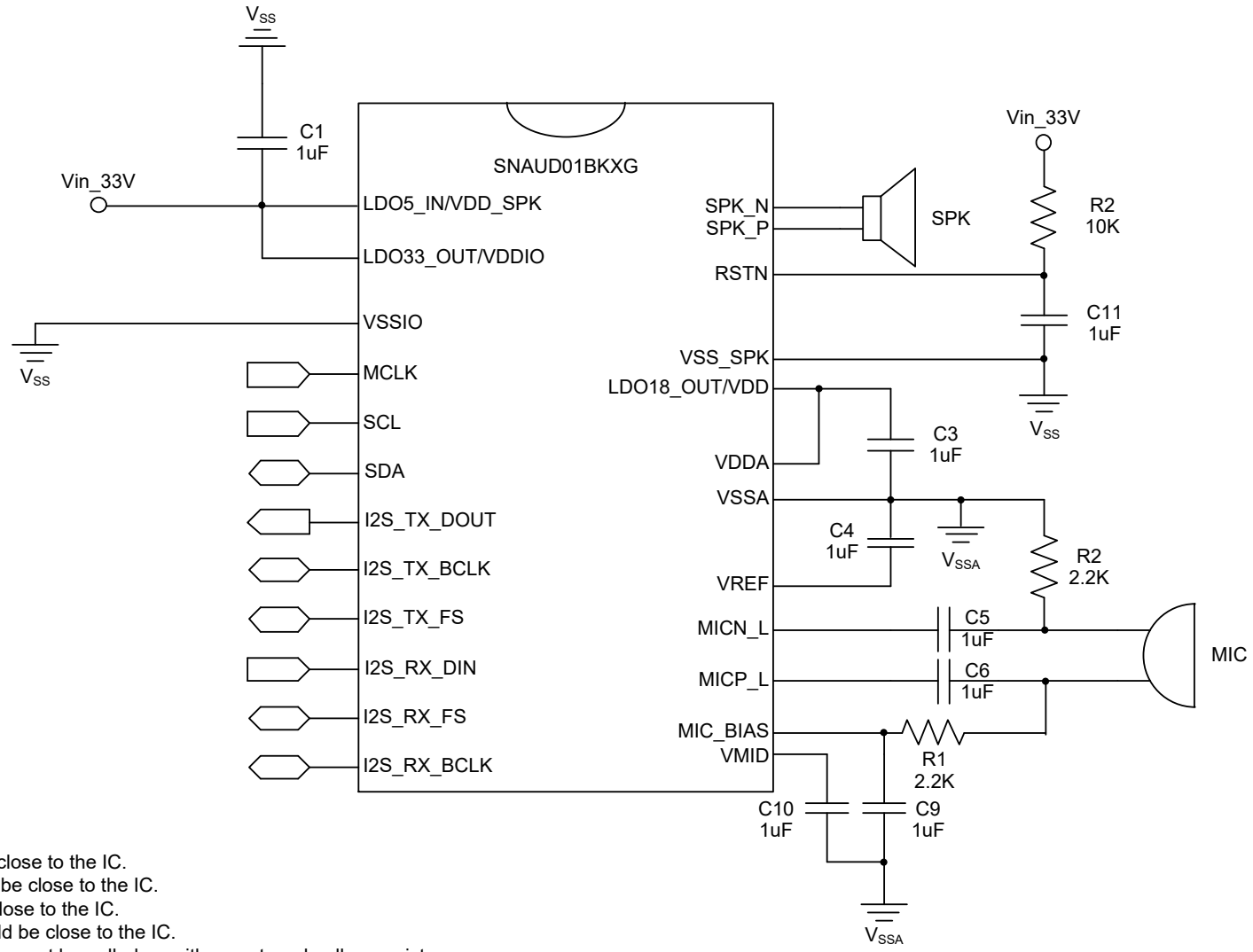
Note:
1. MIC_BIAS: C17 should be close to the IC .
2. VREF: C5 and C6 should be close to the IC .
3. VMID: C3 and C4 should be close to the IC .
4. LDO: C1, C2, C9, C10, C11, and C12 should be close to the IC .
5. I^2C: SCL and SDA pins must be pulled up with an external pull -up resistor .

Figure 3 SNAUD01BMJG with MIC in Differential Mode and Headphone in Capless Mode



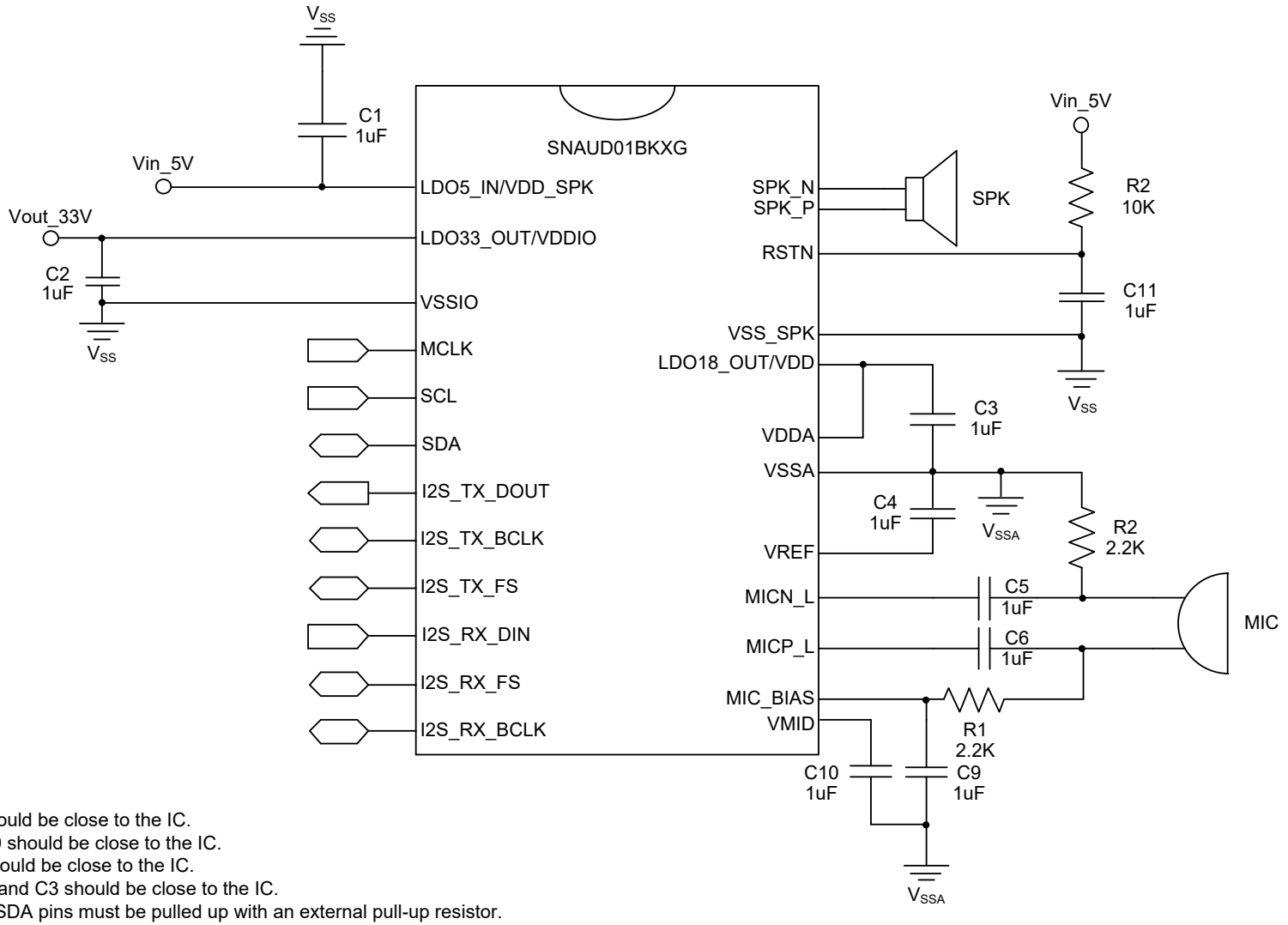
Note:
1. MIC_BIAS: C19 should be close to the IC .
2. VREF: C5 and C6 should be close to the IC .
3. VMID: C3 and C4 should be close to the IC .
4. LDO: C1, C2, C13, and C14 should be close to the IC .
5. I²C: SCL and SDA pins must be pulled up with an external pull -up resistor.

Figure 4 SNAUD01BMJG in 3.3V Application



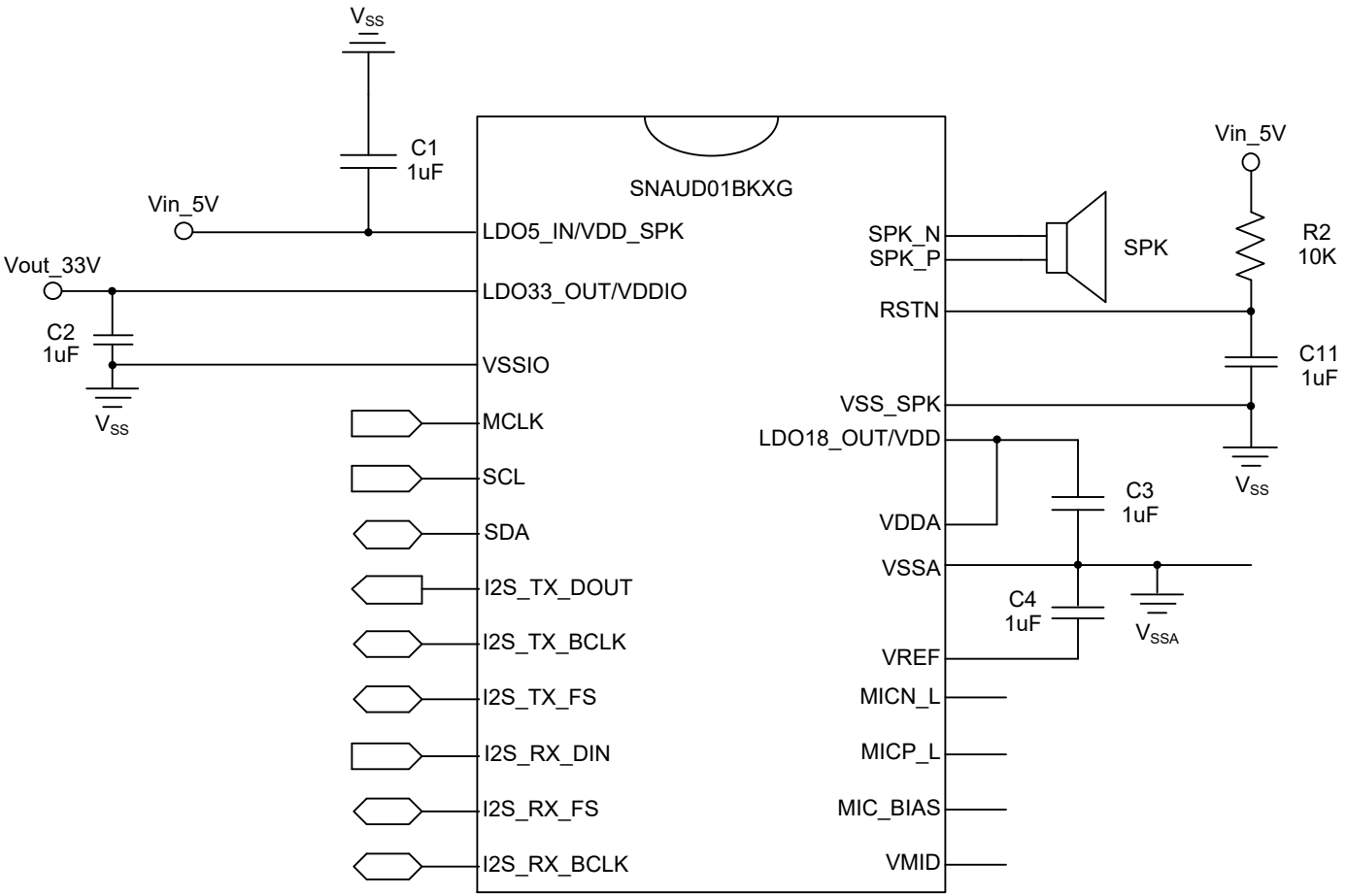
Note:
1. VMID: C10 should be close to the IC.
2. MIC_BIAS: C9 should be close to the IC.
3. VREF: C4 should be close to the IC.
4. LDO: C1 and C3 should be close to the IC.
5. I^2C: SCL and SDA pins must be pulled up with an external pull-up resistor.

Figure 5 SNAUD01BKXG in 3.3V Application



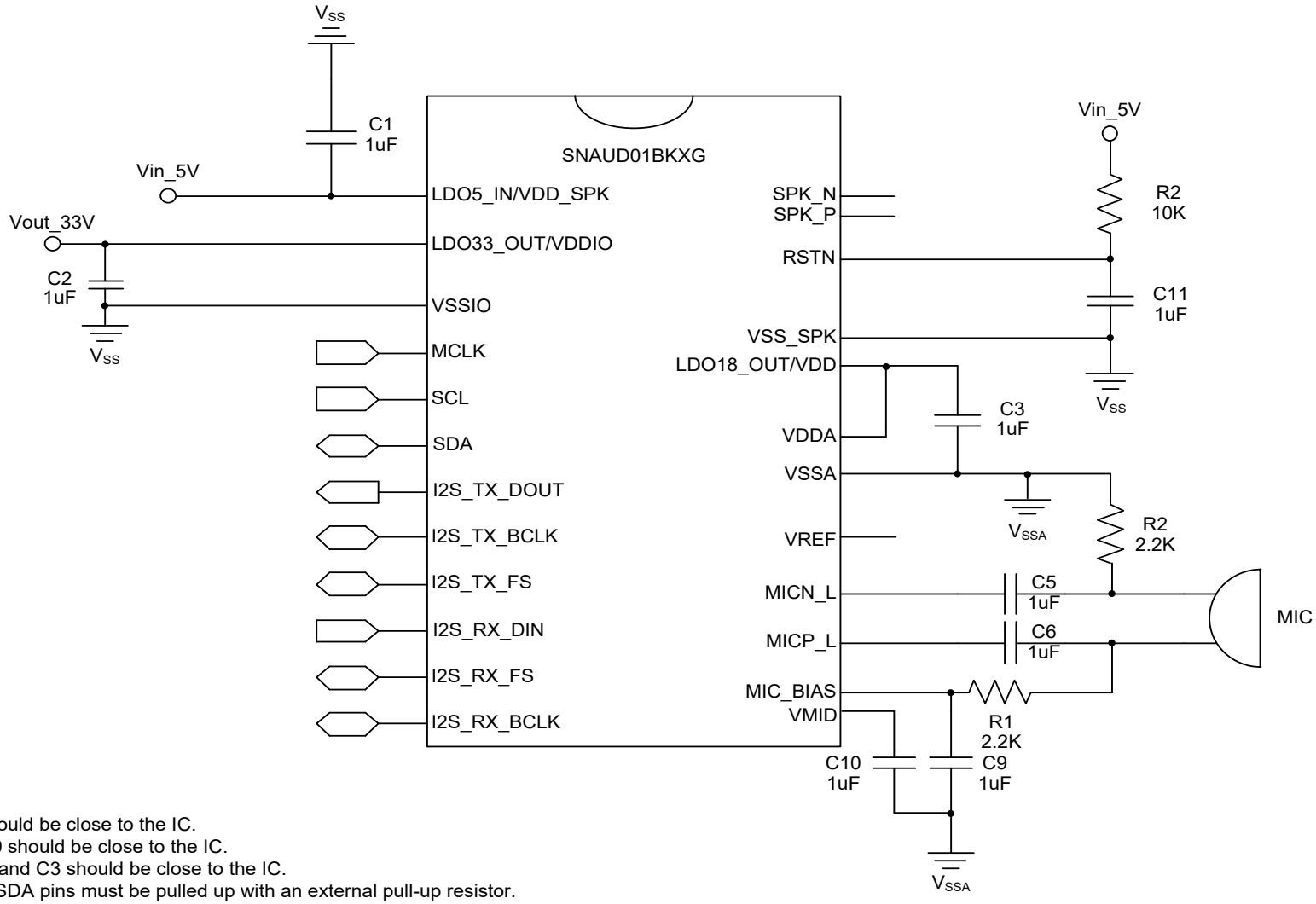
Note:
1. VMID: C10 should be close to the IC.
2. MIC_BIAS: C9 should be close to the IC.
3. VREF: C14 should be close to the IC.
4. LDO: C1, C2, and C3 should be close to the IC.
5. I^2C: SCL and SDA pins must be pulled up with an external pull-up resistor.

Figure 6 SNAUD01BKXG with Speaker and MIC in Simultaneous Operation in Differential Mode



Note:
1. VREF: C4 should be close to the IC.
2. LDO: C1, C2, and C3 should be close to the IC.
3. I^2C: SCL and SDA pins must be pulled up with an external pull-up resistor.

Figure 7 SNAUD01BKXG with Speaker



Note:
1. VMID: C10 should be close to the IC.
2. MIC_BIAS: C9 should be close to the IC.
3. LDO: C1, C2, and C3 should be close to the IC.
4. I^2C: SCL and SDA pins must be pulled up with an external pull-up resistor.

Figure 8 SNAUD01BKXG with MIC