

# **SN32F760/750 Series**

## **USER'S MANUAL**

**SN32F769/759**  
**SN32F768/758**  
**SN32F767/757**  
**SN32F766/756**  
**SN32F765/755**

## **SONiX 32-Bit Cortex-M0 Micro-Controller**

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## AMENDENT HISTORY

| Version | Date       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
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| 1.0     | 2014/02/27 | First version released.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 1.1     | 2014/05/23 | 1. Fix typing errors.<br>2. Update <a href="#">23.3 Marking Example section</a> .<br>3. Update SN-LINK-V2 photos.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 1.2     | 2015/03/06 | 1. Update GPIO & LCD driver characteristics in Chap <a href="#">20 Electrical Characteristic</a> .<br>2. Fix typing error in <a href="#">16.8 LCD DISPLAY MEMORY MAP</a><br>3. Add notice for power input pads.<br>4. Fix typing errors.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 1.3     | 2015/05/29 | 1. Update QFN46 package information.<br>2. Update UART baud rate sample.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 1.4     | 2015/08/21 | 1. Add Note for P2.n GPIO setting if ADC function is used.<br>2. Update <a href="#">PLL recommend input/output frequency setting table</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 1.5     | 2016/07/22 | 1. Fix typing errors.<br>2. Add Notice: HCLK MUST be equal or less than 24MHz during Flash program and erase operations.<br>3. Update LQFP48 package information.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 1.6     | 2016/12/02 | 1. Fix typing errors.<br>2. Remove SN32F74X & SN32F73X.<br>3. Remove SYSTICKPRE[1:0]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 1.7     | 2017/06/05 | 1. Remove SYS0_ANTIEFT register.<br>2. Fix Deep Sleep mode wake up time.<br>3. Update SN-LINK-V3.0 information.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 1.8     | 2017/07/14 | 1. Update WDTPRE[2:0] bits description in SYS1_APBPCP1 register.<br>2. Update TO[15:0] bits description in I2Cn_TOCTRL register.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 1.9     | 2017/12/21 | 1. Update <a href="#">LCD drive waveform</a> .<br>2. Add Note for setting the pins which are not pin-out.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 2.0     | 2018/10/05 | 1. Add Boot pin description.<br>2. Fix maximum F <sub>ADCLK</sub> to 16MHz in Electrical Characteristics.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 2.1     | 2019/02/22 | 1. Remove Deep power-down mode<br>2. Update GPIO2_CFG register to add input gating function instead of the repeat mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 2.2     | 2019/03/15 | 1. Add Unique number descriptions.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 2.3     | 2019/05/31 | 1. Update electrical characteristics of LVD.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 2.4     | 2019/09/20 | 1. Add <a href="#">7.3.3 ADC PIN CONFIGURATION</a><br>2. Update <a href="#">22 PACKAGE INFORMATION</a> with new format.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 2.5     | 2022/03/24 | 1. Update <a href="#">7.2 ADC CONVERTING TIME</a><br>2. Complement Chap 12 I2C.<br>3. Add notifications of BOOT pin in 1.4 PIN ASSIGNMENT.<br>4. Add introduction of <a href="#">2.6 UNIQUE NUMBER</a> .<br>5. Update electrical characteristics of Deep sleep mode.<br>6. Update <a href="#">code security switch schematic diagram</a> .<br>7. Remove reset RTC registers description.<br>8. Update <a href="#">14.6 BAUD RATE CALCULATION</a> .<br>9. Update description in UARTn_FD register.<br>10. Update <a href="#">3.1.4.1 SIMPLY RC RESET CIRCUIT</a><br>11. Fix description in <a href="#">3.4.1 SYS1_AHBCLKEN register</a> .<br>12. Modify pin circuit diagrams in <a href="#">1.6 PIN CIRCUIT DIAGRAMS</a> . |
| 2.6     | 2023/05/29 | 1. Update <a href="#">1.6 PIN CIRCUIT DIAGRAMS</a><br>2. Update description of <a href="#">3.1.4 EXTERNAL RESET</a> .<br>3. Fix description in <a href="#">3.2.3.2 CRYSTAL/CERAMIC</a><br>4. Update description of <a href="#">14.6 BAUD RATE CALCULATION</a> and <a href="#">14.11.14 UASRTn_FD register</a><br>5. Update <a href="#">22 PACKAGE INFORMATION</a><br>6. Update <a href="#">23.4 DATECODE SYSTEM</a>                                                                                                                                                                                                                                                                                                       |
| 2.7     | 2024/05/15 | 1. Add introduction of <a href="#">12.5 TIMING CHARACTERISTICS</a><br>2. Add ESD information in <a href="#">20 ELECTRICAL CHARACTERISTIC</a><br>3. Update <a href="#">21 FLASH ROM PROGRAMMING PIN</a>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 2.8     | 2025/04/07 | 1. Add notice in <a href="#">4.3.2 DEEP-SLEEP MODE</a><br>2. Update description of <a href="#">8.2 FEATURES</a> and <a href="#">9.2 FEATURES</a>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

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| 2.9 | 2025/07/14 | 1. Update <a href="#">1.4 PIN ASSIGNMENT</a><br>2. Update notice in <a href="#">8.7.3 CT16Bn Prescale register</a> and <a href="#">8.7.5 CT16Bn Count Control register</a><br>3. Update <a href="#">22.5 QFN 33 PIN 5x5</a> and <a href="#">22.4 QFN 46 PIN</a> |
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# Table of Content

|          |                                                              |           |
|----------|--------------------------------------------------------------|-----------|
| <b>1</b> | <b>PRODUCT OVERVIEW</b>                                      | <b>15</b> |
| 1.1      | FEATURES                                                     | 15        |
| 1.2      | SYSTEM BLOCK DIAGRAM                                         | 17        |
| 1.3      | CLOCK GENERATION BLOCK DIAGRAM                               | 18        |
| 1.4      | PIN ASSIGNMENT                                               | 19        |
| 1.5      | PIN DESCRIPTIONS                                             | 24        |
| 1.6      | PIN CIRCUIT DIAGRAMS                                         | 29        |
| <b>2</b> | <b>CENTRAL PROCESSOR UNIT (CPU)</b>                          | <b>32</b> |
| 2.1      | MEMORY MAP                                                   | 32        |
| 2.2      | SYSTEM TICK TIMER                                            | 33        |
| 2.2.1    | OPERATION                                                    | 33        |
| 2.2.2    | SYSTICK USAGE HINTS AND TIPS                                 | 34        |
| 2.2.3    | SYSTICK REGISTERS                                            | 34        |
| 2.2.3.1  | System Tick Timer Control and Status register (SYSTICK_CTRL) | 34        |
| 2.2.3.2  | System Tick Timer Reload value register (SYSTICK_LOAD)       | 34        |
| 2.2.3.3  | System Tick Timer Current Value register (SYSTICK_VAL)       | 35        |
| 2.2.3.4  | System Tick Timer Calibration Value register (SYSTICK_CALIB) | 35        |
| 2.3      | NESTED VECTORED INTERRUPT CONTROLLER (NVIC)                  | 36        |
| 2.3.1    | INTERRUPT AND EXCEPTION VECTORS                              | 36        |
| 2.3.2    | NVIC REGISTERS                                               | 37        |
| 2.3.2.1  | IRQ0~31 Interrupt Set-Enable Register (NVIC_ISER)            | 37        |
| 2.3.2.2  | IRQ0~31 Interrupt Clear-Enable Register (NVIC_ICER)          | 37        |
| 2.3.2.3  | IRQ0~31 Interrupt Set-Pending Register (NVIC_ISPR)           | 38        |
| 2.3.2.4  | IRQ0~31 Interrupt Clear-Pending Register (NVIC_ICPR)         | 38        |
| 2.3.2.5  | IRQ0~31 Interrupt Priority Register (NVIC_IPRn) (n=0~7)      | 38        |
| 2.4      | APPLICATION INTERRUPT AND RESET CONTROL (AIRC)               | 39        |
| 2.5      | CODE OPTION TABLE                                            | 40        |
| 2.6      | UNIQUE NUMBER                                                | 40        |
| 2.7      | CORE REGISTER OVERVIEW                                       | 41        |
| <b>3</b> | <b>SYSTEM CONTROL</b>                                        | <b>42</b> |
| 3.1      | RESET                                                        | 42        |
| 3.1.1    | POWER-ON RESET (POR)                                         | 42        |
| 3.1.2    | WATCHDOG RESET (WDT RESET)                                   | 43        |
| 3.1.3    | BROWN-OUT RESET                                              | 43        |
| 3.1.3.1  | BROWN OUT DESCRIPTION                                        | 43        |

|         |                                                            |    |
|---------|------------------------------------------------------------|----|
| 3.1.3.2 | THE SYSTEM OPERATING VOLTAGE DECSRIPTION .....             | 44 |
| 3.1.3.3 | BROWN-OUT RESET IMPROVEMENT .....                          | 44 |
| 3.1.4   | EXTERNAL RESET .....                                       | 45 |
| 3.1.4.1 | SIMPLY RC RESET CIRCUIT .....                              | 46 |
| 3.1.4.2 | DIODE & RC RESET CIRCUIT .....                             | 46 |
| 3.1.4.3 | ZENER DIODE RESET CIRCUIT .....                            | 47 |
| 3.1.4.4 | VOLTAGE BIAS RESET CIRCUIT .....                           | 47 |
| 3.1.4.5 | EXTERNAL RESET IC .....                                    | 48 |
| 3.1.5   | SOFTWARE RESET .....                                       | 48 |
| 3.2     | SYSTEM CLOCK .....                                         | 49 |
| 3.2.1   | INTERNAL RC CLOCK SOURCE .....                             | 49 |
| 3.2.1.1 | Internal High-speed RC Oscillator (IHRC) .....             | 49 |
| 3.2.1.2 | Internal Low-speed RC Oscillator (ILRC) .....              | 49 |
| 3.2.2   | PLL .....                                                  | 50 |
| 3.2.2.1 | PLL Frequency selection .....                              | 50 |
| 3.2.3   | EXTERNAL CLOCK SOURCE .....                                | 51 |
| 3.2.3.1 | External High-speed (EHS) Clock .....                      | 51 |
| 3.2.3.2 | CRYSTAL/CERAMIC .....                                      | 51 |
| 3.2.3.3 | External Low-speed (ELS) Clock .....                       | 52 |
| 3.2.3.4 | CRYSTAL .....                                              | 52 |
| 3.2.3.5 | Bypass Mode .....                                          | 52 |
| 3.2.4   | SYSTEM CLOCK (SYSCLK) SELECTION .....                      | 53 |
| 3.2.5   | CLOCK-OUT CAPABILITY .....                                 | 53 |
| 3.3     | SYSTEM CONTROL REGISTERS 0 .....                           | 54 |
| 3.3.1   | Analog Block Control register (SYS0_ANBCTRL) .....         | 54 |
| 3.3.2   | PLL control register (SYS0_PLLCTRL) .....                  | 54 |
| 3.3.2.1 | RECOMMEND FREQUENCY SETTING .....                          | 55 |
| 3.3.3   | Clock Source Status register (SYS0_CSST) .....             | 55 |
| 3.3.4   | System Clock Configuration register (SYS0_CLKCFG) .....    | 56 |
| 3.3.5   | AHB Clock Prescale register (SYS0_AHBCP) .....             | 56 |
| 3.3.6   | System Reset Status register (SYS0_RSTST) .....            | 57 |
| 3.3.7   | LVD Control register (SYS0_LVDCTRL) .....                  | 57 |
| 3.3.8   | External RESET Pin Control register (SYS0_EXRSTCTRL) ..... | 58 |
| 3.3.9   | SWD Pin Control register (SYS0_SWDCTRL) .....              | 58 |
| 3.4     | SYSTEM CONTROL REGISTERS 1 .....                           | 59 |
| 3.4.1   | AHB Clock Enable register (SYS1_AHBCLKEN) .....            | 59 |
| 3.4.2   | APB Clock Prescale register 0 (SYS1_APB0) .....            | 60 |
| 3.4.3   | APB Clock Prescale register 1 (SYS1_APB1) .....            | 61 |
| 3.4.4   | APB Clock Prescale register 2 (SYS1_APB2) .....            | 63 |
| 3.4.5   | Peripheral Reset register (SYS1_PRST) .....                | 63 |

|          |                                                                             |           |
|----------|-----------------------------------------------------------------------------|-----------|
| 3.4.6    | Divider Dividend register (SYS1_DIVIDEND) .....                             | 65        |
| 3.4.7    | Divider Divisor register (SYS1_DIVISOR) .....                               | 65        |
| 3.4.8    | Divider Quotient register (SYS1_QUOTIENT) .....                             | 65        |
| 3.4.9    | Divider Remainder register (SYS1_REMAINDER).....                            | 65        |
| 3.4.10   | Divider Control register (SYS1_DIVCTRL).....                                | 66        |
| <b>4</b> | <b>SYSTEM OPERATION MODE .....</b>                                          | <b>67</b> |
| 4.1      | OVERVIEW .....                                                              | 67        |
| 4.2      | NORMAL MODE .....                                                           | 67        |
| 4.3      | LOW-POWER MODES .....                                                       | 67        |
| 4.3.1    | SLEEP MODE .....                                                            | 67        |
| 4.3.2    | DEEP-SLEEP MODE.....                                                        | 68        |
| 4.4      | WAKEUP .....                                                                | 69        |
| 4.4.1    | OVERVIEW .....                                                              | 69        |
| 4.4.2    | WAKEUP TIME.....                                                            | 69        |
| 4.5      | STATE MACHINE OF PMU .....                                                  | 70        |
| 4.6      | OPERATION MODE COMPARSION TABLE .....                                       | 71        |
| 4.7      | PMU REGISTERS .....                                                         | 72        |
| 4.7.1    | Power Control register (PMU_CTRL).....                                      | 72        |
| <b>5</b> | <b>GENERAL PURPOSE I/O PORT (GPIO) .....</b>                                | <b>73</b> |
| 5.1      | OVERVIEW .....                                                              | 73        |
| 5.2      | GPIO MODE .....                                                             | 73        |
| 5.3      | GPIO REGISTERS.....                                                         | 74        |
| 5.3.1    | GPIO Port n Data register (GPIOn_DATA) (n=0,1,2,3).....                     | 74        |
| 5.3.2    | GPIO Port n Mode register (GPIOn_MODE) (n=0,1,2,3).....                     | 74        |
| 5.3.3    | GPIO Port n Configuration register (GPIOn_CFG) (n=0,1,3).....               | 74        |
| 5.3.4    | GPIO Port n Configuration register (GPIOn_CFG) (n=2).....                   | 76        |
| 5.3.5    | GPIO Port n Interrupt Sense register (GPIOn_IS) (n=0,1,2,3).....            | 77        |
| 5.3.6    | GPIO Port n Interrupt Both-edge Sense register (GPIOn_IBS) (n=0,1,2,3)..... | 77        |
| 5.3.7    | GPIO Port n Interrupt Event register (GPIOn_IEV) (n=0,1,2,3).....           | 78        |
| 5.3.8    | GPIO Port n Interrupt Enable register (GPIOn_IE) (n=0,1,2,3).....           | 78        |
| 5.3.9    | GPIO Port n Raw Interrupt Status register (GPIOn_RIS) (n=0,1,2,3) .....     | 78        |
| 5.3.10   | GPIO Port n Interrupt Clear register (GPIOn_IC) (n=0,1,2,3).....            | 78        |
| 5.3.11   | GPIO Port n Bits Set Operation register (GPIOn_BSET) (n=0,1,2,3).....       | 79        |
| 5.3.12   | GPIO Port n Bits Clear Operation register (GPIOn_BCLR) (n=0,1,2,3).....     | 79        |
| 5.3.13   | GPIO Port n Open-Drain Control register (GPIOn_ODCTRL) (n=0,1,2,3) .....    | 80        |
| <b>6</b> | <b>PERIPHERAL FUNCTION PIN ASSIGNMENT (PFPA) .....</b>                      | <b>81</b> |
| 6.1      | OVERVIEW .....                                                              | 81        |
| 6.2      | FEATURES .....                                                              | 81        |

|          |                                                            |            |
|----------|------------------------------------------------------------|------------|
| 6.3      | PIN ASSIGNMENT LIST .....                                  | 81         |
| 6.4      | PFPA REGISTERS.....                                        | 82         |
| 6.4.1    | PFPA for UART register (PFPA_UART).....                    | 82         |
| 6.4.2    | PFPA for I2C register (PFPA_I2C).....                      | 83         |
| 6.4.3    | PFPA for SSP register (PFPA_SSP).....                      | 84         |
| 6.4.4    | PFPA for I2S register (PFPA_I2S) .....                     | 85         |
| 6.4.5    | PFPA for CT16B0 register (PFPA_CT16B0) .....               | 86         |
| 6.4.6    | PFPA for CT16B1 register (PFPA_CT16B1) .....               | 87         |
| 6.4.7    | PFPA for CT16B2 register (PFPA_CT16B2) .....               | 87         |
| 6.4.8    | PFPA for CT32B0 register (PFPA_CT32B0) .....               | 88         |
| 6.4.9    | PFPA for CT32B1 register (PFPA_CT32B1) .....               | 89         |
| 6.4.10   | PFPA for CT32B2 register (PFPA_CT32B2) .....               | 90         |
| <b>7</b> | <b>14+1 CHANNEL ANALOG TO DIGITAL CONVERTOR (ADC).....</b> | <b>92</b>  |
| 7.1      | OVERVIEW .....                                             | 92         |
| 7.2      | ADC CONVERTING TIME .....                                  | 93         |
| 7.3      | ADC CONTROL NOTICE.....                                    | 94         |
| 7.3.1    | ADC SIGNAL.....                                            | 94         |
| 7.3.2    | ADC PROGRAM .....                                          | 94         |
| 7.3.3    | ADC PIN CONFIGURATION .....                                | 94         |
| 7.4      | ADC CIRCUIT .....                                          | 95         |
| 7.5      | TEMPERATURE SENSOR (TS).....                               | 95         |
| 7.6      | ADC REGISTERS.....                                         | 97         |
| 7.6.1    | ADC Management register (ADC_ADM).....                     | 97         |
| 7.6.2    | ADC Data register (ADC_ADB) .....                          | 98         |
| 7.6.3    | Port 2 Control register (ADC_P2CON).....                   | 98         |
| 7.6.4    | ADC Interrupt Enable register (ADC_IE).....                | 99         |
| 7.6.5    | ADC Raw Interrupt Status register (ADC_RIS).....           | 99         |
| <b>8</b> | <b>16-BIT TIMER WITH CAPTURE FUNCTION .....</b>            | <b>100</b> |
| 8.1      | OVERVIEW .....                                             | 100        |
| 8.2      | FEATURES .....                                             | 100        |
| 8.3      | PIN DESCRIPTION .....                                      | 100        |
| 8.4      | BLOCK DIAGRAM.....                                         | 101        |
| 8.5      | TIMER OPERATION .....                                      | 102        |
| 8.5.1    | Edge-aligned Up-counting Mode .....                        | 102        |
| 8.5.2    | Edge-aligned Down-counting Mode.....                       | 103        |
| 8.5.3    | Center-aligned Counting Mode .....                         | 103        |
| 8.6      | PWM.....                                                   | 104        |
| 8.6.1    | PWM Mode 1 .....                                           | 104        |

|          |                                                                         |            |
|----------|-------------------------------------------------------------------------|------------|
| 8.6.2    | PWM Mode 2 .....                                                        | 105        |
| 8.7      | CT16Bn REGISTERS .....                                                  | 107        |
| 8.7.1    | CT16Bn Timer Control register (CT16Bn_TMRCTRL) (n=0,1,2) .....          | 107        |
| 8.7.2    | CT16Bn Timer Counter register (CT16Bn_TC) (n=0,1,2) .....               | 107        |
| 8.7.3    | CT16Bn Prescale register (CT16Bn_PRE) (n=0,1,2).....                    | 108        |
| 8.7.4    | CT16Bn Prescale Counter register (CT16Bn_PC) (n=0,1,2).....             | 108        |
| 8.7.5    | CT16Bn Count Control register (CT16Bn_CNTCTRL) (n=0,1,2).....           | 108        |
| 8.7.6    | CT16Bn Match Control register (CT16Bn_MCTRL) (n=0,1,2) .....            | 109        |
| 8.7.7    | CT16Bn Match register 0~3 (CT16Bn_MR0~3) (n=0,1,2).....                 | 110        |
| 8.7.8    | CT16Bn Capture Control register (CT16Bn_CAPCTRL) (n=0,1,2) .....        | 110        |
| 8.7.9    | CT16Bn Capture 0 register (CT16Bn_CAP0) (n=0,1,2) .....                 | 110        |
| 8.7.10   | CT16Bn External Match register (CT16Bn_EM) (n=0,1,2) .....              | 111        |
| 8.7.11   | CT16Bn PWM Control register (CT16Bn_PWMCTRL) (n=0,1,2).....             | 111        |
| 8.7.12   | CT16Bn Timer Raw Interrupt Status register (CT16Bn_RIS) (n=0,1,2) ..... | 112        |
| 8.7.13   | CT16Bn Timer Interrupt Clear register (CT16Bn_IC) (n=0,1,2).....        | 113        |
| <b>9</b> | <b>32-BIT TIMER WITH CAPTURE FUNCTION .....</b>                         | <b>114</b> |
| 9.1      | OVERVIEW .....                                                          | 114        |
| 9.2      | FEATURES .....                                                          | 114        |
| 9.3      | PIN DESCRIPTION .....                                                   | 114        |
| 9.4      | BLOCK DIAGRAM.....                                                      | 115        |
| 9.5      | TIMER OPERATION .....                                                   | 116        |
| 9.5.1    | Edge-aligned Up-counting Mode .....                                     | 116        |
| 9.5.2    | Edge-aligned Down-counting Mode.....                                    | 117        |
| 9.5.3    | Center-aligned Counting Mode .....                                      | 117        |
| 9.6      | PWM.....                                                                | 118        |
| 9.6.1    | PWM Mode 1 .....                                                        | 118        |
| 9.6.2    | PWM Mode 2 .....                                                        | 119        |
| 9.7      | CT32Bn REGISTERS .....                                                  | 121        |
| 9.7.1    | CT32Bn Timer Control register (CT32Bn_TMRCTRL) (n=0,1,2) .....          | 121        |
| 9.7.2    | CT32Bn Timer Counter register (CT32Bn_TC) (n=0,1,2) .....               | 121        |
| 9.7.3    | CT32Bn Prescale register (CT32Bn_PRE) (n=0,1,2).....                    | 122        |
| 9.7.4    | CT32Bn Prescale Counter register (CT32Bn_PC) (n=0,1,2).....             | 122        |
| 9.7.5    | CT32Bn Count Control register (CT32Bn_CNTCTRL) (n=0,1,2).....           | 122        |
| 9.7.6    | CT32Bn Match Control register (CT32Bn_MCTRL) (n=0,1,2) .....            | 123        |
| 9.7.7    | CT32Bn Match register 0~3 (CT32Bn_MR0~3) (n=0,1,2).....                 | 123        |
| 9.7.8    | CT32Bn Capture Control register (CT32Bn_CAPCTRL) (n=0,1,2) .....        | 124        |
| 9.7.9    | CT32Bn Capture 0 register (CT32Bn_CAP0) (n=0,1,2) .....                 | 124        |
| 9.7.10   | CT32Bn External Match register (CT32Bn_EM) (n=0,1,2) .....              | 124        |
| 9.7.11   | CT32Bn PWM Control register (CT32Bn_PWMCTRL) (n=0,1,2).....             | 125        |

|           |                                                                   |            |
|-----------|-------------------------------------------------------------------|------------|
| 9.7.12    | CT32Bn Timer Raw Interrupt Status register (CT32Bn_RIS) (n=0,1,2) | 126        |
| 9.7.13    | CT32Bn Timer Interrupt Clear register (CT32Bn_IC) (n=0,1,2)       | 127        |
| <b>10</b> | <b>WATCHDOG TIMER (WDT)</b>                                       | <b>128</b> |
| 10.1      | OVERVIEW                                                          | 128        |
| 10.2      | BLOCK DIAGRAM                                                     | 129        |
| 10.3      | WDT REGISTERS                                                     | 130        |
| 10.3.1    | Watchdog Configuration register (WDT_CFG)                         | 130        |
| 10.3.2    | Watchdog Clock Source register (WDT_CLKSOURCE)                    | 130        |
| 10.3.3    | Watchdog Timer Constant register (WDT_TC)                         | 130        |
| 10.3.4    | Watchdog Feed register (WDT_FEED)                                 | 131        |
| <b>11</b> | <b>REAL-TIME CLOCK (RTC)</b>                                      | <b>132</b> |
| 11.1      | OVERVIEW                                                          | 132        |
| 11.2      | FEATURES                                                          | 132        |
| 11.3      | FUNCTIONAL DESCRIPTION                                            | 132        |
| 11.3.1    | INTRODUCTION                                                      | 132        |
| 11.3.2    | RTC FLAG ASSERTION                                                | 132        |
| 11.3.3    | RTC OPERATION                                                     | 132        |
| 11.4      | BLOCK DIAGRAM                                                     | 134        |
| 11.5      | RTC REGISTERS                                                     | 135        |
| 11.5.1    | RTC Control register (RTC_CTRL)                                   | 135        |
| 11.5.2    | RTC Clock Source Select register (RTC_CLKS)                       | 135        |
| 11.5.3    | RTC Interrupt Enable register (RTC_IE)                            | 135        |
| 11.5.4    | RTC Raw Interrupt Status register (RTC_RIS)                       | 135        |
| 11.5.5    | RTC Interrupt Clear register (RTC_IC)                             | 136        |
| 11.5.6    | RTC Second Counter Reload Value register (RTC_SECCNTV)            | 136        |
| 11.5.7    | RTC Second Count register (RTC_SECCNT)                            | 136        |
| 11.5.8    | RTC Alarm Counter Reload Value register (RTC_ALMCNTV)             | 136        |
| 11.5.9    | RTC Alarm Count register (RTC_ALMCNT)                             | 137        |
| <b>12</b> | <b>SPI/SSP</b>                                                    | <b>138</b> |
| 12.1      | OVERVIEW                                                          | 138        |
| 12.2      | FEATURES                                                          | 138        |
| 12.3      | PIN DESCRIPTION                                                   | 138        |
| 12.4      | INTERFACE DESCRIPTION                                             | 139        |
| 12.4.1    | SPI                                                               | 139        |
| 12.4.2    | SSI                                                               | 140        |
| 12.4.3    | COMMUNICATION FLOW                                                | 140        |
| 12.4.3.1  | SINGLE-FRAME                                                      | 140        |
| 12.4.3.2  | MULTI-FRAME                                                       | 141        |

|           |                                                             |            |
|-----------|-------------------------------------------------------------|------------|
| 12.5      | TIMING CHARACTERISTICS.....                                 | 141        |
| 12.6      | AUTO-SEL.....                                               | 142        |
| 12.7      | SSP REGISTERS .....                                         | 143        |
| 12.7.1    | SSP n Control register 0 (SSPn_CTRL0) (n=0,1).....          | 143        |
| 12.7.2    | SSP n Control register 1 (SSPn_CTRL1) (n=0,1).....          | 144        |
| 12.7.3    | SSP n Clock Divider register (SSPn_CLKDIV) (n=0,1).....     | 144        |
| 12.7.4    | SSP n Status register (SSPn_STAT) (n=0,1).....              | 144        |
| 12.7.5    | SSP n Interrupt Enable register (SSPn_IE) (n=0,1).....      | 145        |
| 12.7.6    | SSP n Raw Interrupt Status register (SSPn_RIS) (n=0,1)..... | 145        |
| 12.7.7    | SSP n Interrupt Clear register (SSPn_IC) (n=0,1).....       | 146        |
| 12.7.8    | SSP n Data register (SSPn_DATA) (n=0,1).....                | 146        |
| 12.7.9    | SSP n Data Fetch register (SSPn_DF) (n=0,1).....            | 146        |
| <b>13</b> | <b>I2C.....</b>                                             | <b>147</b> |
| 13.1      | OVERVIEW.....                                               | 147        |
| 13.2      | FEATURES.....                                               | 147        |
| 13.3      | PIN DESCRIPTION.....                                        | 147        |
| 13.4      | I2C PROTOCOL.....                                           | 148        |
| 13.4.1    | 7-BIT ADDRESSING MODES .....                                | 148        |
| 13.4.1.1  | MASTER TRANSMITTER MODE .....                               | 148        |
| 13.4.1.2  | MASTER RECEIVER MODE.....                                   | 149        |
| 13.4.1.3  | SLAVE TRANSMITTER MODE.....                                 | 149        |
| 13.4.1.4  | SLAVE RECEIVER MODE .....                                   | 149        |
| 13.4.2    | 10-BIT ADDRESSING MODES .....                               | 149        |
| 13.4.2.1  | MASTER TRANSMITTER MODE .....                               | 149        |
| 13.4.2.2  | MASTER RECEIVER MODE.....                                   | 149        |
| 13.5      | ARBITRATION.....                                            | 150        |
| 13.6      | CLOCK STRETCHING.....                                       | 150        |
| 13.7      | GENERAL CALL ADDRESS .....                                  | 150        |
| 13.8      | TIMING CHARACTERISTICS.....                                 | 151        |
| 13.8.1    | MASTER TRANSMITTER MODE .....                               | 151        |
| 13.8.2    | SLAVE TRANSMITTER MODE .....                                | 151        |
| 13.9      | MONITOR MODE.....                                           | 152        |
| 13.9.1    | INTERRUPT.....                                              | 152        |
| 13.9.2    | LOSS of ARBITRATION.....                                    | 152        |
| 13.10     | I2C REGISTERS .....                                         | 153        |
| 13.10.1   | I2C n Control register (I2Cn_CTRL) (n=0,1).....             | 153        |
| 13.10.2   | I2C n Status register (I2Cn_STAT) (n=0,1).....              | 154        |
| 13.10.3   | I2C n TX Data register (I2Cn_TXDATA) (n=0,1).....           | 155        |
| 13.10.4   | I2C n RX Data register (I2Cn_RXDATA) (n=0,1).....           | 155        |

|           |                                                                                     |            |
|-----------|-------------------------------------------------------------------------------------|------------|
| 13.10.5   | I2C n Slave Address 0 register (I2Cn_SLVADDR0) (n=0,1).....                         | 155        |
| 13.10.6   | I2C n Slave Address 1~3 register (I2Cn_SLVADDR1~3) (n=0,1) .....                    | 155        |
| 13.10.7   | I2C n SCL High Time register (I2Cn_SCLHT) (n=0,1).....                              | 156        |
| 13.10.8   | I2C n SCL Low Time register (I2Cn_SCLLT) (n=0,1).....                               | 156        |
| 13.10.9   | I2C n Timeout Control register (I2Cn_TOCTRL) (n=0,1) .....                          | 156        |
| 13.10.10  | I2C n Monitor Mode Control register (I2Cn_MMCTRL) (n=0,1).....                      | 156        |
| <b>14</b> | <b>UNIVERSAL SYNCHRONOUS AND ASYNCHRONOUS RECEIVER AND TRANSMITTER (USART).....</b> | <b>158</b> |
| 14.1      | OVERVIEW .....                                                                      | 158        |
| 14.2      | FEATURES .....                                                                      | 158        |
| 14.3      | PIN DESCRIPTION .....                                                               | 158        |
| 14.4      | BLOCK DIAGRAM.....                                                                  | 159        |
| 14.5      | EIA-485/RS-485 MODES .....                                                          | 160        |
| 14.5.1    | RS-485/EIA-485 NORMAL MULTIDROP MODE (NMM).....                                     | 160        |
| 14.5.2    | RS-485/EIA-485 AUTO ADDRESS DETECTION (AAD) MODE .....                              | 160        |
| 14.5.3    | RS-485/EIA-485 AUTO DIRECTION CONTROL (ADC).....                                    | 160        |
| 14.5.4    | RS485/EIA-485 DRIVER DELAY TIME.....                                                | 161        |
| 14.5.5    | RS485/EIA-485 OUTPUT INVERSION .....                                                | 161        |
| 14.5.6    | RS485/EIA-485 FRAME STRUCTURE.....                                                  | 161        |
| 14.6      | BAUD RATE CALCULATION .....                                                         | 161        |
| 14.7      | MODEM CONTROL (MC).....                                                             | 163        |
| 14.7.1    | AUTO-RTS.....                                                                       | 163        |
| 14.7.2    | AUTO-CTS.....                                                                       | 164        |
| 14.8      | AUTO-BAUD FLOW .....                                                                | 164        |
| 14.8.1    | AUTO-BAUD.....                                                                      | 164        |
| 14.8.2    | AUTO-BAUD MODES .....                                                               | 165        |
| 14.9      | SMART CARD MODE .....                                                               | 166        |
| 14.9.1    | SMART CARD SETUP PROCEDURE.....                                                     | 166        |
| 14.10     | SYNCHRONOUS MODE.....                                                               | 167        |
| 14.11     | USART REGISTERS .....                                                               | 169        |
| 14.11.1   | USART n Receiver Buffer register (USARTn_RB) (n=0,1).....                           | 169        |
| 14.11.2   | USART n Transmitter Holding register (USARTn_TH) (n=0,1).....                       | 169        |
| 14.11.3   | USART n Divisor Latch LSB registers (USARTn_DLL) (n =0,1) .....                     | 169        |
| 14.11.4   | USART n Divisor Latch MSB register (USARTn_DLM) (n=0,1) .....                       | 169        |
| 14.11.5   | USART n Interrupt Enable register (USARTn_IE) (n=0,1) .....                         | 170        |
| 14.11.6   | USART n Interrupt Identification register (USARTn_II) (n=0,1) .....                 | 170        |
| 14.11.7   | USART n Line Status register (USARTn_LS) (n=0,1).....                               | 172        |
| 14.11.8   | USART n FIFO Control register (USARTn_FIFOCtrl) (n=0,1).....                        | 173        |
| 14.11.9   | USART n Line Control register (USARTn_LC) (n=0,1) .....                             | 173        |

|           |                                                                              |            |
|-----------|------------------------------------------------------------------------------|------------|
| 14.11.10  | USART n Modem Control register (USARTn_MC) (n=0,1) .....                     | 174        |
| 14.11.11  | USART n Modem Status register (USARTn_MS) (n=0,1).....                       | 174        |
| 14.11.12  | USART n Scratch Pad register (USARTn_SP) (n=0,1).....                        | 175        |
| 14.11.13  | USART n Auto-baud Control register (USARTn_ABCTRL) (n=0,1).....              | 175        |
| 14.11.14  | USART n Fractional Divider register (USARTn_FD) (n=0,1) .....                | 175        |
| 14.11.15  | USART n Control register (USARTn_CTRL) (n=0,1).....                          | 176        |
| 14.11.16  | USART n Half-duplex Enable register (USARTn_HDEN) (n=0,1) .....              | 177        |
| 14.11.17  | USART n Smart card Interface Control register (USARTn_SCICTRL) (n=0,1) ..... | 177        |
| 14.11.18  | USART n RS485 Control register (USARTn_RS485CTRL) (n=0,1).....               | 178        |
| 14.11.19  | USART n RS485 Address Match register (USARTn_RS485ADRMATCH) (n=0,1) .....    | 178        |
| 14.11.20  | USART n RS485 Delay Value register (USARTn_RS485DLYV) (n=0,1) .....          | 178        |
| 14.11.21  | USART n Synchronous Mode Control Register (USARTn_SYNCCTRL) (n=0,1) .....    | 179        |
| <b>15</b> | <b>I2S .....</b>                                                             | <b>180</b> |
| 15.1      | OVERVIEW .....                                                               | 180        |
| 15.2      | FEATURES .....                                                               | 180        |
| 15.3      | PIN DESCRIPTION .....                                                        | 180        |
| 15.4      | BLOCK DIAGRAM.....                                                           | 181        |
| 15.4.1    | I2S CLCOK CONTROL.....                                                       | 181        |
| 15.4.2    | I2S BLOCK DIAGRAM .....                                                      | 181        |
| 15.5      | FUNCTIONAL DESCRIPTION .....                                                 | 182        |
| 15.5.1    | I2S OPERATION .....                                                          | 182        |
| 15.5.2    | I2S FIFO OPERAION .....                                                      | 184        |
| 15.5.2.1  | MONO .....                                                                   | 184        |
| 15.5.2.2  | STEREO .....                                                                 | 184        |
| 15.6      | I2S REGISTERS.....                                                           | 185        |
| 15.6.1    | I2S Control register (I2S_CTRL) .....                                        | 185        |
| 15.6.2    | I2S Clock register (I2S_CLK).....                                            | 186        |
| 15.6.3    | I2S Status register (I2S_STATUS).....                                        | 186        |
| 15.6.4    | I2S Interrupt Enable register (I2S_IE).....                                  | 187        |
| 15.6.5    | I2S Raw Interrupt Status register (I2S_RIS) .....                            | 187        |
| 15.6.6    | I2S Interrupt Clear register (I2S_IC).....                                   | 188        |
| 15.6.7    | I2S RXFIFO register (I2S_RXFIFO) .....                                       | 188        |
| 15.6.8    | I2S TXFIFO register (I2S_TXFIFO).....                                        | 188        |
| <b>16</b> | <b>4X32 LCD DRIVER .....</b>                                                 | <b>189</b> |
| 16.1      | OVERVIEW .....                                                               | 189        |
| 16.2      | FEATURES .....                                                               | 189        |
| 16.3      | PIN DESCRIPTION .....                                                        | 189        |
| 16.4      | BLOCK DIAGRAM.....                                                           | 190        |

|           |                                                      |            |
|-----------|------------------------------------------------------|------------|
| 16.4.1    | LCD CLOCK CONTROL .....                              | 190        |
| 16.4.2    | LCD BLOCK DIAGRAM.....                               | 190        |
| 16.5      | LCD TIMING.....                                      | 191        |
| 16.5.1    | LCD Timing Table.....                                | 191        |
| 16.5.2    | LCD Driver Waveform .....                            | 191        |
| 16.6      | R-TYPE LCD APPLICATION CIRCUIT.....                  | 193        |
| 16.7      | C-TYPE LCD APPLICATION CIRCUIT.....                  | 194        |
| 16.7.1    | 4C-TYPE.....                                         | 195        |
| 16.7.2    | 1C-Type .....                                        | 197        |
| 16.8      | LCD DISPLAY MEMORY MAP .....                         | 198        |
| 16.9      | LCD REGISTERS .....                                  | 199        |
| 16.9.1    | LCD Control register (LCD_CTRL).....                 | 199        |
| 16.9.2    | LCD Control register 1(LCD_CTRL1).....               | 200        |
| 16.9.3    | LCD C-Type Control register 1 (LCD_CCTRL1) .....     | 200        |
| 16.9.4    | LCD C-Type Control register 2 (LCD_CCTRL2) .....     | 201        |
| 16.9.5    | LCD Frame Counter Control register (LCD_FCC).....    | 201        |
| 16.9.6    | LCD Raw Interrupt Status register (LCD_RIS) .....    | 202        |
| 16.9.7    | LCD SEG Memory register 0 (LCD_SEGM0) .....          | 202        |
| 16.9.8    | LCD SEG Memory register 1 (LCD_SEGM1) .....          | 202        |
| 16.9.9    | LCD SEG Memory register 2 (LCD_SEGM2) .....          | 203        |
| 16.9.10   | LCD SEG Memory register 3 (LCD_SEGM3) .....          | 203        |
| <b>17</b> | <b>FLASH.....</b>                                    | <b>204</b> |
| 17.1      | OVERVIEW .....                                       | 204        |
| 17.2      | EMBEDDED FLASH MEMORY .....                          | 204        |
| 17.3      | FEATURES .....                                       | 204        |
| 17.4      | ORGANIZATION.....                                    | 205        |
| 17.5      | READ .....                                           | 205        |
| 17.6      | PROGRAM/ERASE.....                                   | 205        |
| 17.7      | EMBEDDED BOOT LOADER .....                           | 205        |
| 17.8      | FLASH MEMORY CONTROLLER (FMC).....                   | 206        |
| 17.8.1    | CODE SECURITY (CS).....                              | 206        |
| 17.8.2    | PROGRAM FLASH MEMORY.....                            | 206        |
| 17.8.3    | ERASE .....                                          | 207        |
| 17.8.3.1  | PAGE ERASE .....                                     | 207        |
| 17.8.3.2  | MASS ERASE.....                                      | 207        |
| 17.9      | READ PROTECTION.....                                 | 207        |
| 17.10     | HW CHECKSUM.....                                     | 207        |
| 17.11     | FMC REGISTERS.....                                   | 208        |
| 17.11.1   | Flash Low Power Control register (FLASH_LPCTRL)..... | 208        |

|           |                                                   |            |
|-----------|---------------------------------------------------|------------|
| 17.11.2   | Flash Status register (FLASH_STATUS) .....        | 208        |
| 17.11.3   | Flash Control register (FLASH_CTRL) .....         | 208        |
| 17.11.4   | Flash Data register (FLASH_DATA) .....            | 209        |
| 17.11.5   | Flash Address register (FLASH_ADDR) .....         | 209        |
| 17.11.6   | Flash Checksum register (FLASH_CHKSUM) .....      | 209        |
| <b>18</b> | <b>SERIAL-WIRE DEBUG (SWD) .....</b>              | <b>210</b> |
| 18.1      | OVERVIEW .....                                    | 210        |
| 18.2      | FEATURES .....                                    | 210        |
| 18.3      | PIN DESCRIPTION .....                             | 210        |
| 18.4      | DEBUG NOTE .....                                  | 210        |
| 18.4.1    | LIMITATIONS .....                                 | 210        |
| 18.4.2    | DEBUG RECOVERY .....                              | 210        |
| 18.4.3    | INTERNAL PULL-UP/DOWN RESISTORS on SWD PINS ..... | 210        |
| <b>19</b> | <b>DEVELOPMENT TOOL .....</b>                     | <b>212</b> |
| 19.1      | SN-LINK-V3 .....                                  | 213        |
| 19.2      | SN32F760 STARTER-KIT .....                        | 214        |
| <b>20</b> | <b>ELECTRICAL CHARACTERISTIC .....</b>            | <b>216</b> |
| 20.1      | ABSOLUTE MAXIMUM RATING .....                     | 216        |
| 20.2      | ELECTRICAL CHARACTERISTIC .....                   | 216        |
| 20.3      | CHARACTERISTIC GRAPHS .....                       | 218        |
| <b>21</b> | <b>FLASH ROM PROGRAMMING PIN .....</b>            | <b>220</b> |
| <b>22</b> | <b>PACKAGE INFORMATION .....</b>                  | <b>221</b> |
| 22.1      | LQFP 80 PIN .....                                 | 221        |
| 22.2      | LQFP 64 PIN .....                                 | 222        |
| 22.3      | LQFP 48 PIN .....                                 | 223        |
| 22.4      | QFN 46 PIN .....                                  | 224        |
| 22.5      | QFN 33 PIN 5x5 .....                              | 225        |
| <b>23</b> | <b>MARKING DEFINITION .....</b>                   | <b>226</b> |
| 23.1      | INTRODUCTION .....                                | 226        |
| 23.2      | MARKING INDETIFICATION SYSTEM .....               | 226        |
| 23.3      | MARKING EXAMPLE .....                             | 227        |
| 23.4      | DATECODE SYSTEM .....                             | 228        |

# 1 PRODUCT OVERVIEW

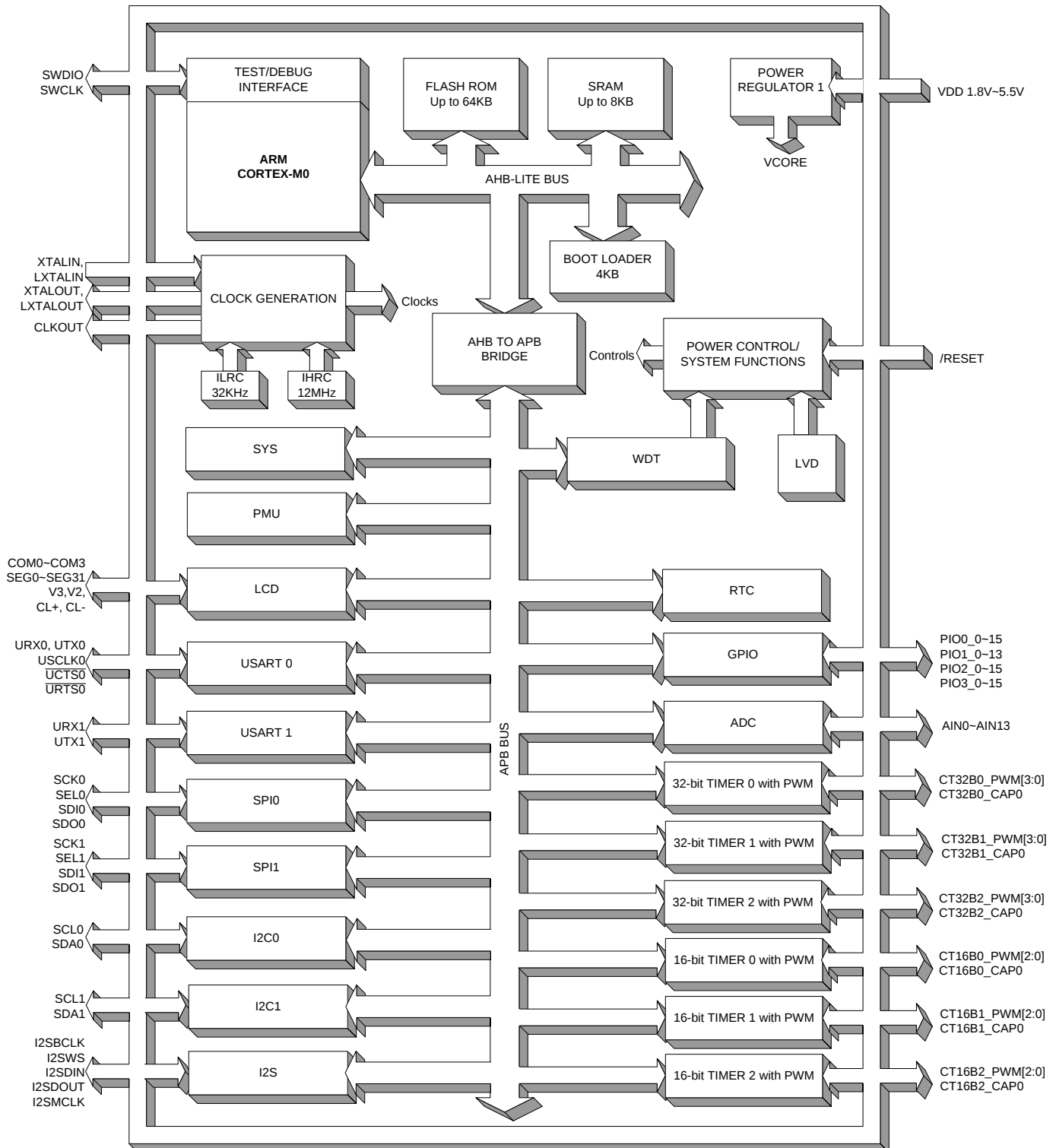
## 1.1 FEATURES

- ◆ **Memory configuration**  
Up to 64KB on-chip Flash programming memory.  
Up to 8KB SRAM.  
4KB Boot ROM
- ◆ **Operation Frequency up to 50MHz**
- ◆ **Interrupt sources**  
ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
- ◆ **I/O pin configuration**  
Up to 64 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors.  
GPIO pins can be used as edge and level sensitive interrupt sources.  
High-current source driver (20 mA)
- ◆ **Programmable Watchdog Timer (WDT)**  
Programmable watchdog frequency with watchdog clock source and divider.
- ◆ **System tick timer**  
24-bit timer.  
The system tick timer clock is fixed to the frequency of the system clock.  
The SysTick timer is intended to generate a fixed 10-ms interrupt.
- ◆ **Hardware divider**
- ◆ **Real-Time Clock (RTC)**
- ◆ **LVD with separate thresholds**  
Reset: 1.65V for V<sub>CORE</sub>  
Reset: 1.8V/2.0V/2.4V/2.7V/3.0V/3.6V for VDD  
Interrupt: 1.8V/2.0V/2.4V/2.7V/3.0V/3.6V for VDD
- ◆ **Fcpu (Instruction cycle)**  
 $F_{CPU} = F_{HCLK} = F_{SYSCLK}/1, F_{SYSCLK}/2, F_{SYSCLK}/4, \dots, F_{SYSCLK}/512.$
- ◆ **Operating modes**  
Normal, Sleep, and Deep-sleep
- ◆ **Serial Wire Debug (SWD)**
- ◆ **In-Circuit Programming (ICP) supported**
- ◆ **Timer**  
3 16-bit and 3 32-bit general purpose timers with a total of 6 capture inputs and 21 PWMs.
- ◆ **Working voltage 1.8V ~ 5.5V**
- ◆ **ADC**  
14-channel 12-bit SAR ADC  
Temperature sensor inside
- ◆ **Interface**  
-Two I2C controllers supporting I2C-bus specification with multiple address recognition and monitor mode.  
- USART controller with fractional baud rate generation, and EIA-485 support.  
- UART controller with fractional baud rate generation.  
-Two SPI controllers with SSP features and multi-protocol capabilities.  
-I2S Function with mono and stereo audio data supported, MSB justified data format supported, and can operate as either master or slave.
- ◆ **System clocks**  
-External high clock: Crystal type 10MHz~25MHz  
-External low clock: Crystal type 32.768 KHz  
-Internal high clock: RC type 12 MHz  
-Internal low clock: RC type 32 KHz  
-PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal.  
-Clock output function which can reflect the internal high/low RC oscillator, HCLK, PLL output, and external high/low clock.
- ◆ **LCD driver**  
Support both R-type and C-type  
4 common x 32 segment  
1/3 or 1/2 bias voltage  
Multiple C-type LCD Voltage: 2.7 ~5.0V  
R-type optional-bias resistor: 400K, 200K, 100K, 35K  
Support 1/2 duty, 1/3 duty, 1/4 duty
- ◆ **In-System Programming (ISP) supported**
- ◆ **Package (Chip form support)**  
LQFP 80/64/48 pin  
QFN 46/33 pin

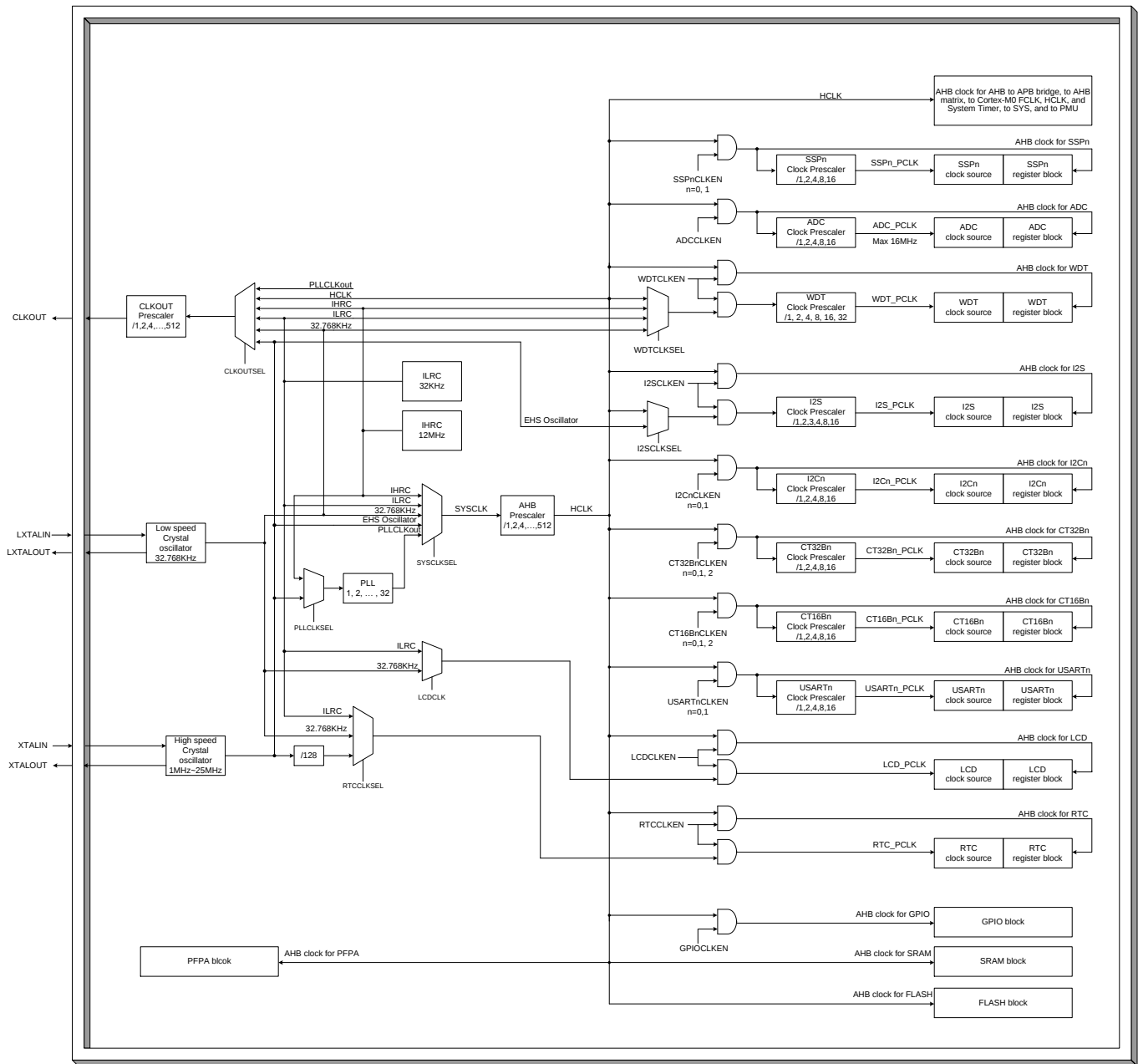
 **Features Selection Table**

| Chip      | ROM  | RAM | Boot Loader | F <sub>CPU</sub><br>(Max MHz) | TIMER                | USART             | SPI | I2C | I2S | PWM | 12-bit ADC | LCD  | GPIO with Wakeup | Package |
|-----------|------|-----|-------------|-------------------------------|----------------------|-------------------|-----|-----|-----|-----|------------|------|------------------|---------|
| SN32F769F | 64KB | 8KB | 4KB         | 50 MHz                        | 16-bitx3<br>32-bitx3 | USARTx1<br>UARTx1 | 2   | 2   | 1   | 21  | 14CH       | 4x32 | 64               | LQFP80  |
| SN32F768F | 64KB | 8KB | 4KB         | 50 MHz                        | 16-bitx3<br>32-bitx3 | USARTx1<br>UARTx1 | 2   | 2   | 1   | 21  | 11CH       | 4x28 | 57               | LQFP64  |
| SN32F767F | 64KB | 8KB | 4KB         | 50 MHz                        | 16-bitx3<br>32-bitx3 | USARTx1<br>UARTx1 | 2   | 2   | 1   | 21  | 8CH        | 4x18 | 42               | LQFP48  |
| SN32F766J | 64KB | 8KB | 4KB         | 50 MHz                        | 16-bitx3<br>32-bitx3 | USARTx1<br>UARTx1 | 2   | 2   | 1   | 21  | 7CH        | 4x17 | 40               | QFN46   |
| SN32F765J | 64KB | 8KB | 4KB         | 50 MHz                        | 16-bitx3<br>32-bitx3 | UARTx2            | 2   | 2   | -   | 21  | 4CH        | -    | 26               | QFN33   |
| SN32F759F | 32KB | 4KB | 4KB         | 50 MHz                        | 16-bitx3<br>32-bitx3 | USARTx1<br>UARTx1 | 2   | 2   | 1   | 21  | 14CH       | 4x32 | 64               | LQFP80  |
| SN32F758F | 32KB | 4KB | 4KB         | 50 MHz                        | 16-bitx3<br>32-bitx3 | USARTx1<br>UARTx1 | 2   | 2   | 1   | 21  | 11CH       | 4x28 | 57               | LQFP64  |
| SN32F757F | 32KB | 4KB | 4KB         | 50 MHz                        | 16-bitx3<br>32-bitx3 | USARTx1<br>UARTx1 | 2   | 2   | 1   | 21  | 8CH        | 4x18 | 42               | LQFP48  |
| SN32F756J | 32KB | 4KB | 4KB         | 50 MHz                        | 16-bitx3<br>32-bitx3 | USARTx1<br>UARTx1 | 2   | 2   | 1   | 21  | 7CH        | 4x17 | 40               | QFN46   |
| SN32F755J | 32KB | 4KB | 4KB         | 50 MHz                        | 16-bitx3<br>32-bitx3 | UARTx2            | 2   | 2   | -   | 21  | 4CH        | -    | 26               | QFN33   |

## 1.2 SYSTEM BLOCK DIAGRAM

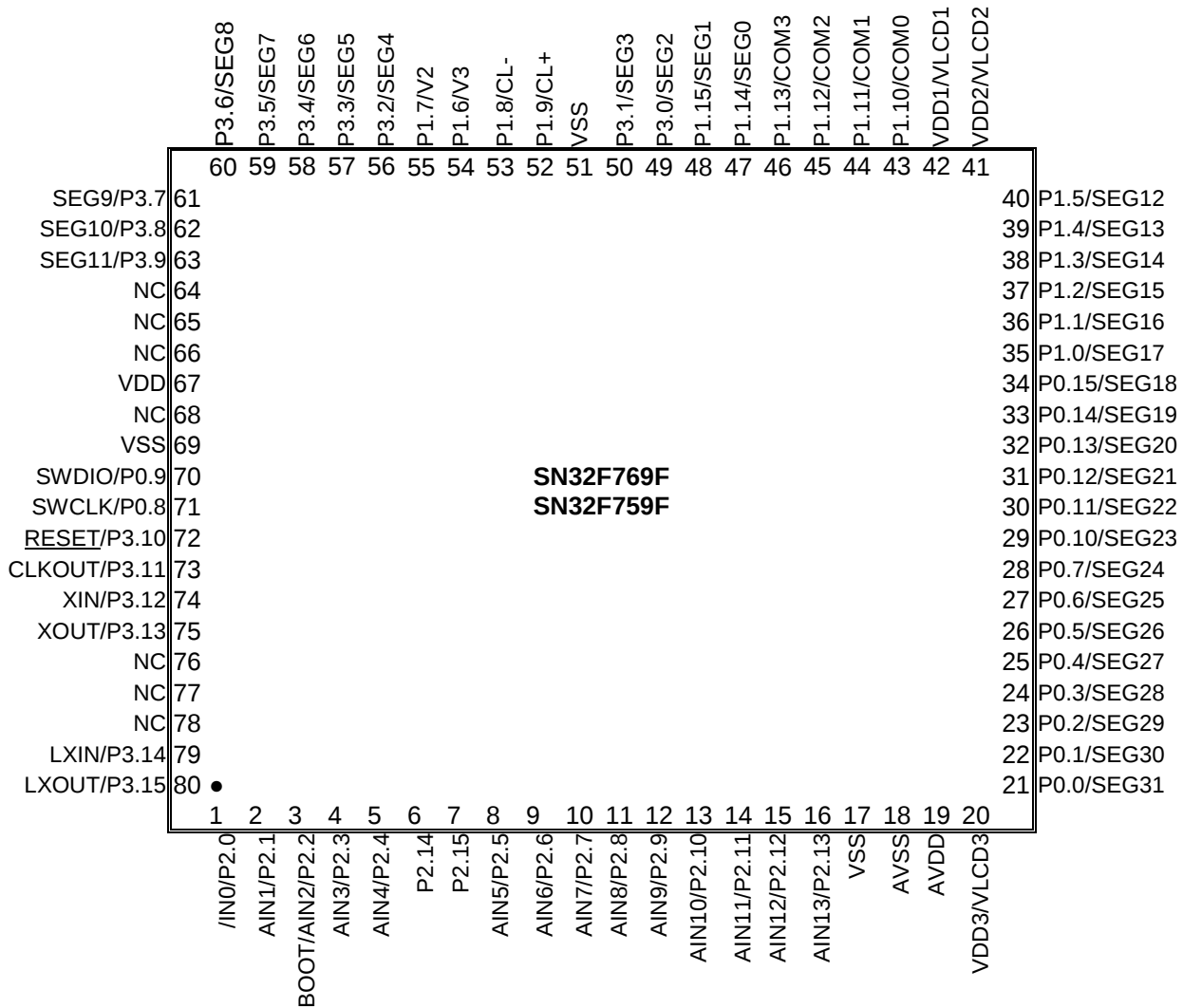


## 1.3CLOCK GENERATION BLOCK DIAGRAM



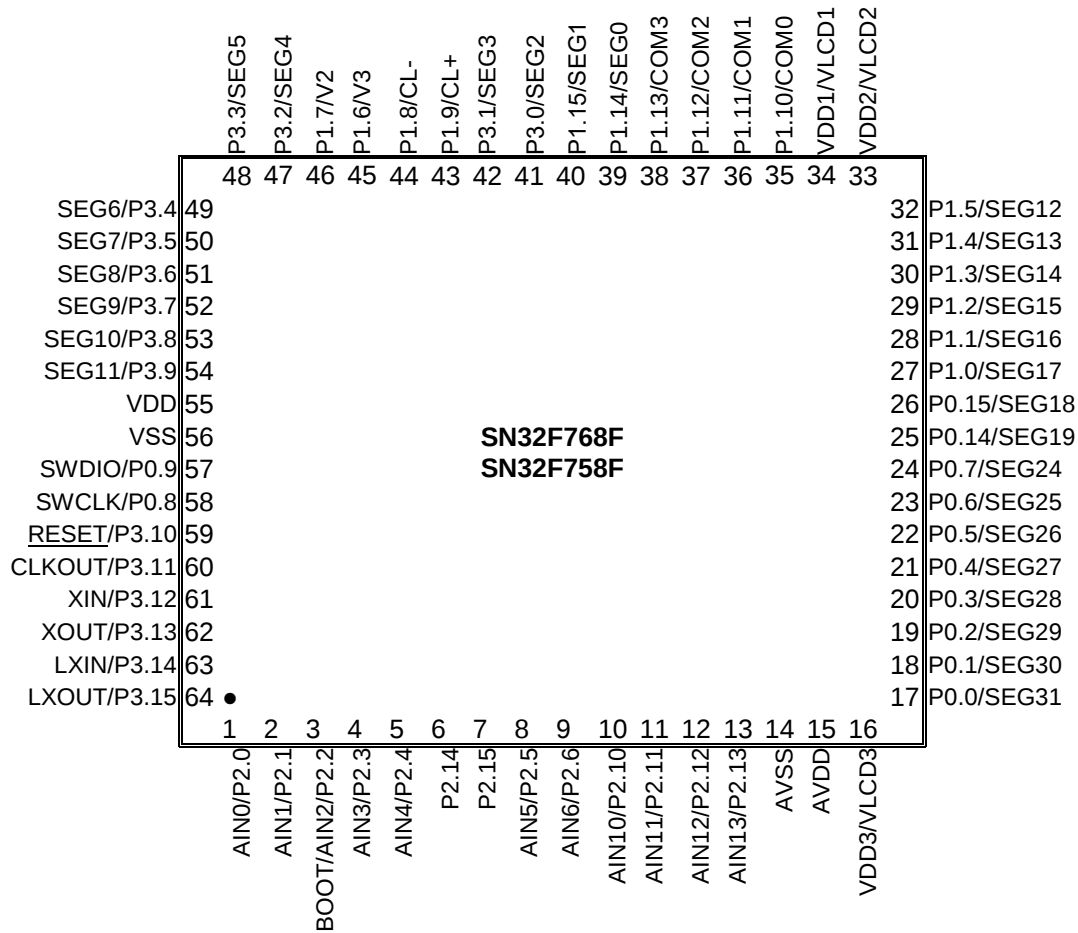
## 1.4 PIN ASSIGNMENT

SN32F769/759F (LQFP 80 pins)



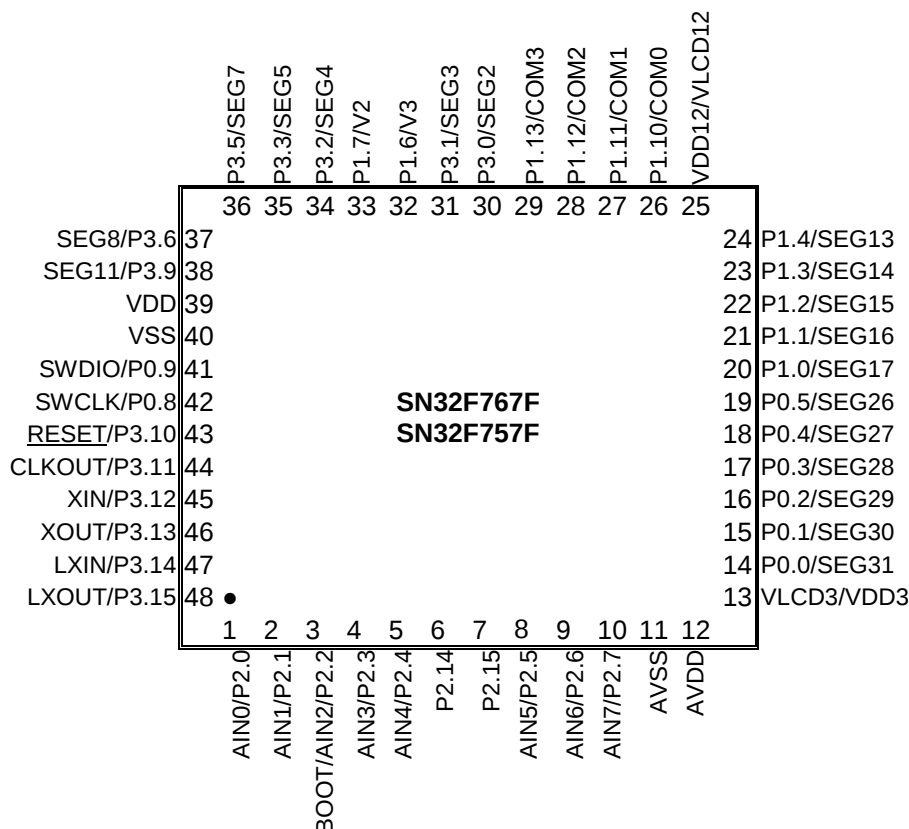
\* **Note:** SONiX provide Boot loader to check the status of P2.2 (BOOT pin) during boot procedure. If BOOT pin is Low during Boot procedure, MCU will execute code in Boot loader instead of User code. We strongly recommended NOT using BOOT pin as output pin to drive the LED, otherwise, the BOOT pin status may be low during boot procedure.

**SN32F768/758F (LQFP 64 pins)**



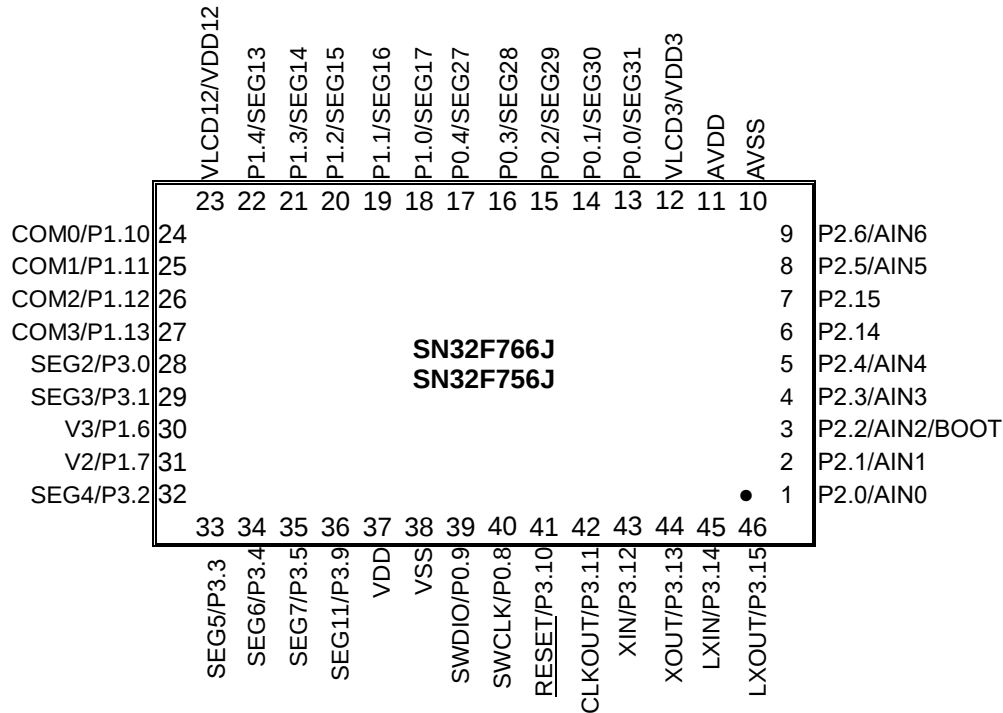
- \* **Note:**
1. The pins which are not pin-out shall be set correctly to decrease power consumption in low-power modes. Strongly recommended to set these pins as input pull-up.
  2. SONiX provide Boot loader to check the status of P2.2 (BOOT pin) during boot procedure. If BOOT pin is Low during Boot procedure, MCU will execute code in Boot loader instead of User code. We strongly recommended NOT using BOOT pin as output pin to drive the LED, otherwise, the BOOT pin status may be low during boot procedure.

**SN32F767/757 (LQFP 48 pins)**



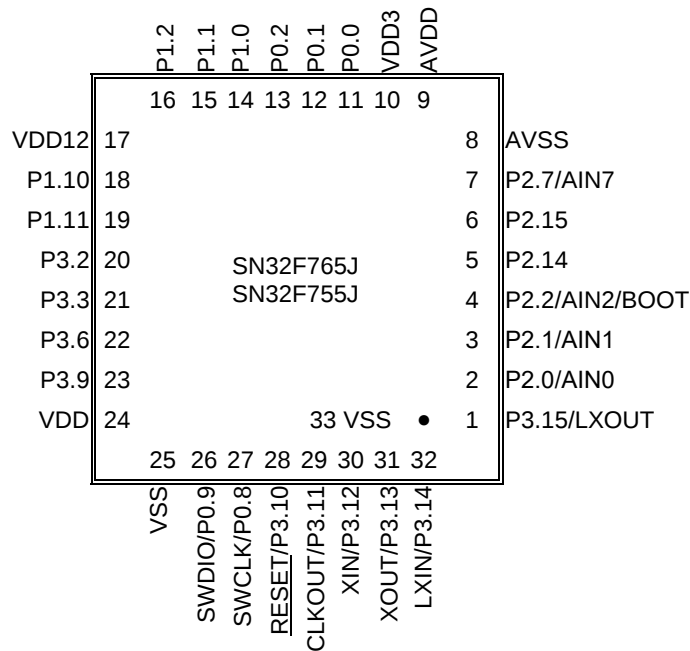
- \* **Note:**
1. The pins which are not pin-out shall be set correctly to decrease power consumption in low-power modes. Strongly recommended to set these pins as input pull-up.
  2. SONiX provide Boot loader to check the status of P2.2 (BOOT pin) during boot procedure. If BOOT pin is Low during Boot procedure, MCU will execute code in Boot loader instead of User code. We strongly recommended NOT using BOOT pin as output pin to drive the LED, otherwise, the BOOT pin status may be low during boot procedure.

**SN32F766/756 (QFN 46 pins)**



- \* **Note:**
1. The pins which are not pin-out shall be set correctly to decrease power consumption in low-power modes. Strongly recommended to set these pins as input pull-up.
  2. SONiX provide Boot loader to check the status of P2.2 (BOOT pin) during boot procedure. If BOOT pin is Low during Boot procedure, MCU will execute code in Boot loader instead of User code. We strongly recommended NOT using BOOT pin as output pin to drive the LED, otherwise, the BOOT pin status may be low during boot procedure.

**SN32F765/755 (QFN 33 pins)**



- \* **Note:**
1. The pins which are not pin-out shall be set correctly to decrease power consumption in low-power modes. Strongly recommended to set these pins as input pull-up.
  2. SONiX provide Boot loader to check the status of P2.2 (BOOT pin) during boot procedure. If BOOT pin is Low during Boot procedure, MCU will execute code in Boot loader instead of User code. We strongly recommended NOT using BOOT pin as output pin to drive the LED, otherwise, the BOOT pin status may be low during boot procedure.

## 1.5 PIN DESCRIPTIONS

| PIN NAME           | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                        |
|--------------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VDD, VSS           | P    | Power supply input pins for digital circuit.                                                                                                                                                                                                                                                                                                                       |
| AVDD, AVSS         | P    | Power supply input pins for analog circuit.                                                                                                                                                                                                                                                                                                                        |
| VDD1/VLCD1         | P    | I/O and LCD driver power input pins for P1.6~P1.15 and P3.0~P3.9.<br>This power input used for I/O power must be equal to VDD.<br>This power input shall not be floating.                                                                                                                                                                                          |
| VDD2/VLCD2         | P    | I/O and LCD driver power input pins for P0.10~P0.15 and P1.0~P1.5.<br>VDD2/VLCD2 is the I/O and LCD driver power input pin for P0.10~P0.15 and P1.0~P1.5. If VDD2 voltage is lower than VDD, user should manually force to set the I/O port P1.6 and P1.7 as input pull-down state in case of internal power collision.<br>This power input shall not be floating. |
| VDD12/VLCD12       | P    | Double bonding pins with VDD1 and VDD2.<br>This power input used for I/O power must be equal to VDD.<br>This power input shall not be floating.                                                                                                                                                                                                                    |
| VDD3/VLCD3         | P    | I/O and LCD driver power input pins for P0.0~P0.7.<br>If VDD3 voltage is lower than VDD, user should manually force to set the I/O port P1.6 and P1.7 as input pull-down state in case of internal power collision.<br>This power input shall not be floating.                                                                                                     |
| CL+, CL-           | P    | C-Type LCD charge pump capacitor                                                                                                                                                                                                                                                                                                                                   |
| V3                 | P    | 2/3 VLCD bias voltage                                                                                                                                                                                                                                                                                                                                              |
| V2                 | P    | 1/3 VLCD bias voltage                                                                                                                                                                                                                                                                                                                                              |
| P0.0~P0.7          | I/O  | <b>P0.0~P0.7</b> — Port 0 bi-direction pin.<br>Schmitt trigger structure and built-in pull-up/pull-down resisters as input mode.                                                                                                                                                                                                                                   |
| P0.8/SWCLK         | I/O  | <b>P0.8</b> — Port 0.8 bi-direction pin.<br>Schmitt trigger structure and built-in pull-up/pull-down resisters as input mode.<br>Built-in wakeup function.<br><b>SWCLK</b> — Serial Wire Clock pin.                                                                                                                                                                |
| P0.9/SWDIO         | I/O  | <b>P0.9</b> — Port 0.9 bi-direction pin.<br>Schmitt trigger structure and built-in pull-up/pull-down resisters as input mode.<br>Built-in wakeup function.<br><b>SWDIO</b> — Serial Wire Data input/output pin.                                                                                                                                                    |
| P0.10~P0.15        | I/O  | <b>P0.10~P0.15</b> — Port 0 bi-direction pin.<br>Schmitt trigger structure and built-in pull-up/pull-down resisters as input mode.                                                                                                                                                                                                                                 |
| P1.0~P1.15         | I/O  | <b>P1.0~P1.15</b> — Port 1 bi-direction pin.<br>Schmitt trigger structure and built-in pull-up/pull-down resisters as input mode.                                                                                                                                                                                                                                  |
| P2.0~P2.1/AIN0~1   | I/O  | <b>P2.0~P2.1</b> — Port 2 bi-direction pin.<br>Schmitt trigger structure and built-in pull-up/pull-down resisters as input mode.<br><b>AIN0~AIN1</b> — ADC channel input 0~13 pins.                                                                                                                                                                                |
| P2.2/AIN2/BOOT     | I/O  | <b>P2.0~P2.1</b> — Port 2 bi-direction pin.<br>Schmitt trigger structure and built-in pull-up/pull-down resisters as input mode.<br><b>AIN0~AIN1</b> — ADC channel input 0~13 pins.                                                                                                                                                                                |
|                    | I    | <b>BOOT</b> — Internal pull-up in Boot loader, tie LOW to keep in Boot loader or left HIGH to exit Boot loader and execute User program at boot time.                                                                                                                                                                                                              |
| P2.3~P2.13/AIN3~13 | I/O  | <b>P2.3~P2.13</b> — Port 2 bi-direction pin.<br>Schmitt trigger structure and built-in pull-up/pull-down resisters as input mode.<br><b>AIN3~AIN13</b> — ADC channel input 0~13 pins.                                                                                                                                                                              |
| P2.14              | I/O  | <b>P2.14</b> — Port 2.14 bi-direction pin.<br>Schmitt trigger structure and built-in pull-up/pull-down resisters as input mode.                                                                                                                                                                                                                                    |
| P2.15              | I/O  | <b>P2.15</b> — Port 2.15 bi-direction pin.                                                                                                                                                                                                                                                                                                                         |

|                     |     |                                                                                                                                                                                                                                        |
|---------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                     |     | Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode.                                                                                                                                                      |
| P3.0~P3.9           | I/O | <b>P3.0~P3.9</b> — Port 3 bi-direction pin.<br>Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode.                                                                                                       |
| P3.10/ <u>RESET</u> | I/O | <b>P3.10</b> — Port 3.10 bi-direction pin.<br>Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode.<br><b>RESET</b> — External Reset input. Schmitt trigger structure, active “Low”, normally stay “High”. |
| P3.11/CLKOUT        | I/O | <b>P3.11</b> — Port 3.11 bi-direction pin.<br>Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode.<br><b>CLKOUT</b> — Clockout pin.                                                                       |
| P3.12/XIN           | I/O | <b>P3.12</b> — Port 3.12 bi-direction pin.<br>Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode.<br><b>XIN</b> — External high-speed X’tal input pin.                                                   |
| P3.13/XOUT          | I/O | <b>P3.13</b> — Port 3.13 bi-direction pin.<br>Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode.<br><b>XOUT</b> — External high-speed X’tal output pin.                                                 |
| P3.14/LXIN          | I/O | <b>P3.14</b> — Port 3.14 bi-direction pin.<br>Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode.<br><b>LXIN</b> — External low-speed X’tal input pin.                                                   |
| P3.15/LXOUT         | I/O | <b>P3.15</b> — Port 3.15 bi-direction pin.<br>Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode.<br><b>LXOUT</b> — External low-speed X’tal output pin.                                                 |

Please refer to [Peripheral Function Pin Assignment \(PFPA\)](#) chapters for setting of each GPIOs.

| Pin Name | Shared pins                                                                                              |
|----------|----------------------------------------------------------------------------------------------------------|
| P0.0     | SEG31 / URXD0 / CT32B0_CAP0 / SCL1 / MISO0<br>CT16B0_PWM0 / CT16B2_PWM1 / CT32B2_PWM2                    |
| P0.1     | SEG30 / UTXD0 / SDA1 / MOSI0<br>CT16B0_PWM1 / CT16B2_PWM2 / CT32B1_PWM0                                  |
| P0.2     | SEG29 / SCL0 / MISO0 / SEL1<br>CT16B0_CAP0 / CT32B1_CAP0 / CT16B2_PWM0/CT32B2_PWM1                       |
| P0.3     | SEG28 / SDA0 / MOSI0 /<br>CT16B2_CAP0 / CT32B2_PWM2 / CT32B0_PWM3 / CT32B2_PWM0                          |
| P0.4     | SEG27 / URXD0 / SCK0 / MISO1<br>CT16B0_PWM1 / CT32B0_PWM0 / CT32B1_PWM1                                  |
| P0.5     | SEG26 / UTXD0 / SEL0 / MOSI1<br>CT16B1_PWM0 / CT32B0_PWM2 / CT32B1_PWM2                                  |
| P0.6     | SEG25 / UTXD1 / SCL1 / MISO0<br>CT16B1_PWM2 / CT32B1_PWM3 / C32B2_PWM3                                   |
| P0.7     | SEG24 / URXD1 / SDA1 / MOSI0 / SCK1<br>CT16B1_CAP0 / CT32B0_PWM3 / CT32B1_PWM3                           |
| P0.8     | SWCLK / CT16B0_CAP0 / CT32B1_CAP0<br>CT16B1_PWM1 / CT32B0_PWM1 / CT32B1_PWM2 / CT32B2_PWM0               |
| P0.9     | SWDIO / CT32B0_CAP0 / CT32B2_CAP0<br>CT16B0_PWM2 / CT16B2_PWM1 / CT32B0_PWM2 / CT32B1_PWM0 / CT32B2_PWM2 |
| P0.10    | SEG23 / I2SDIN / SDA0 / SEL0 / MISO1<br>CT16B0_PWM1 / CT16B1_PWM0 / CT32B2_CAP0                          |
| P0.11    | SEG22 / I2SDOUT / SCK0<br>CT16B0_PWM2 / CT32B0_PWM0 / CT16B1_PWM1/CT32B1_PWM2                            |
| P0.12    | SEG21 / URXD1 / SEL0 / MOSI1 / I2SMCLK<br>CT16B1_PWM1 / CT16B1_CAP0                                      |
| P0.13    | SEG20 / UTXD1 / SCK0 / SEL1 / I2SBCLK<br>CT16B2_CAP0 / CT32B2_PWM0                                       |
| P0.14    | SEG19 / MOSI0 / SCK1 / I2SWS                                                                             |

|       |                                                                     |
|-------|---------------------------------------------------------------------|
|       | CT32B2_PWM1 / CT16B2_PWM0 / CT32B0_PWM1                             |
| P0.15 | SEG18 / SCL0 / MISO0                                                |
|       | CT32B1_PWM1 / CT16B1_PWM2 / CT32B0_PWM3 / CT32B2_PWM1 / CT32B1_CAP0 |
| P1.0  | SEG17 / URXD1 / SDA1 / MISO0 / SEL1                                 |
|       | CT16B0_CAP0 / CT16B2_PWM2 / CT32B2_PWM3                             |
| P1.1  | SEG16 / UTXD1 / SCL1 / MOSI0 / SCK1                                 |
|       | CT16B0_PWM0 / CT32B2_PWM0 / CT32B0_CAP0                             |
| P1.2  | SEG15 / UTXD0 / SDA0 / MOSI1                                        |
|       | CT16B1_PWM2 / CT32B1_PWM1 / CT32B0_PWM3 / CT32B1_PWM3               |
| P1.3  | SEG14 / URXD0 / SCL0 / MISO1                                        |
|       | CT32B1_CAP0 / CT16B1_PWM1 / CT32B1_PWM0                             |
| P1.4  | SEG13 / UTXD1 / SDA0 / SCK0 / SEL1                                  |
|       | CT16B2_PWM1 / CT16B2_PWM0 / CT32B2_CAP0                             |
| P1.5  | SEG12 / URXD1 / SCL0 / SEL0                                         |
|       | CT16B2_CAP0 / CT32B0_PWM1 / CT32B2_PWM1                             |
| P1.6  | V3 / UCTS0 / I2SDIN / MOSI1                                         |
|       | CT16B0_PWM2 / CT32B1_PWM2 / CT32B2_PWM2 / CT32B1_CAP0               |
| P1.7  | V2 / USCLK0 / I2SDOUT / SEL1                                        |
|       | CT16B1_CAP0 / CT32B1_PWM3 / CT32B2_PWM0 / CT32B2_PWM3               |
| P1.8  | CL- / URTS0 / SDA1 / I2SMCLK                                        |
|       | CT16B0_PWM0 / CT16B2_CAP0 / CT32B0_PWM0                             |
| P1.9  | CL+ / SCL1 / I2SBCLK                                                |
|       | CT16B1_PWM2 / CT16B1_PWM0 / CT32B0_PWM2                             |
| P1.10 | COM0 / MISO1 / I2SWS                                                |
|       | CT16B1_PWM3 / CT16B1_PWM1 / CT32B1_PWM1                             |
| P1.11 | COM1 / SEL0 / SCK1                                                  |
|       | CT16B1_CAP0 / CT16B2_PWM1 / CT32B0_PWM1                             |
| P1.12 | COM2 / SCK0                                                         |
|       | CT16B0_PWM0 / CT16B0_PWM2 / CT16B2_PWM2 / CT32B0_PWM3               |
| P1.13 | COM3 / URXD1 / SDA0 / MOSI1                                         |
|       | CT16B0_PWM1 / CT32B1_PWM0 / CT32B2_CAP0                             |
| P1.14 | SEG0 / UTXD1 / SCL0 / MISO0 / SEL1                                  |
|       | CT16B1_PWM2 / CT32B0_PWM0 / CT32B0_PWM2                             |
| P1.15 | SEG1 / URXD1 / MOSI0 / SCK1                                         |
|       | CT16B1_PWM0 / CT32B0_PWM0 / CT32B2_PWM0                             |
| P2.0  | AIN0 / I2SDIN / SEL0 / MOSI1                                        |
|       | CT16B0_CAP0 / CT16B1_PWM0 / CT32B0_PWM2                             |
| P2.1  | AIN1 / MISO0 / MISO1 / SEL1 / I2SWS                                 |
|       | CT16B1_CAP0 / CT16B2_PWM1 / CT32B1_PWM1                             |
| P2.2  | AIN2 / MOSI0 / SCK1 / I2SMCLK                                       |
|       | CT16B2_CAP0 / CT16B0_PWM1 / CT32B0_PWM3                             |
| P2.3  | AIN3 / SCK0                                                         |
|       | CT16B0_PWM0 / CT16B1_PWM2 / CT32B0_PWM0 / CT32B2_PWM3 / CT32B0_CAP0 |
| P2.4  | AIN4 / CT32B1_CAP0                                                  |
|       | CT16B0_PWM2 / CT16B1_PWM1 / CT16B2_PWM2 / CT32B0_PWM1 / CT32B1_PWM3 |
| P2.5  | AIN5 / I2SDIN                                                       |
|       | CT16B2_PWM0 / CT32B1_PWM2 / CT32B2_CAP0                             |
| P2.6  | AIN6 / I2SMCLK                                                      |
|       | CT16B2_PWM1 / CT32B1_PWM0                                           |
| P2.7  | AIN7 / I2SWS                                                        |
|       | CT16B1_PWM2 / CT32B2_PWM1                                           |
| P2.8  | AIN8 / I2SDOUT                                                      |
|       | CT16B1_PWM1 / CT32B1_PWM1 / CT32B2_PWM3                             |
| P2.9  | AIN9 / I2SWS                                                        |
|       | CT16B1_CAP0 / CT16B2_PWM0 / CT32B2_PWM3                             |
| P2.10 | AIN10 / I2SBCLK                                                     |

|       |                                                                     |
|-------|---------------------------------------------------------------------|
|       | CT16B0_PWM2 / CT16B2_PWM2 / CT32B1_CAP0                             |
| P2.11 | AIN11 / I2SBCLK                                                     |
|       | CT16B0_PWM1 / CT32B0_PWM2 / CT32B2_PWM0                             |
| P2.12 | AIN12 / MISO0 / MISO1 / I2SDOUT                                     |
|       | CT16B1_PWM0 / CT32B0_PWM3 / CT32B1_PWM2 / CT32B2_CAP0               |
| P2.13 | AIN13 / MOSI0 / SCK1                                                |
|       | CT16B0_CAP0 / CT32B0_PWM1 / CT32B1_PWM3 / CT32B2_PWM1               |
| P2.14 | SCK0 / SEL1                                                         |
|       | CT16B2_CAP0 / CT32B0_PWM0 / CT32B1_PWM2 / CT32B2_PWM2               |
| P2.15 | SEL0 / MOSI1                                                        |
|       | CT16B0_PWM0 / CT32B1_PWM0 / CT32B2_PWM0 / CT32B2_PWM3 / CT32B0_CAP0 |
| P3.0  | SEG2 / URXD0 / I2SDIN / SCL1 / MISO1                                |
|       | CT16B0_CAP0 / CT16B2_PWM2 / CT32B2_PWM1                             |
| P3.1  | SEG3 / I2SDOUT / UTXD0 / SEL0                                       |
|       | CT16B2_PWM2 / CT16B2_PWM0 / CT32B2_PWM2 / CT32B0_CAP0               |
| P3.2  | SEG4 / UTXD0 / SDA1 / I2SMCLK / SCK0 / MOSI1                        |
|       | CT16B0_CAP0 / CT32B1_PWM0                                           |
| P3.3  | SEG5 / URXD0 / SCL1 / MISO0 / SCK1 / I2SBCLK                        |
|       | CT16B0_PWM0 / CT32B0_CAP0                                           |
| P3.4  | SEG6 / UTXD0 / SDA1 / MOSI0 / MISO1 / I2SWS                         |
|       | CT16B0_PWM1 / CT32B0_PWM3                                           |
| P3.5  | SEG7 / URXD0 / SDA1 / SEL0                                          |
|       | CT16B1_CAP0 / CT16B2_PWM0 / CT16B2_PWM1 / CT32B1_PWM1               |
| P3.6  | SEG8 / URXD1 / SCL1 / SEL1 / SCK0 / I2SBCLK                         |
|       | CT16B2_CAP0 / CT16B0_PWM2                                           |
| P3.7  | SEG9 / SDA0 / SCK1 / I2SMCLK                                        |
|       | CT16B1_PWM0 / CT32B0_PWM2 / CT32B2_PWM1 / CT32B2_CAP0               |
| P3.8  | SEG10 / UTXD1 / I2SDOUT / MOSI1                                     |
|       | CT16B1_PWM2 / CT32B0_PWM1 / CT32B1_CAP0                             |
| P3.9  | SEG11 / I2SDIN / MISO1 / SCL0                                       |
|       | CT16B1_PWM1 / CT32B0_PWM0 / CT32B1_PWM3 / CT32B0_CAP0               |
| P3.10 | RESET / UTXD0 / UTXD1 / SEL0                                        |
|       | CT16B0_CAP0 / CT16B2_PWM0 / CT32B1_PWM1 / CT32B2_PWM3               |
| P3.11 | CLKOUT / URXD0 / SCL0 / SCK0 / SEL1                                 |
|       | CT16B0_PWM0 / CT16B2_PWM2 / CT32B1_PWM3                             |
| P3.12 | XIN / URXD1 / SDA1 / MISO1                                          |
|       | CT16B0_PWM1 / CT16B2_CAP0 / CT32B1_PWM2                             |
| P3.13 | XOUT / UTXD1 / SCL1 / SDA0 / MOSI1                                  |
|       | CT16B1_CAP0 / CT32B0_PWM2 / CT32B2_PWM2                             |
| P3.14 | LXIN / URXD0 / SCL0 / MOSI0 / SCK1                                  |
|       | CT16B1_PWM0 / CT32B0_PWM1 / CT32B2_CAP0                             |
| P3.15 | LXOUT / UTXD0 / SDA0 / MISO0                                        |
|       | CT16B0_PWM2 / CT16B2_PWM1 / CT32B1_PWM0 / CT32B2_PWM2               |

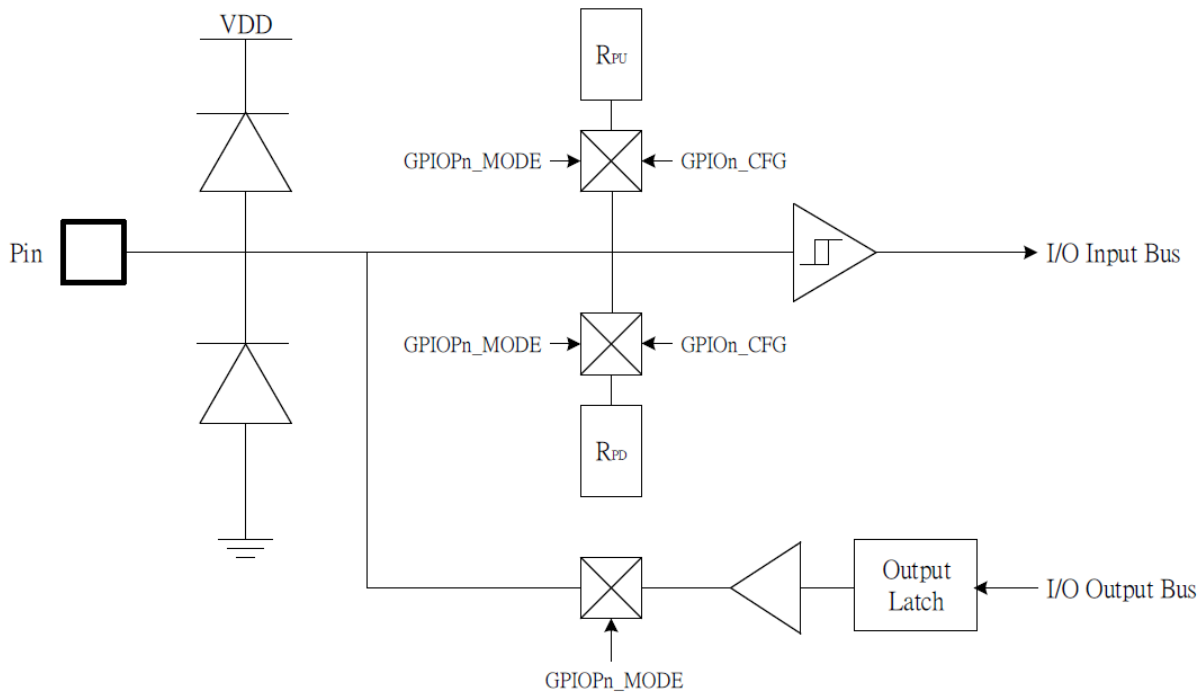
**\* Note:**

1. VDD1/VLCD1 is the I/O and LCD driver power input pin for P1.6~P1.15 and P3.0~P3.9. This power input used for I/O power must be equal to VDD.
2. VDD12/VLCD12 is the double bonding pin with VDD1 and VDD2. This power input used for I/O power must be equal to VDD.
3. VDD2/VLCD2 is the I/O and LCD driver power input pin for P0.10~P0.15 and P1.0~P1.5. If VDD2 voltage is lower than VDD, user should manually force to set the I/O port P1.6 and P1.7 as input pull-down state in case of internal power collision.
4. VDD3/VLCD3 is the I/O and LCD driver power input pin for P0.0~P0.7. If VDD3 voltage is lower than VDD, user should manually force to set the I/O port P1.6 and P1.7 as input pull-down state

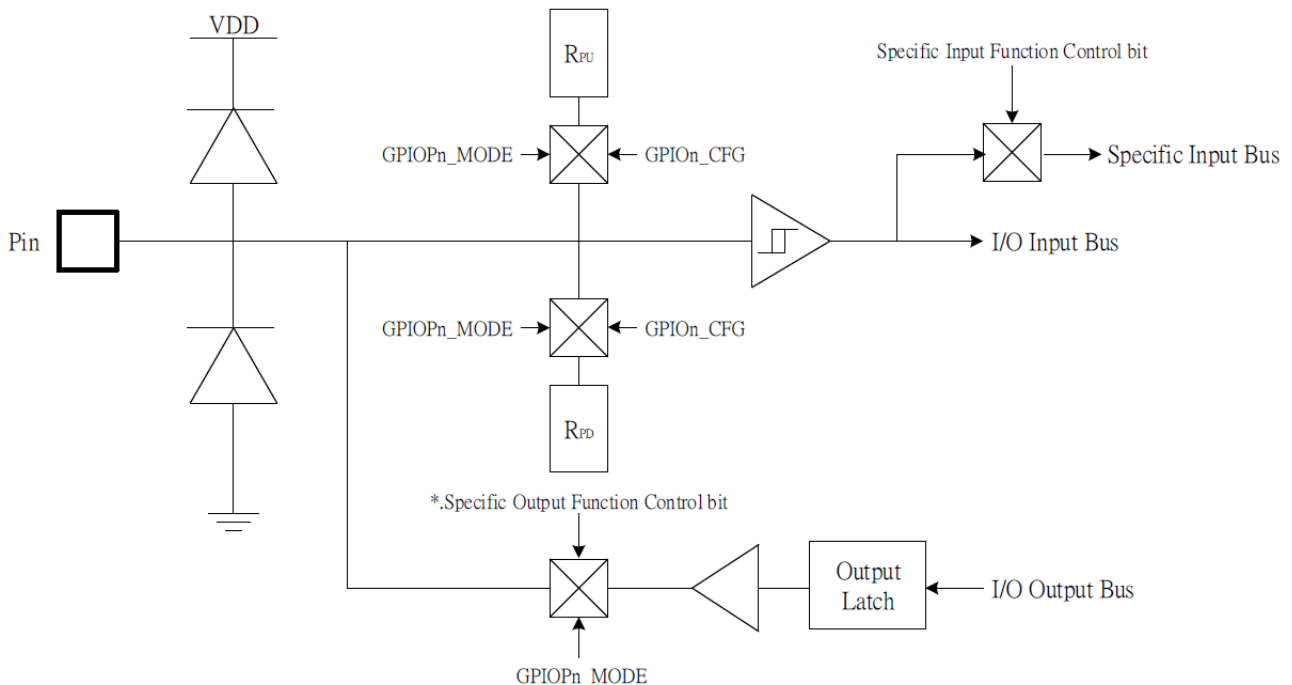
*in case of internal power collision.*  
**5. VDD1/VLCD1, VDD2/VLCD2, VDD3/VLCD3, and VDD12/VLCD12 power input shall not be floating.**

## 1.6 PIN CIRCUIT DIAGRAMS

- **Normal Bi-direction I/O Pin.**

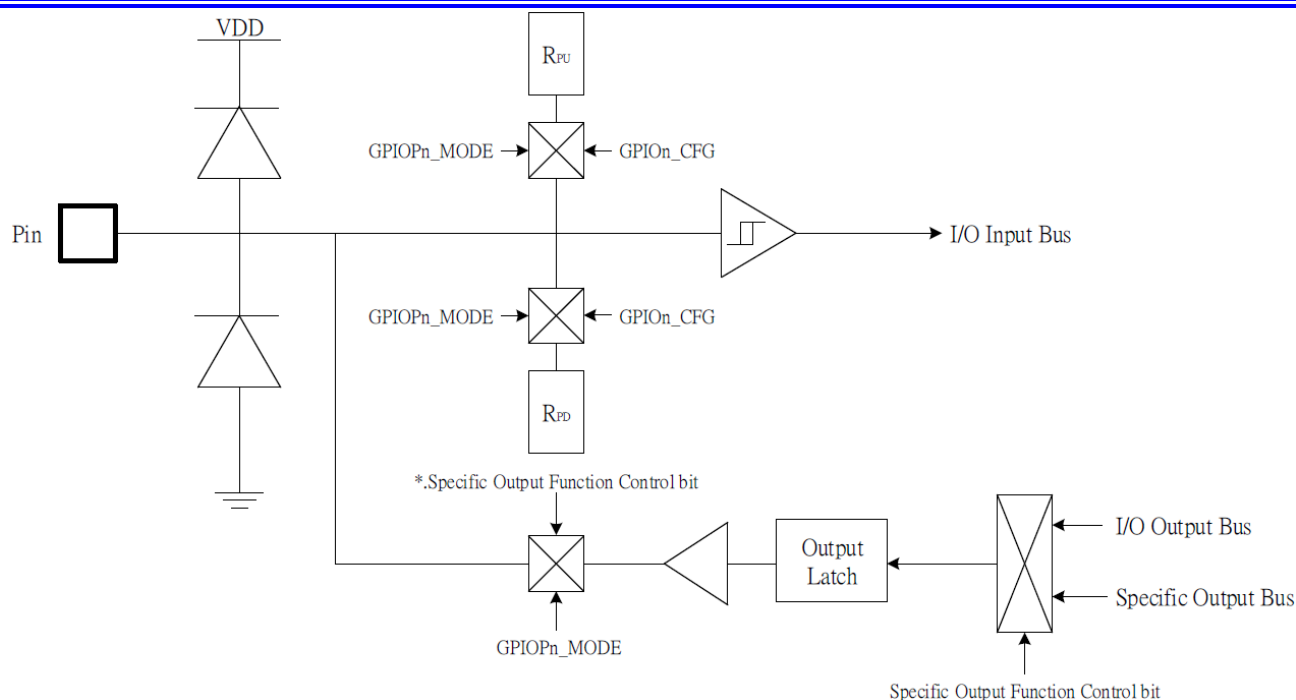


- **Bi-direction I/O Pin Shared with Specific Digital Input Function, e.g. SPI, I2C...**



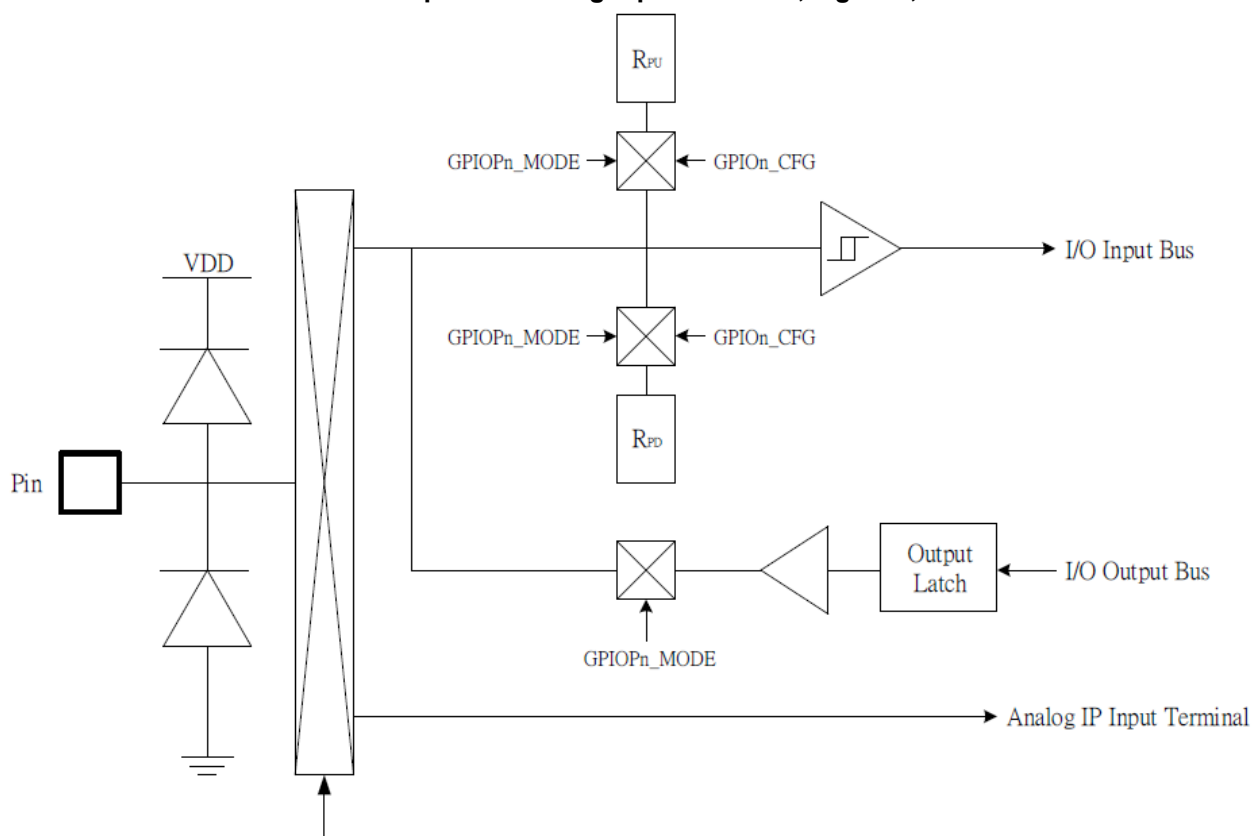
\*. Some specific functions switch I/O direction directly, not through GPIO<sub>n</sub>\_MODE register.

- **Bi-direction I/O Pin Shared with Specific Digital Output Function, e.g. SPI, I2C...**



\*. Some specific functions switch I/O direction directly, not through GPIOn\_MODE register.

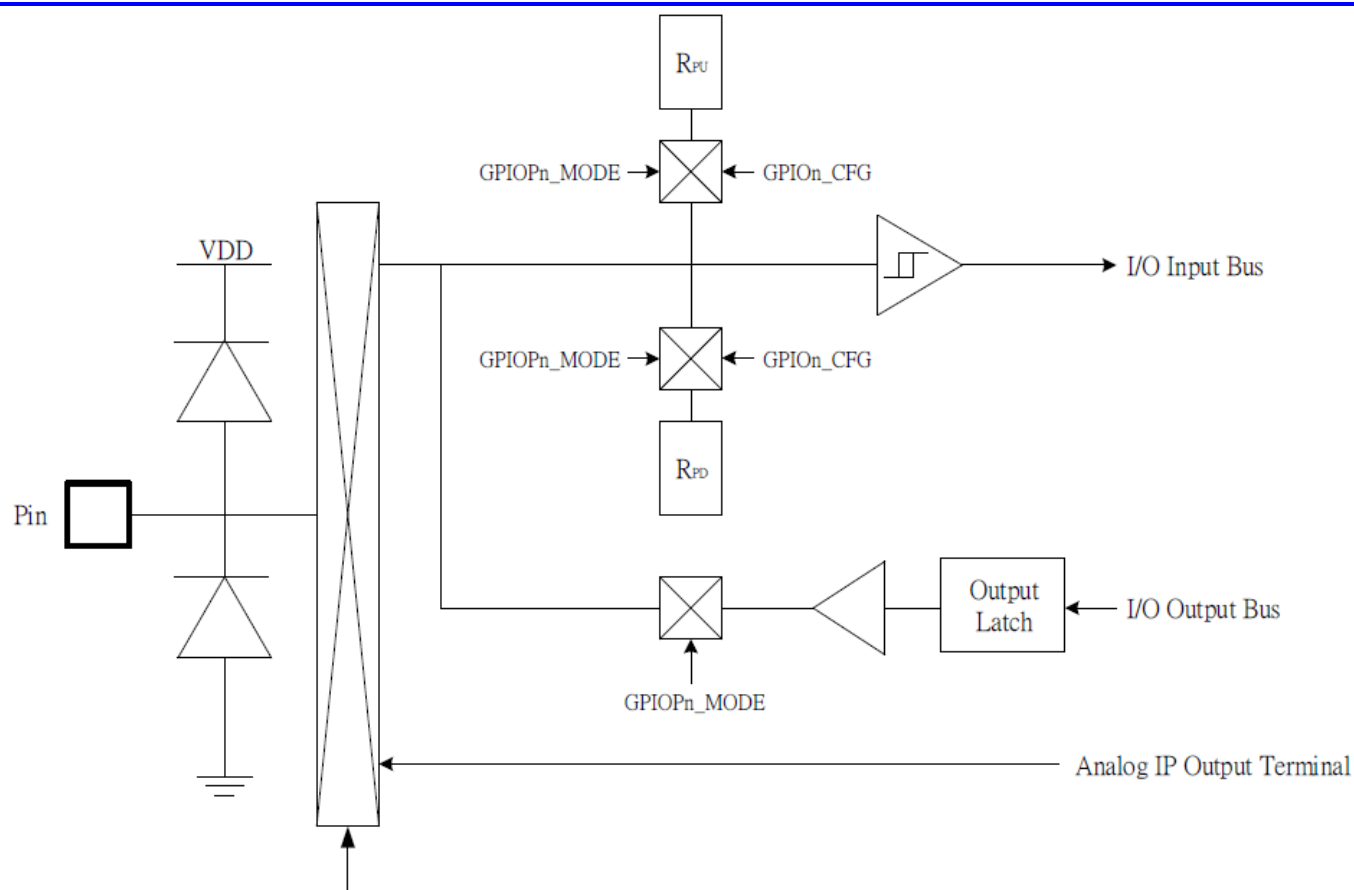
- **Bi-direction I/O Pin Shared with Specific Analog Input Function, e.g. XIN, ADC...**



\*. Specific Analog Function Control bit

\*. Some specific functions switch I/O direction directly, not through GPIOn\_MODE register.

- **Bi-direction I/O Pin Shared with Specific Analog Output Function, e.g. XOUT...**

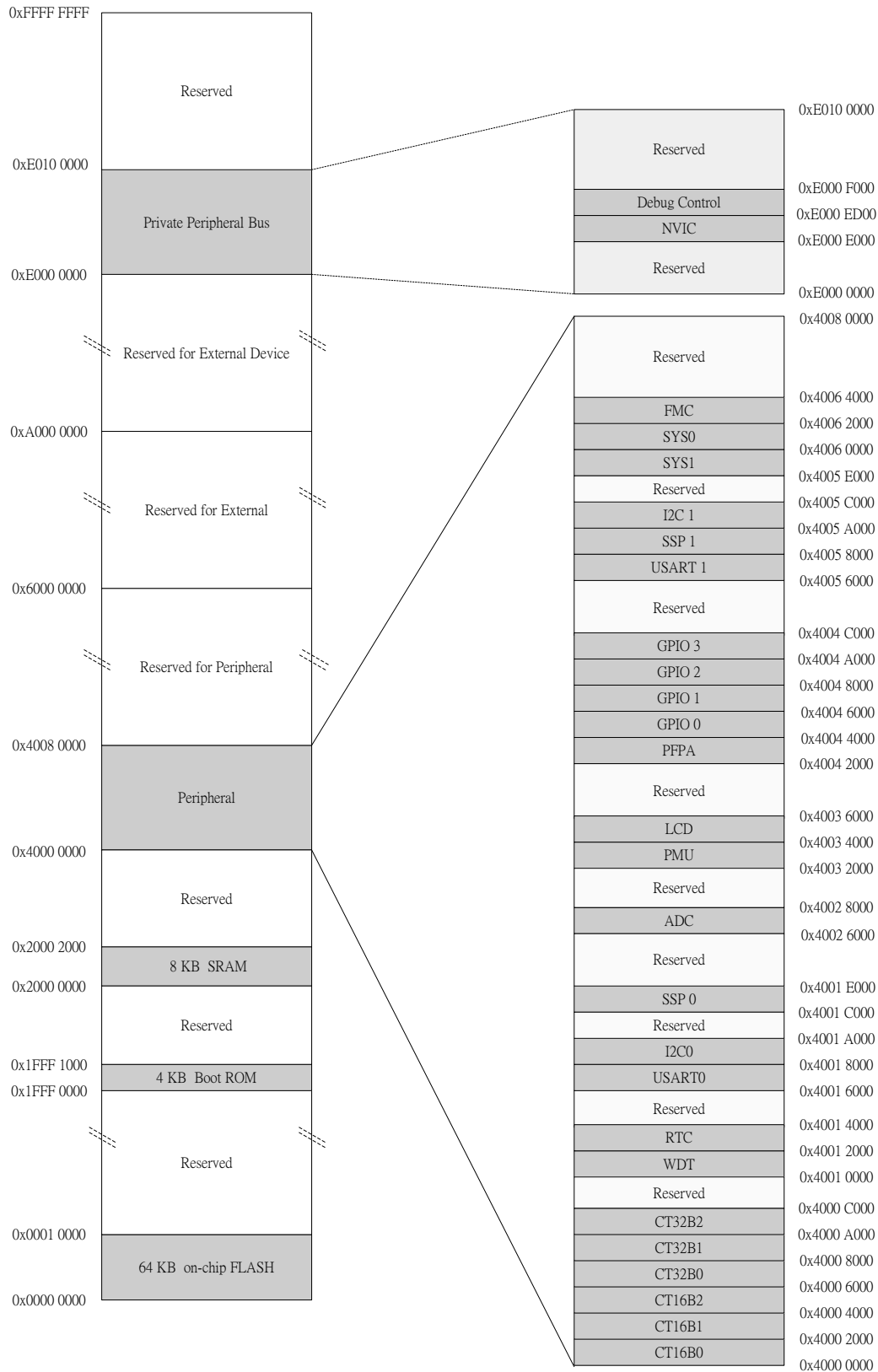


\*. Specific Analog Function Control bit

\*. Some specific functions switch I/O direction directly, not through `GPIOFn_MODE` register.

# 2 CENTRAL PROCESSOR UNIT (CPU)

## 2.1 MEMORY MAP



## 2.2 SYSTEM TICK TIMER

The SysTick timer is an integral part of the Cortex-M0. The SysTick timer is intended to generate a fixed 10-ms interrupt for use by an operating system or other system management software.

Since the SysTick timer is a part of the Cortex-M0, it facilitates porting of software by providing a standard timer that is available on Cortex-M0 based devices.

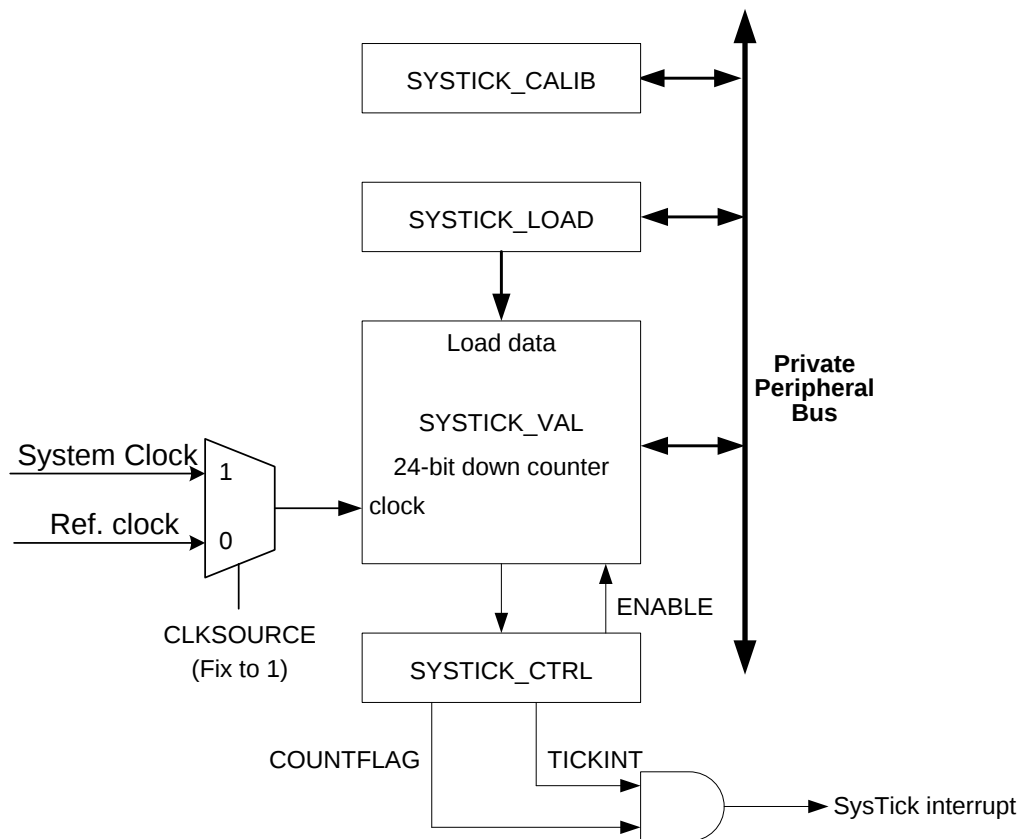
Refer to the *Cortex-M0 User Guide* for details.

### 2.2.1 OPERATION

The SysTick timer is a 24-bit timer that counts down to zero and generates an interrupt.

The intent is to provide a fixed 10-ms time interval between interrupts. The system tick timer is enabled through the SysTick control register. The system tick timer clock is fixed to the frequency of the system clock.

The block diagram of the SysTick timer:



When SysTick timer is enabled, the timer counts down from the current value (SYSTICK\_VAL) to zero, reloads to the value in the SysTick Reload Value Register (SYSTICK\_LOAD) on the next clock edge, then decrements on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set to 1. The COUNTFLAG bit clears on reads.

**\* Note:** When the processor is halted for debugging the counter does not decrease.

## 2.2.2 SYSTICK USAGE HINTS AND TIPS

The interrupt controller clock updates the SysTick counter. Some implementations stop this clock signal for low power mode. If this happens, the SysTick counter stops.

Ensure SW uses word accesses to access the SysTick registers.

The SysTick counter reload and current value are not initialized by HW. This means the correct initialization sequence for the SysTick counter is:

1. Program the reload value in SYSTICK\_LOAD register.
2. Clear the current value by writing any value to SYSTICK\_VAL register.
3. Program the Control and Status (SYSTICK\_CTRL) register.

## 2.2.3 SYSTICK REGISTERS

### 2.2.3.1 System Tick Timer Control and Status register (SYSTICK\_CTRL)

Address: 0xE000 E010 (Refer to Cortex-M0 Spec)

| Bit   | Name      | Description                                                                                                                                                                             | Attribute | Reset |
|-------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:17 | Reserved  |                                                                                                                                                                                         | R         | 0     |
| 16    | COUNTFLAG | This flag is set when the System Tick counter counts down to 0, and is cleared by reading this register.                                                                                | R/W       | 0     |
| 15:3  | Reserved  |                                                                                                                                                                                         | R         | 0     |
| 2     | CLKSOURCE | Selects the SysTick timer clock source.<br>0: reference clock.<br>1: system clock. (Fixed)                                                                                              | R         | 1     |
| 1     | TICKINT   | System Tick interrupt enable.<br>0: Disable the System Tick interrupt<br>1: Enable the System Tick interrupt, the interrupt is generated when the System Tick counter counts down to 0. | R/W       | 0     |
| 0     | ENABLE    | System Tick counter enable.<br>0: Disable<br>1: Enable                                                                                                                                  | R/W       | 0     |

### 2.2.3.2 System Tick Timer Reload value register (SYSTICK\_LOAD)

Address: 0xE000 E014 (Refer to Cortex-M0 Spec)

The RELOAD register is set to the value that will be loaded into the SysTick timer whenever it counts down to zero. This register is set by software as part of timer initialization. The SYSTICK\_CALIB register may be read and used as the value for RELOAD if the CPU or external clock is running at the frequency intended for use with the SYSTICK\_CALIB value.

The following example illustrates selecting the SysTick timer reload value to obtain a 10 ms time interval with the system clock set to 50 MHz.

The SysTick clock = system clock = 50 MHz

RELOAD = (system tick clock frequency × 10 ms) - 1 = (50 MHz × 10 ms) - 1  
= 0x0007A11F.

| Bit   | Name     | Description                                                                           | Attribute | Reset    |
|-------|----------|---------------------------------------------------------------------------------------|-----------|----------|
| 31:24 | Reserved |                                                                                       | R         | 0        |
| 23:0  | RELOAD   | Value to load into the SYSTICK_VAL when the counter is enabled and when it reaches 0. | R/W       | 0x5F7F9B |

**2.2.3.3 System Tick Timer Current Value register (SYSTICK\_VAL)**

Address: 0xE000 E018 (Refer to Cortex-M0 Spec)

| Bit   | Name     | Description                                                                                                                                                         | Attribute | Reset    |
|-------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|----------|
| 31:24 | Reserved |                                                                                                                                                                     | R         | 0        |
| 23:0  | CURRENT  | Reading this register returns the current value of the System Tick counter. Writing any value clears the System Tick counter and the COUNTFLAG bit in SYSTICK_CTRL. | R/W       | 0x7E7F35 |

**2.2.3.4 System Tick Timer Calibration Value register (SYSTICK\_CALIB)**

Address: 0xE000 E01C (Refer to Cortex-M0 Spec)

| Bit   | Name     | Description                                                                                                                                                                                                    | Attribute | Reset   |
|-------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|---------|
| 31    | NOREF    | Indicates the reference clock to M0 is provided or not.<br>1: No reference clock provided.                                                                                                                     | R         | 1       |
| 30    | SKEW     | Indicates whether the TENMS value is exact, an inexact TENMS value can affect the suitability of SysTick as a software real time clock.<br>0: TENMS value is exact<br>1: TENMS value is inexact, or not given. | R         | 0       |
| 29:24 | Reserved |                                                                                                                                                                                                                | R         | 0       |
| 23:0  | TENMS    | Reload value for 10ms timing, subject to system clock skew errors. If the value reads as zero, the calibration value is not known.                                                                             | R/W       | 0xA71FF |

## 2.3 NESTED VECTORED INTERRUPT CONTROLLER (NVIC)

All interrupts including the core exceptions are managed by the NVIC. NVIC has the following Features:

- The NVIC supports 32 vectored interrupts.
- 4 programmable interrupt priority levels with hardware priority level masking.
- Low-latency exception and interrupt handling.
- Efficient processing of late arriving interrupts.
- Implementation of System Control Registers
- Software interrupt generation.

### 2.3.1 INTERRUPT AND EXCEPTION VECTORS

| Execution No. | Priority | Function          | Description             | Address Offset |
|---------------|----------|-------------------|-------------------------|----------------|
| 0             | -        | -                 | Reserved                | 0x0000 0000    |
| 1             | -3       | Reset             | Reset                   | 0x0000 0004    |
| 2             | -2       | NMI_Handler       | Non maskable interrupt. | 0x0000 0008    |
| 3             | -1       | HardFault_Handler | All class of fault      | 0x0000 000C    |
| 4~10          | Reserved | Reserved          | Reserved                | -              |
| 11            | Settable | SVCCall           |                         | 0x0000 002C    |
| 12~13         | Reserved | Reserved          | Reserved                | -              |
| 14            | Settable | PendSV            |                         | 0x0000 0038    |
| 15            | Settable | SysTick           |                         | 0x0000 003C    |
| 16            | Settable | IRQ0/NDTIRQ       | NDT                     | 0x0000 0040    |
| 17            | Settable | IRQ1/             |                         | 0x0000 0044    |
| 18            | Settable | IRQ2/LCDIRQ       | LCD                     | 0x0000 0048    |
| 19            | Settable | IRQ3/I2SIRQ       | I2S                     | 0x0000 004C    |
| 20            | Settable | IRQ4/             |                         | 0x0000 0050    |
| 21            | Settable | IRQ5/             |                         | 0x0000 0054    |
| 22            | Settable | IRQ6/SSP0IRQ      | SSP0                    | 0x0000 0058    |
| 23            | Settable | IRQ7/SSP1IRQ      | SSP1                    | 0x0000 005C    |
| 24            | Settable | IRQ8/             |                         | 0x0000 0060    |
| 25            | Settable | IRQ9/             |                         | 0x0000 0064    |
| 26            | Settable | IRQ10/I2C0IRQ     | I2C0                    | 0x0000 0068    |
| 27            | Settable | IRQ11/I2C1IRQ     | I2C1                    | 0x0000 006C    |
| 28            | Settable | IRQ12/            |                         | 0x0000 0070    |
| 29            | Settable | IRQ13/USART0IRQ   | USART0                  | 0x0000 0074    |
| 30            | Settable | IRQ14/USART1IRQ   | USART1                  | 0x0000 0078    |

|    |          |                 |                                 |             |
|----|----------|-----------------|---------------------------------|-------------|
| 31 | Settable | IRQ15/CT16B0IRQ | CT16B0                          | 0x0000 007C |
| 32 | Settable | IRQ16/CT16B1IRQ | CT16B1                          | 0x0000 0080 |
| 33 | Settable | IRQ17/CT16B2IRQ | CT16B2                          | 0x0000 0084 |
| 34 | Settable | IRQ18/          |                                 | 0x0000 0088 |
| 35 | Settable | IRQ19/CT32B0IRQ | CT32B0                          | 0x0000 008C |
| 36 | Settable | IRQ20/CT32B1IRQ | CT32B1                          | 0x0000 0090 |
| 37 | Settable | IRQ21/CT32B2IRQ | CT32B2                          | 0x0000 0094 |
| 38 | Settable | IRQ22/          |                                 | 0x0000 0098 |
| 39 | Settable | IRQ23/RTCIRQ    | RTC                             | 0x0000 009C |
| 40 | Settable | IRQ24/ADCIRQ    | ADC                             | 0x0000 00A0 |
| 41 | Settable | IRQ25/WDTIRQ    | WDT                             | 0x0000 00A4 |
| 42 | Settable | IRQ26/LVDIRQ    | LVD                             | 0x0000 00A8 |
| 43 | Settable | IRQ27/          |                                 | 0x0000 00AC |
| 44 | Settable | IRQ28/P3IRQ     | GPIO interrupt status of port 3 | 0x0000 00B0 |
| 45 | Settable | IRQ29/P2IRQ     | GPIO interrupt status of port 2 | 0x0000 00B4 |
| 46 | Settable | IRQ30/P1IRQ     | GPIO interrupt status of port 1 | 0x0000 00B8 |
| 47 | Settable | IRQ31/P0IRQ     | GPIO interrupt status of port 0 | 0x0000 00BC |

## 2.3.2 NVIC REGISTERS

### 2.3.2.1 IRQ0~31 Interrupt Set-Enable Register (NVIC\_ISER)

Address: 0xE000 E100 (Refer to Cortex-M0 Spec.)

The ISER enables interrupts, and shows the interrupts that are enabled.

| Bit  | Name         | Description                                                                                                                         | Attribute | Reset |
|------|--------------|-------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:0 | SETENA[31:0] | Interrupt set-enable bits.<br>Write → 0: No effect<br>1: Enable interrupt.<br>Read → 0: Interrupt disabled<br>1: Interrupt enabled. | R/W       | 0     |

### 2.3.2.2 IRQ0~31 Interrupt Clear-Enable Register (NVIC\_ICER)

Address: 0xE000 E180 (Refer to Cortex-M0 Spec.)

The ICER disables interrupts, and shows the interrupts that are enabled.

| Bit  | Name         | Description                                                                                                                          | Attribute | Reset |
|------|--------------|--------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:0 | CLRENA[31:0] | Interrupt clear-enable bits.<br>Write→ 0: No effect<br>1: Disable interrupt.<br>Read→ 0: Interrupt disabled<br>1: Interrupt enabled. | R/W       | 0     |

### 2.3.2.3 IRQ0~31 Interrupt Set-Pending Register (NVIC\_ISPR)

Address: 0xE000 E200 (Refer to Cortex-M0 Spec.)

The ISPR forces interrupts into the pending state, and shows the interrupts that are pending.

**\* Note: Writing 1 to the ISPR bit corresponding to**  
**1. an interrupt that is pending has no effect**  
**2. a disabled interrupt sets the state of that interrupt to pending.**

| Bit  | Name          | Description                                                                                                                                                | Attribute | Reset |
|------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:0 | SETPEND[31:0] | Interrupt set-pending bits.<br>Write→ 0: No effect<br>1: Change interrupt state to pending<br>Read→ 0: Interrupt is not pending<br>1: Interrupt is pending | R/W       | 0     |

### 2.3.2.4 IRQ0~31 Interrupt Clear-Pending Register (NVIC\_ICPR)

Address: 0xE000 E280 (Refer to Cortex-M0 Spec.)

The ICPR removes the pending state from interrupts, and shows the interrupts that are pending.

**\* Note: Writing 1 to an ICPR bit does not affect the active state of the corresponding interrupt.**

| Bit  | Name          | Description                                                                                                                                                      | Attribute | Reset |
|------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:0 | CLRPEND[31:0] | Interrupt clear-pending bits.<br>Write→ 0: No effect<br>1: Removes pending state of an interrupt<br>Read→ 0: Interrupt is not pending<br>1: Interrupt is pending | R/W       | 0     |

### 2.3.2.5 IRQ0~31 Interrupt Priority Register (NVIC\_IPRn) (n=0~7)

Address: 0xE000 E400 + 0x4 \* n (Refer to Cortex-M0 Spec.)

The interrupt priority registers provide an 8-bit priority field for each interrupt, and each register holds four priority fields. This means the number of registers is implementation-defined, and corresponds to the number of implemented interrupts.

| Bit   | Name        | Description                                                                                                                                                                                                                                                                                                           | Attribute | Reset |
|-------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:24 | PRI_(4*n+3) | Each priority field holds a priority value, 0-192. The lower the value, the greater the priority of the corresponding interrupt. The processor implements only bits[31:30] of each field, bits [29:24] read as zero and ignore writes. This means writing 255 to a priority register saves value 192 to the register. | R/W       | 0     |
| 23:16 | PRI_(4*n+2) | Each priority field holds a priority value, 0-192. The lower the value, the greater the priority of the corresponding interrupt. The processor implements only bits[23:22] of each field, bits [21:16] read as zero and ignore writes. This                                                                           | R/W       | 0     |

|      |             |                                                                                                                                                                                                                                                                                                                      |     |   |
|------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---|
|      |             | means writing 255 to a priority register saves value 192 to the register.                                                                                                                                                                                                                                            |     |   |
| 15:8 | PRI_(4*n+1) | Each priority field holds a priority value, 0-192. The lower the value, the greater the priority of the corresponding interrupt. The processor implements only bits[15:14] of each field, bits [13:8] read as zero and ignore writes. This means writing 255 to a priority register saves value 192 to the register. | R/W | 0 |
| 7:0  | PRI_4*n     | Each priority field holds a priority value, 0-192. The lower the value, the greater the priority of the corresponding interrupt. The processor implements only bits[7:6] of each field, bits [5:0] read as zero and ignore writes. This means writing 255 to a priority register saves value 192 to the register.    | R/W | 0 |

## 2.4 APPLICATION INTERRUPT AND RESET CONTROL (AIRC)

Address: 0xE000 ED0C (Refer to Cortex-M0 Spec)

The entire MCU, including the core, can be reset by SW by setting the SYSRESREQ bit in the AIRC register in Cortex-M0 spec.

**\* Note: To write to this register, user must write 0x05FA to the VECTKEY field at the same time, otherwise the processor ignores the write.**

| Bit   | Name          | Description                                                                                                                                 | Attribute | Reset |
|-------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:16 | VECTKEY       | Register key.<br>Read as unknown. Write 0x05FA to VECTKEY, otherwise the write is ignored.                                                  | R/W       | 0     |
| 15    | ENDIANESS     | Data endianness implemented<br>0: Little-endian<br>1: Big-endian                                                                            | R         | 0     |
| 14:3  | Reserved      |                                                                                                                                             | R         | 0     |
| 2     | SYSRESETREQ   | System reset request. This bit read as 0.<br>0: No effect<br>1: Requests a system level reset.                                              | W         | 0     |
| 1     | VECTCLRACTIVE | Reserved for debug use. This bit read as 0. When writing to the register you must write 0 to this bit, otherwise behavior is Unpredictable. | W         | 0     |
| 0     | Reserved      |                                                                                                                                             | R         | 0     |

## 2.5 CODE OPTION TABLE

Address: 0x1FFF 2000

| Bit   | Name                | Description                                                               | Attribute | Reset  |
|-------|---------------------|---------------------------------------------------------------------------|-----------|--------|
| 31:16 | Code Security[15:0] | Code Security<br>0xFFFF: CS0<br>0x5A5A: CS1<br>0xA5A5: CS2<br>0x55AA: CS3 | R/W       | 0xFFFF |
| 15:0  | Reserved            |                                                                           | R         | All 1  |

## 2.6 UNIQUE NUMBER

The unique number is a 8-byte unique device serial number of each IC. In other words, the unique number is different and discontinuous for each IC. Users can use the unique number to pair in RF application, or use as USB string serial number.

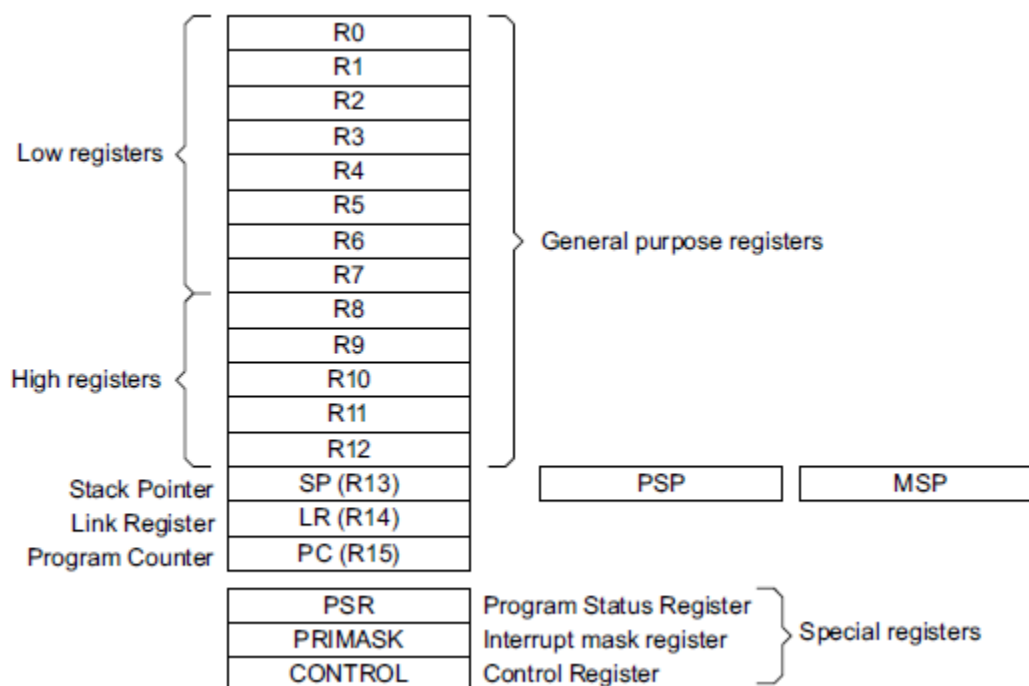
Address: 0x1FFF 2C08

| Bit  | Name         | Description                    | Attribute | Reset  |
|------|--------------|--------------------------------|-----------|--------|
| 31:0 | L4BYTE[31:0] | Lower 4 bytes of Unique number | R         | By Die |

Address: 0x1FFF 2C0C

| Bit  | Name         | Description                   | Attribute | Reset  |
|------|--------------|-------------------------------|-----------|--------|
| 31:0 | H4BYTE[31:0] | High 4 bytes of Unique number | R         | By Die |

## 2.7 CORE REGISTER OVERVIEW



| Register | Description (Refer to Cortex-M0 Spec)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R0~R12   | General-purpose registers for data operations.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| SP (R13) | The Stack Pointer (SP). In Thread mode, the CONTROL register indicates the stack pointer to use, Main Stack Pointer (MSP) or Process Stack Pointer (PSP)<br>On reset, the processor loads the MSP with the value from address 0x00000000.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| LR (R14) | The Link Register (LR). It stores the return information for subroutines, function calls, and exceptions.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| PC (R15) | The Program Counter (PC). It contains the current program address.<br>On reset, the processor loads the PC with the value of the reset vector, at address 0x00000004.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| PSR      | <p>The Program Status Register (PSR) combines:</p> <ul style="list-style-type: none"> <li>• Application Program Status Register (APSR)</li> <li>• Interrupt Program Status Register (IPSR)</li> <li>• Execution Program Status Register (EPSR).</li> </ul> <p>These registers are mutually exclusive bit fields in the 32-bit PSR.</p> <p>The diagram illustrates the 32-bit structure of the Program Status Register (PSR). It is divided into three main sections: APSR (Application Program Status Register), IPSR (Interrupt Program Status Register), and EPSR (Execution Program Status Register). APSR covers bits 31 down to 27, containing flags N, Z, C, and V, followed by 23 reserved bits. IPSR covers bits 26 down to 5, containing 21 reserved bits and an 8-bit exception number. EPSR covers bits 4 down to 0, containing 3 reserved bits, a single bit T, and 28 reserved bits.</p> |
| PRIMASK  | The PRIMASK register prevents activation of all exceptions with configurable priority.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| CONTROL  | The CONTROL register controls the stack used when the processor is in Thread mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

# 3 SYSTEM CONTROL

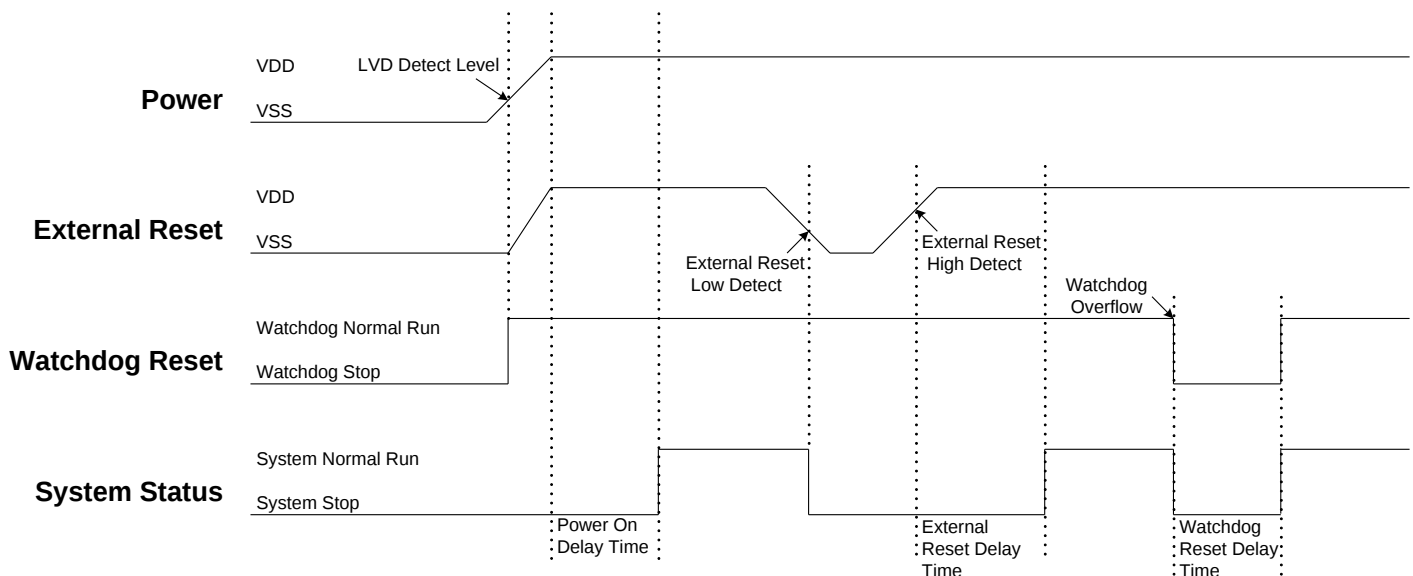
## 3.1 RESET

A system reset is generated when one of the following events occurs:

1. A low level on the RST pin (external reset).
2. Power-on reset (POR reset)
3. LVD reset
4. Watchdog Timer reset (WDT reset)
5. Software reset (SW reset)

The reset source can be identified by checking the reset flags in [System Reset Status register \(SYS0\\_RSTST\)](#). These sources act on the RST pin and it is always kept low during the delay phase. The RESET service routine vector is fixed at address 0x00000004 in the memory map. For more details, refer to [Interrupt and Exception Vectors](#).

Finishing any reset sequence needs some time. The system provides complete procedures to make the power on reset successful. For different oscillator types, the reset time is different. That causes the VDD rise rate and start-up time of different oscillator is not fixed. RC type oscillator's start-up time is very short, but the crystal type is longer. Under client terminal application, users have to take care of the power on reset time for the master terminal requirement. The reset timing diagram is as following.



### 3.1.1 POWER-ON RESET (POR)

The power on reset depends on LVD operation for most power-up situations. The power supplying to system is a rising curve and needs some time to achieve the normal voltage. Power on reset sequence is as following:

- **Power-up:** System detects the power voltage up and waits for power stable.
- **External reset (only external reset pin enable):** System checks external reset pin status. If external reset pin is not high level, the system keeps reset status and waits external reset pin released.
- **System initialization:** All system registers is set as initial conditions and system is ready.
- **Oscillator warm up:** Oscillator operation is successfully and supply to system clock.
- **Program executing:** Power on sequence is finished and program executes from Boot loader.

### 3.1.2 WATCHDOG RESET (WDT RESET)

Watchdog reset is a system protection. In normal condition, system works well and clears watchdog timer by program. Under error condition, system is in unknown situation and watchdog can't be clear by program before watchdog timer overflow. Watchdog timer overflow occurs and the system is reset. After watchdog reset, the system restarts and returns normal mode. Watchdog reset sequence is as following.

- **Watchdog timer status:** System checks watchdog timer overflow status. If watchdog timer overflow occurs, the system is reset.
- **System initialization:** All system registers is set as initial conditions and system is ready.
- **Oscillator warm up:** Oscillator operation is successfully and supply to system clock.
- **Program executing:** Power on sequence is finished and program executes from 0x0.

Watchdog timer application note is as following.

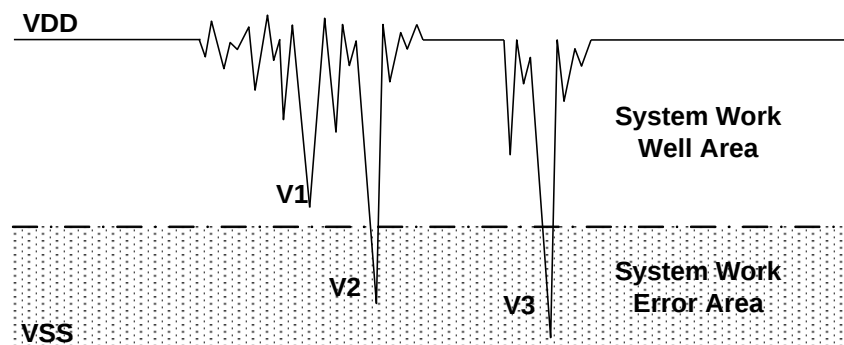
- Before clearing watchdog timer, check I/O status and check RAM contents can improve system error.
- Don't clear watchdog timer in interrupt vector and interrupt service routine. That can improve main routine fail.
- Clearing watchdog timer program is only at one part of the program. This way is the best structure to enhance the watchdog timer function.

\* **Note:** Please refer to the "WATCHDOG TIMER" about watchdog timer detail information.

### 3.1.3 BROWN-OUT RESET

#### 3.1.3.1 BROWN OUT DESCRIPTION

The brown-out reset is a power dropping condition. The power drops from normal voltage to low voltage by external factors (e.g. EFT interference or external loading changed). The brown out reset would make the system not work well or executing program error.



Brown-Out Reset Diagram

The power dropping might through the voltage range that's the system dead-band. The dead-band means the power range can't offer the system minimum operation power requirement. The above diagram is a typical brown out reset diagram. There is a serious noise under the VDD, and VDD voltage drops very deep. There is a dotted line to separate the system working area. The above area is the system work well area. The below area is the system work error area called dead-band. V1 doesn't touch the below area and not affect the system operation. But the V2 and V3 is under the below area and may induce the system error occurrence. Let system under dead-band includes some conditions.

#### DC application:

The power source of DC application is usually using battery. When low battery condition and MCU drive any loading, the

power drops and keeps in dead-band. Under the situation, the power won't drop deeper and not touch the system reset voltage. That makes the system under dead-band.

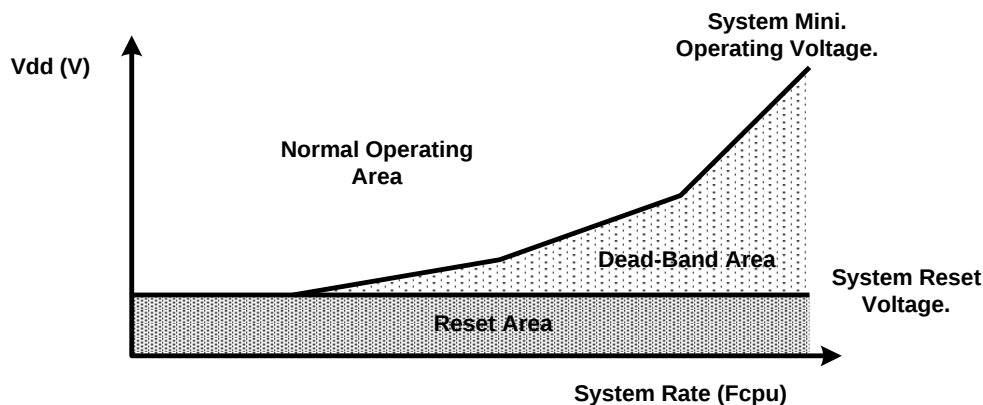
#### AC application:

In AC power application, the DC power is regulated from AC power source. This kind of power usually couples with AC noise that makes the DC power dirty. Or the external loading is very heavy, e.g. driving motor. The loading operating induces noise and overlaps with the DC power. VDD drops by the noise, and the system works under unstable power situation.

The power on duration and power down duration are longer in AC application. The system power on sequence protects the power on successful, but the power down situation is like DC low battery condition. When turn off the AC power, the VDD drops slowly and through the dead-band for a while.

### 3.1.3.2 THE SYSTEM OPERATING VOLTAGE DECSRIPTION

To improve the brown out reset needs to know the system minimum operating voltage which is depend on the system executing rate and power level. Different system executing rates have different system minimum operating voltage. The electrical characteristic section shows the system voltage to executing rate relationship.



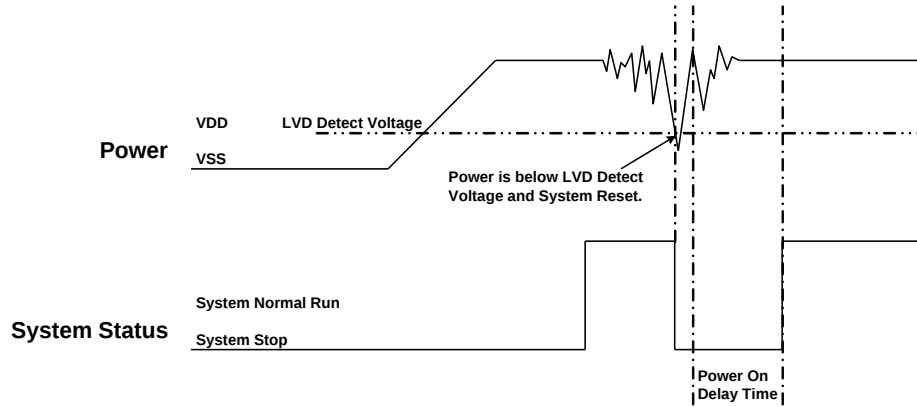
Normally the system operation voltage area is higher than the system reset voltage to VDD, and the reset voltage is decided by LVD detect level. The system minimum operating voltage rises when the system executing rate upper even higher than system reset voltage. The dead-band definition is the system minimum operating voltage above the system reset voltage.

### 3.1.3.3 BROWN-OUT RESET IMPROVEMENT

**How to improve the brown reset condition?** There are some methods to improve brown out reset as following.

- LVD reset
- Watchdog reset
- Reduce the system executing rate
- External reset circuit. (Zener diode reset circuit, Voltage bias reset circuit, External reset IC)

**\* Note:** The “Zener diode reset circuit”, “Voltage bias reset circuit” and “External reset IC” can completely improve the brown out reset, DC low battery and AC slow power down conditions.

**LVD reset:**

The LVD (low voltage detector) is built-in SONiX 32-bit MCU to be brown out reset protection. When the VDD drops and is below LVD detect voltage, the LVD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, SW can monitor the signal by reading a dedicated status register. An additional threshold level can be selected to cause a forced reset of the chip. The LVD detect level is different by each MCU. The LVD voltage level is a point of voltage and not easy to cover all dead-band range. Using LVD to improve brown out reset is dependent on application requirement and environment. If the power variation is very deep, violent and trigger the LVD, the LVD can be the protection. If the power variation can touch the LVD detect level and make system work error, the LVD can't be the protection and need to other reset methods. More detail LVD information is in the electrical characteristic section.

**Watchdog reset:**

The watchdog timer is a protection to make sure the system executes well. Normally the watchdog timer would be clear at one point of program. Don't clear the watchdog timer in several addresses. The system executes normally and the watchdog won't reset system. When the system is under dead-band and the execution error, the watchdog timer can't be clear by program. The watchdog is continuously counting until overflow occurrence. The overflow signal of watchdog timer triggers the system to reset and return to normal mode after reset sequence. This method also can improve brown out reset condition and make sure the system to return normal mode.

If the system reset by watchdog and the power is still in dead-band, the system reset sequence won't be successful and the system stays in reset status until the power return to normal range.

**Reduce the system executing rate:**

If the system rate is fast and the dead-band exists, to reduce the system executing rate can improve the dead-band. The lower system rate is with lower minimum operating voltage. Select the power voltage that's no dead-band issue and find out the mapping system rate. Adjust the system rate to the value and the system exits the dead-band issue. This way needs to modify whole program timing to fit the application requirement.

**External reset circuit:**

The external reset methods also can improve brown out reset and is the complete solution. There are three external reset circuits to improve brown out reset including "Zener diode reset circuit", "Voltage bias reset circuit" and "External reset IC". These three reset structures use external reset signal and control to make sure the MCU be reset under power dropping and under dead-band. The external reset information is described in the next section.

### 3.1.4 EXTERNAL RESET

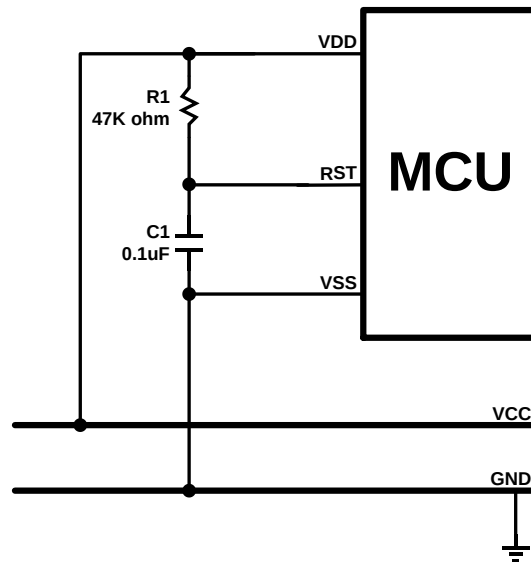
External reset function is controlled by [External RESET pin control \(SYS0\\_EXRSTCTRL\)](#) register. Default value is 1, which means external reset function is disabled. External reset pin is Schmitt Trigger structure and low level active. The system is running when reset pin is high level voltage input. The reset pin receives the low voltage and the system is reset. The external reset operation activates in power on and normal running mode. During system power-up, the external reset pin must be high level input, or the system keeps in reset status. External reset sequence is as following.

- **External reset (only external reset pin enable):** System checks external reset pin status. If external reset pin is not high level, the system keeps reset status and waits external reset pin released.
- **System initialization:** All system registers is set as initial conditions and system is ready.

- **Oscillator warm up:** Oscillator operation is successfully and supply to system clock.
- **Program executing:** Power on sequence is finished and program executes from Boot loader.

The external reset can reset the system during power on duration, and good external reset circuit can protect the system to avoid working at unusual power condition, e.g. brown out reset in AC power application.

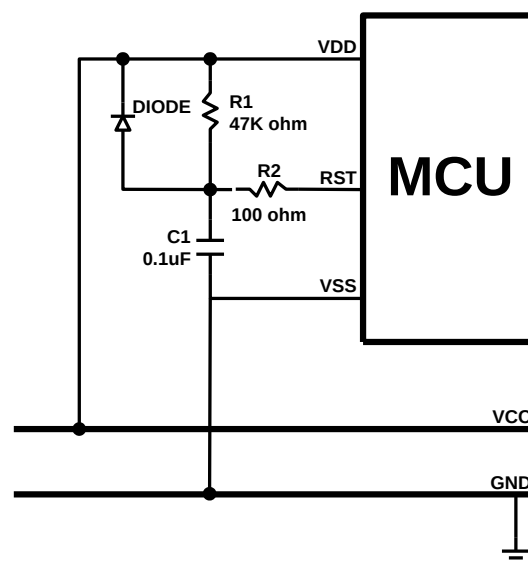
#### 3.1.4.1 SIMPLY RC RESET CIRCUIT



This is the basic reset circuit, and only includes R1 and C1. The RC circuit operation makes a slow rising signal into reset pin as power up. The reset signal is slower than VDD power up timing, and system occurs a power on signal from the timing difference.

\* **Note:** The reset circuit is no any protection against unusual power or brown out reset.

#### 3.1.4.2 DIODE & RC RESET CIRCUIT

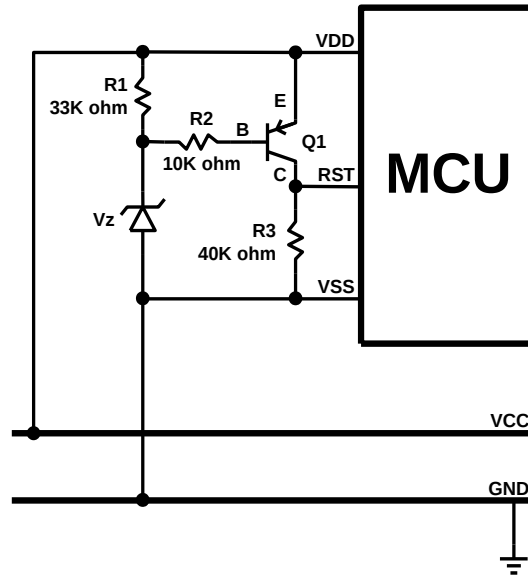


This is the better reset circuit. The R1 and C1 circuit operation is like the simply reset circuit to make a power on signal. The reset circuit has a simply protection against unusual power. The diode offers a power positive path to conduct

higher power to VDD. It is can make reset pin voltage level to synchronize with VDD voltage. The structure can improve slight brown out reset condition.

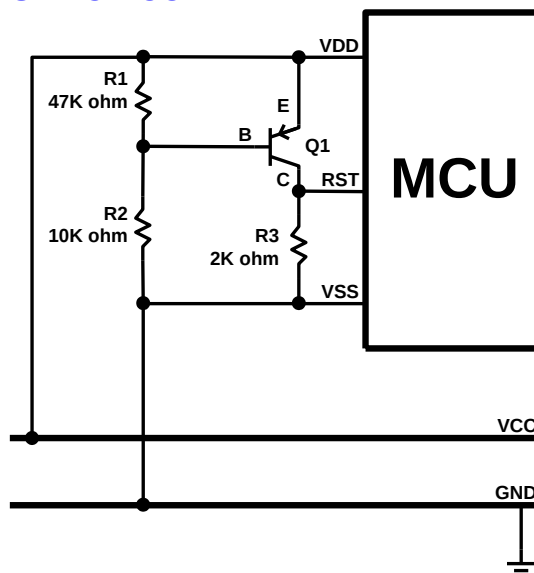
\* **Note:** The R2 100 ohm resistor of “Simply reset circuit” and “Diode & RC reset circuit” is necessary to limit any current flowing into reset pin from external capacitor C in the event of reset pin breakdown due to Electrostatic Discharge (ESD) or Electrical Over-stress (EOS).

### 3.1.4.3 ZENER DIODE RESET CIRCUIT



The Zener diode reset circuit is a simple low voltage detector and can **improve brown out reset condition completely**. Use Zener voltage to be the active level. When VDD voltage level is above “ $V_z + 0.7V$ ”, the C terminal of the PNP transistor outputs high voltage and MCU operates normally. When VDD is below “ $V_z + 0.7V$ ”, the C terminal of the PNP transistor outputs low voltage and MCU is in reset mode. Decide the reset detect voltage by Zener specification. Select the right Zener voltage to conform the application.

### 3.1.4.4 VOLTAGE BIAS RESET CIRCUIT



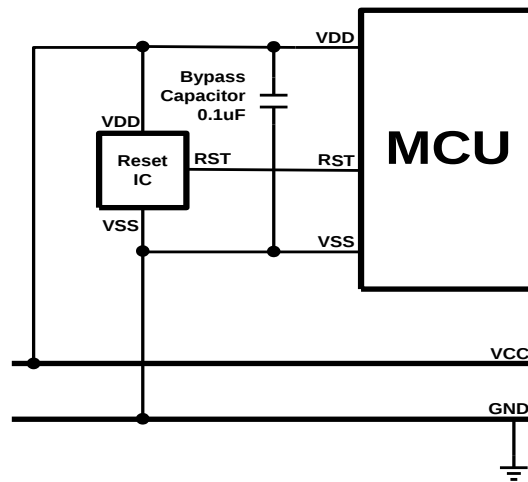
The voltage bias reset circuit is a low cost voltage detector and can **improve brown out reset condition completely**. The operating voltage is not accurate as Zener diode reset circuit. Use R1, R2 bias voltage to be the active level. When

VDD voltage level is above or equal to  $0.7V \times (R1 + R2) / R1$ , the C terminal of the PNP transistor outputs high voltage and MCU operates normally. When VDD is below  $0.7V \times (R1 + R2) / R1$ , the C terminal of the PNP transistor outputs low voltage and MCU is in reset mode.

Decide the reset detect voltage by R1, R2 resistances. Select the right R1, R2 value to conform the application. In the circuit diagram condition, the MCU's reset pin level varies with VDD voltage variation, and the differential voltage is 0.7V. If the VDD drops and the voltage lower than reset pin detect level, the system would be reset. If want to make the reset active earlier, set the  $R2 > R1$  and the cap between VDD and C terminal voltage is larger than 0.7V. The external reset circuit is with a stable current through R1 and R2. For power consumption issue application, e.g. DC power system, the current must be considered to whole system power consumption.

**\* Note:** Under unstable power condition as brown out reset, “Zener diode reset circuit” and “Voltage bias reset circuit” can protect system no any error occurrence as power dropping. When power drops below the reset detect voltage, the system reset would be triggered, and then system executes reset sequence. That makes sure the system work well under unstable power situation.

### 3.1.4.5 EXTERNAL RESET IC



The external reset circuit also uses external reset IC to enhance MCU reset performance. This is a high cost and good effect solution. By different application and system requirement to select suitable reset IC. The reset circuit can improve all power variation.

### 3.1.5 SOFTWARE RESET

The entire MCU, including the core, can be reset by software by setting the SYSRESREQ bit in the [AIRC \(Application Interrupt and Reset Control\)](#) register in Cortex-M0 spec.

The software-initiated system reset sequence is as follows:

1. A software reset is initiated by setting the SYSRESREQ bit.
2. An internal reset is asserted.
3. The internal reset is deasserted and the MCU loads from memory the initial stack pointer, the initial program counter, and the first instruction designated by the program counter, and then begins execution.

## 3.2 SYSTEM CLOCK

Different clock sources can be used to drive the system clock (SYSCLK):

- 12 MHz internal high speed RC (IHRC)
- 32 KHz internal low speed RC (ILRC)
- PLL clock
- High speed external (EHS) crystal clock
- Low speed external (ELS) 32.768 KHz crystal

Each clock source can be switched on or off independently when it is not used, to optimize power consumption.

The micro-controller is a dual clock system. There are high-speed clock and low-speed clock. The high-speed clock is generated from the external oscillator & on-chip PLL circuit. The low-speed clock is generated from on-chip low-speed RC oscillator circuit (ILRC 16 KHz).

### 3.2.1 INTERNAL RC CLOCK SOURCE

#### 3.2.1.1 Internal High-speed RC Oscillator (IHRC)

The internal high-speed oscillator is 12MHz RC type. The accuracy is  $\pm 2\%$  under commercial condition. The IHRC can be switched on and off using the IHRCE bit in [Analog Block Control register \(SYS0\\_ANBCTRL\)](#).

#### 3.2.1.2 Internal Low-speed RC Oscillator (ILRC)

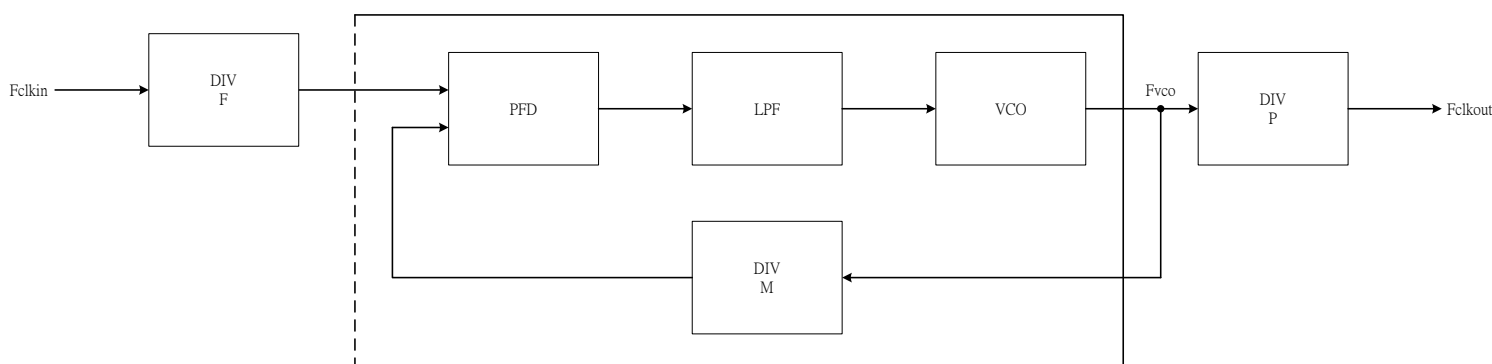
The system low clock source is the internal low-speed oscillator built in the micro-controller. The low-speed oscillator uses RC type oscillator circuit. The frequency is affected by the voltage and temperature of the system. In common condition, the frequency of the RC oscillator is about 32 KHz.

**\* Note:** The ILRC can ONLY be switched on and off by HW.

### 3.2.2 PLL

SONiX 32-bit MCU uses the PLL to create the clocks for the core and peripherals. The input frequency range is 10MHz to 25MHz. The input clock is divided down and fed to the Phase-Frequency Detector (PFD). This block compares the phase and frequency of its inputs, and generates a control signal when phase and/ or frequency do not match. The loop filter filters these control signals and drives the voltage controlled oscillator (VCO), which generates the main clock and optionally two additional phases. The VCO frequency range is 156MHz to 320MHz. These clocks are divided by P by the programmable post divider to create the output clock(s). The VCO output clock is then divided by M by the programmable feedback divider to generate the feedback clock. The output signal of the phase-frequency detector is also monitored by the lock detector, to signal when the PLL has locked on to the input clock.

The PLL settling time is 100  $\mu$ s.



#### 3.2.2.1 PLL Frequency selection

The PLL frequency equations:

$$F_{VCO} = F_{CLKIN} / F * M$$

$$F_{CLKOUT} = F_{VCO} / P$$

The PLL frequency is determined by the following parameters:

- $F_{CLKIN}$ : Frequency from the PLLCLKSEL multiplexer.
- $F_{VCO}$ : Frequency of the Voltage Controlled Oscillator (VCO); 156 to 320 MHz.
- $F_{CLKOUT}$ : Frequency of PLL output.
- P: System PLL post divider ratio, controlled by PSEL bits in [PLL control register \(SYS0\\_PLLCTRL\)](#).
- F: System PLL front divider ratio, controlled by FSEL bits in [PLL control register \(SYS0\\_PLLCTRL\)](#).
- M: System PLL feedback divider ratio, controlled by MSEL bits in [PLL control register \(SYS0\\_PLLCTRL\)](#).

To select the appropriate values for M, P, and F, it is recommended to follow these constraints:

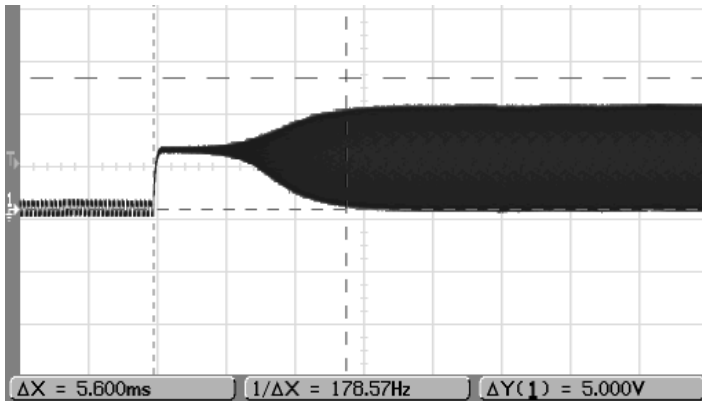
1.  $10\text{MHz} \leq F_{CLKIN} \leq 25\text{MHz}$
2.  $150\text{MHz} \leq F_{VCO} \leq 330\text{MHz}$
3.  $2 < M \leq 31$
4.  $F = 1$ , or  $2$
5.  $P = 6, 8, 10, 12$ , or  $14$  (duty 50% +/- 2.5%)
6.  $F_{CLKOUT} = 20\text{MHz}, 30\text{MHz}, 40\text{MHz}, 50\text{MHz}, 24\text{MHz}, 36\text{MHz}, 48\text{MHz}, 32\text{MHz}, 22\text{MHz}, 24\text{MHz}, 50\text{MHz}$   
with jitter  $< \pm 500$  ps

### 3.2.3 EXTERNAL CLOCK SOURCE

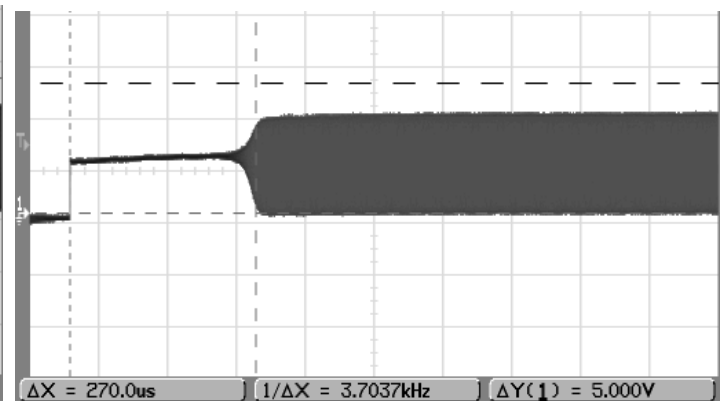
#### 3.2.3.1 External High-speed (EHS) Clock

External high clock includes Crystal/Ceramic modules. The startup time of Crystal is longer. The oscillator start-up time decides reset time length.

4MHz Crystal

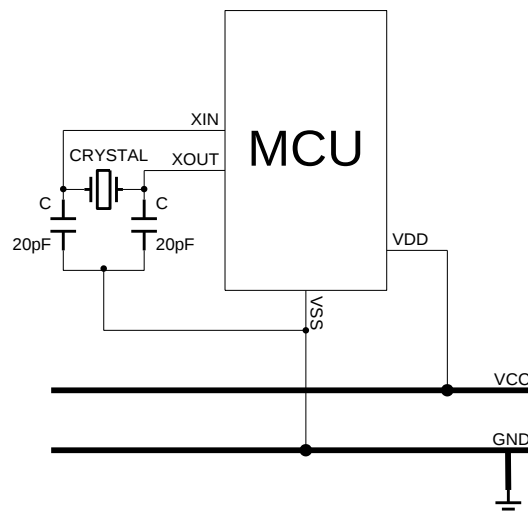


4MHz Ceramic



#### 3.2.3.2 CRYSTAL/CERAMIC

Crystal/Ceramic devices are driven by XIN, XOUT pins. For high/normal/low frequency, the driving currents are different.



\* **Note:** Connect the Crystal/Ceramic and C as near as possible to the XIN/XOUT/VSS pins of MCU.

- **Structure:** 10MHz~25MHz EHS external crystal/ceramic resonator
- **Main Purpose:** System high clock source, RTC clock source, and PLL clock source.
- **Warm-up Time:** 2048\*F<sub>EHS</sub>
- **XIN/XOUT Shared Pin Selection:**

| Oscillator Mode | XIN pin         | XOUT pin        |
|-----------------|-----------------|-----------------|
| IHRC            | GPIO            | GPIO            |
| EHS X'TAL       | Crystal/Ceramic | Crystal/Ceramic |

The resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

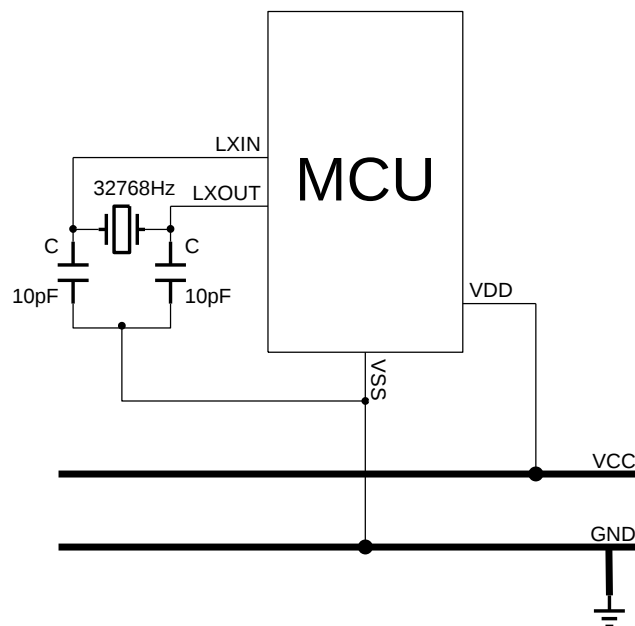
The EHS crystal is switched on and off using the EHSEN bit in [Analog Block Control register \(SYS0\\_ANBCTRL\)](#).

### 3.2.3.3 External Low-speed (ELS) Clock

The low-speed oscillator can use 32768 crystal oscillator circuit.

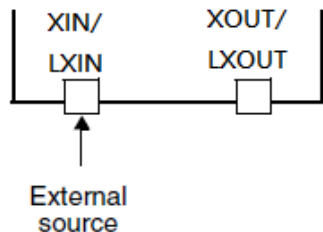
### 3.2.3.4 CRYSTAL

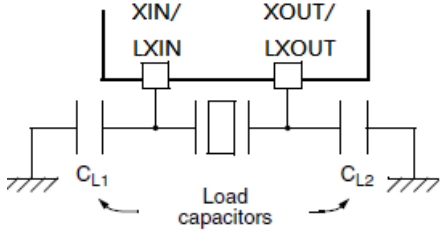
Crystal devices are driven by LXIN, LXOUT pins. The 32768 crystal and 10pF capacitor must be as near as possible to MCU. The ELS crystal is switched on and off using the ELSSEN bit in [Analog Block Control register \(SYS0\\_ANBCTRL\)](#).



\* **Note:** Connect the Crystal/Ceramic and C as near as possible to the LXIN/LXOUT/VSS pins of MCU. The capacitor between LXIN/LXOUT and VSS must be 10pF.

### 3.2.3.5 Bypass Mode

| Clock Source                      | H/W Configuration                                                                   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----------------------------------|-------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| External clock source<br>(Bypass) |  | <p>In Bypass mode, the external clock signal (square, sinus or triangle) with ~50% duty cycle must be provided to drive the XIN/LXIN pin while the XOUT/LXOUT pin should be the inverse of the input clock signal.</p> <p>EHS X'tal can have a frequency of up to 25 MHz. Select this mode by setting EHSEN bit in <a href="#">Analog Block Control register (SYS0_ANBCTRL)</a>.</p> <p>ELS X'TAL must have a frequency of 32.768 KHz.</p> |

|                                   |                                                                                   |                                                                                                                                                               |
|-----------------------------------|-----------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                   |                                                                                   | You select this mode by setting ELSEN bit in <a href="#">Analog Block Control register (SYS0_ANBCTRL)</a> .                                                   |
| External X'TAL<br>(EHS/ELS X'TAL) |  | <p>The 10 to 25 MHz EHS X'TAL has the advantage of producing a very accurate rate on the main clock</p> <p>ELS X'TAL must have a frequency of 32.768 KHz.</p> |

### 3.2.4 SYSTEM CLOCK (SYSCLK) SELECTION

After a system reset, the IHRC is selected as system clock. When a clock source is used directly or through the PLL as system clock, it is not possible to stop it.

A switch from one clock source to another occurs only if the target clock source is ready (clock stable after startup delay or PLL locked). If a clock source which is not yet ready is selected, the switch will occur when the clock source is ready.

Ready bits in [SYS0\\_CSST](#) register indicate which clock(s) is (are) ready and SYSCLKST bits in [SYS0\\_CLKCFG](#) register indicate which clock is currently used as system clock.

### 3.2.5 CLOCK-OUT CAPABILITY

The MCU clock output (CLKOUT) capability allows the clock to be output onto the external CLKOUT pin. The configuration registers of the corresponding GPIO port must be programmed in alternate function mode.

One of 6 clock signals can be selected as clock output:

1. HCLK
2. IHRC
3. ILRC
4. PLL clock output
5. ELS X'TAL
6. EHS X'TAL

The selection is controlled by the CLKOUTSEL bits in [SYS1\\_AHBCLKEN](#) register.

### 3.3 SYSTEM CONTROL REGISTERS 0

Base Address: 0x4006 0000

#### 3.3.1 Analog Block Control register (SYS0\_ANBCTRL)

Address Offset: 0x00

Reset value: 0x0000 0001

**\* Note: EHSEN / ELSEN / IHRcen bit can NOT be cleared if the EHS X'tal / ELS X'tal / IHRC is selected as system clock or is selected to become the system clock.**

| Bit  | Name     | Description                                                                                                                   | Attribute | Reset |
|------|----------|-------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:6 | Reserved |                                                                                                                               | R         | 0     |
| 5    | EHSFREQ  | Frequency range (driving ability) of EHS X'TAL<br>0: <=12MHz<br>1: >12MHz                                                     | R/W       | 0     |
| 4    | EHSEN    | External high-speed clock enable<br>0: Disable EHS X'TAL.<br>1: Enable EHS X'TAL.                                             | R/W       | 0     |
| 3    | Reserved |                                                                                                                               | R         | 0     |
| 2    | ELSEN    | External low-speed oscillator enable<br>0: Disable External 32.768 KHz oscillator<br>1: Enable External 32.768 KHz oscillator | R/W       | 0     |
| 1    | Reserved |                                                                                                                               | R         | 0     |
| 0    | IHRcen   | Internal high-speed clock enable<br>0: Disable internal 12 MHz RC oscillator.<br>1: Enable internal 12 MHz RC oscillator.     | R/W       | 1     |

#### 3.3.2 PLL control register (SYS0\_PLLCTRL)

Address Offset: 0x04

**\* Note: PLLen bit can NOT be cleared if the PLL is selected as system clock or is selected to become the system clock.**

| Bit   | Name           | Description                                                                                               | Attribute | Reset |
|-------|----------------|-----------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:16 | Reserved       |                                                                                                           | R         | 0     |
| 15    | PLLEN          | PLL enable<br>0: Disable<br>1: Enable                                                                     | R/W       | 0     |
| 14    | Reserved       |                                                                                                           | R         | 0     |
| 13:12 | PLLCLKSEL[1:0] | System PLL clock source<br>00: IHRC 12 MHz oscillator<br>01: EHS X'TAL 10 MHz ~ 25 MHz<br>Other: Reserved | R/W       | 0     |
| 11:9  | Reserved       |                                                                                                           | R         | 0     |
| 8     | FSEL           | Front divider value. The division value F is the programmed $2^{FSEL}$<br>0: F = 1<br>1: F = 2            | R/W       | 0     |

|            |                  |                                                                                                                                  |     |      |
|------------|------------------|----------------------------------------------------------------------------------------------------------------------------------|-----|------|
| <b>7:5</b> | <b>PSEL[2:0]</b> | Post divider value. P= PSEL[2:0]*2<br>000~010: Reserved<br>011: P = 6<br>100: P = 8<br>101: P = 10<br>110: P = 12<br>111: P = 14 | R/W | 011b |
| <b>4:0</b> | <b>MSEL[4:0]</b> | Feedback divider value.<br>M: 3~31                                                                                               | R/W | 0x3  |

To select the appropriate values for M, P, and F, it is recommended to follow these constraints:

1.  $10\text{MHz} \leq F_{\text{CLKIN}} \leq 25\text{MHz}$
2.  $150\text{MHz} \leq F_{\text{VCO}} \leq 330\text{MHz}$
3.  $2 < M \leq 31$
4.  $F = 1$ , or  $2$
5.  $P = 6, 8, 10, 12$ , or  $14$  (**duty 50% +/- 2.5%**)
6.  $F_{\text{CLKOUT}} = 20\text{MHz}, 30\text{MHz}, 40\text{MHz}, 50\text{MHz}, 24\text{MHz}, 36\text{MHz}, 48\text{MHz}, 32\text{MHz}, 22\text{MHz}, 24\text{MHz}, 50\text{MHz}$   
with jitter < ±500 ps

|         | Fclkout | 10MHz | 12MHz | 16MHz | 20MHz | 22MHz | 24MHz | 25MHz | 30MHz | 32MHz | 36MHz | 40MHz | 44MHz | 48MHz | 50MHz |
|---------|---------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Fclkkin |         |       |       |       |       |       |       |       |       |       |       |       |       |       |       |
| 10MHz   |         |       |       |       | V     |       |       |       | V     |       |       | V     |       |       | V     |
| 12MHz   |         |       |       |       |       |       | V     |       |       |       | V     |       |       | V     |       |
| 16MHz   |         |       |       |       |       |       |       |       |       | V     |       |       |       | V     |       |
| 22MHz   |         |       |       |       |       |       |       |       |       |       |       |       | V     |       |       |
| 24MHz   |         |       |       |       |       |       |       |       |       |       |       |       |       | V     |       |
| 25MHz   |         |       |       |       |       |       |       |       |       |       |       |       |       |       | V     |

### 3.3.2.1 RECOMMEND FREQUENCY SETTING

$$F_{\text{VCO}} = F_{\text{CLKIN}} / F * M$$

$$F_{\text{CLKOUT}} = F_{\text{VCO}} / P$$

| <b>F<sub>CLKIN</sub> (MHz)</b> | <b>FSEL</b> | <b>F=2<sup>FEL</sup></b> | <b>MSEL[4:0]=M</b> | <b>F<sub>VCO</sub> (MHz)<br/>=F<sub>CLKIN</sub> / F * M</b> | <b>PSEL[2:0]</b> | <b>P= PSEL[2:0]*2</b> | <b>F<sub>CLKOUT</sub> (MHz)</b> |
|--------------------------------|-------------|--------------------------|--------------------|-------------------------------------------------------------|------------------|-----------------------|---------------------------------|
| 10                             | 0           | 1                        | 20                 | 200                                                         | 5                | 10                    | 20                              |
| 10                             | 0           | 1                        | 22                 | 220                                                         | 5                | 10                    | 22                              |
| 10                             | 0           | 1                        | 18                 | 180                                                         | 3                | 6                     | 30                              |
| 10                             | 0           | 1                        | 24                 | 240                                                         | 3                | 6                     | 40                              |
| 10                             | 0           | 1                        | 30                 | 300                                                         | 3                | 6                     | 50                              |
| 12                             | 0           | 1                        | 16                 | 192                                                         | 4                | 8                     | 24                              |
| 12                             | 0           | 1                        | 18                 | 216                                                         | 3                | 6                     | 36                              |
| 12                             | 0           | 1                        | 24                 | 288                                                         | 3                | 6                     | 48                              |
| 12                             | 0           | 1                        | 25                 | 300                                                         | 3                | 6                     | 50                              |
| 16                             | 0           | 1                        | 16                 | 256                                                         | 4                | 8                     | 32                              |
| 16                             | 0           | 1                        | 18                 | 288                                                         | 3                | 6                     | 48                              |
| 20                             | 1           | 2                        | 30                 | 300                                                         | 3                | 6                     | 50                              |
| 22                             | 0           | 1                        | 12                 | 264                                                         | 3                | 6                     | 44                              |
| 24                             | 0           | 1                        | 12                 | 288                                                         | 3                | 6                     | 48                              |
| 25                             | 0           | 1                        | 12                 | 300                                                         | 3                | 6                     | 50                              |

### 3.3.3 Clock Source Status register (SYS0\_CSST)

Address Offset: 0x08

| Bit | Name | Description | Attribute | Reset |
|-----|------|-------------|-----------|-------|
|-----|------|-------------|-----------|-------|

|             |          |                                                                                                |   |   |
|-------------|----------|------------------------------------------------------------------------------------------------|---|---|
| <b>31:7</b> | Reserved |                                                                                                | R | 0 |
| <b>6</b>    | PLLRDY   | PLL clock ready flag<br>0: PLL unlocked<br>1: PLL locked                                       | R | 0 |
| <b>5</b>    | Reserved |                                                                                                | R | 0 |
| <b>4</b>    | EHSRDY   | External high-speed clock ready flag<br>0: EHS oscillator not ready<br>1: EHS oscillator ready | R | 0 |
| <b>3</b>    | Reserved |                                                                                                | R | 0 |
| <b>2</b>    | ELSRDY   | External low-speed clock ready flag<br>0: ELS oscillator not ready<br>1: ELS oscillator ready  | R | 0 |
| <b>1</b>    | Reserved |                                                                                                | R | 0 |
| <b>0</b>    | IHRCRDY  | IHRC ready flag<br>0: IHRC not ready<br>1: IHRC ready                                          | R | 1 |

### 3.3.4 System Clock Configuration register (SYS0\_CLKCFG)

Address Offset: 0x0C

| Bit         | Name           | Description                                                                                                                                                                                                                                                                                                                      | Attribute | Reset |
|-------------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:7</b> | Reserved       |                                                                                                                                                                                                                                                                                                                                  | R         | 0     |
| <b>6:4</b>  | SYSCLKST[2:0]  | System clock switch status<br>Set and cleared by HW to indicate which clock source is used as system clock.<br>000: IHRC is used as system clock<br>001: ILRC is used as system clock<br>010: EHS X'TAL is used as system clock<br>011: ELS X'TAL is used as system clock<br>100: PLL is used as system clock<br>Other: Reserved | R         | 0     |
| <b>3</b>    | Reserved       |                                                                                                                                                                                                                                                                                                                                  | R         | 0     |
| <b>2:0</b>  | SYSCLKSEL[2:0] | System clock switch<br>Set and cleared by SW.<br>000: IHRC<br>001: ILRC<br>010: EHS X'TAL<br>011: ELS X'TAL<br>100: PLL output<br>Other: Reserved                                                                                                                                                                                | R/W       | 0     |

### 3.3.5 AHB Clock Prescale register (SYS0\_AHBCP)

Address Offset: 0x10

| Bit         | Name         | Description                                                                                                                                                                                                                | Attribute | Reset |
|-------------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:4</b> | Reserved     |                                                                                                                                                                                                                            | R         | 0     |
| <b>3:0</b>  | AHBPRES[3:0] | AHB clock source prescale value<br>0000: SYSCLK / 1<br>0001: SYSCLK / 2<br>0010: SYSCLK / 4<br>0011: SYSCLK / 8<br>0100: SYSCLK / 16<br>0101: SYSCLK / 32<br>0110: SYSCLK / 64<br>0111: SYSCLK / 128<br>1000: SYSCLK / 256 | R/W       | 0     |

|  |  |                                       |  |  |
|--|--|---------------------------------------|--|--|
|  |  | 1001: SYSCLK / 512<br>Other: Reserved |  |  |
|--|--|---------------------------------------|--|--|

### 3.3.6 System Reset Status register (SYS0\_RSTST)

Address Offset: 0x14

This register contains the reset source except DPDWAKEUP reset, since the MODE bits in [PMU\\_CTRL](#) register had presented this case.

| Bit  | Name     | Description                                                                                                                                                                                       | Attribute | Reset |
|------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:5 | Reserved |                                                                                                                                                                                                   | R         | 0     |
| 4    | PORRSTF  | POR reset flag<br>Set by HW when a POR reset occurs.<br>0: Read→No POR reset occurred<br>Write→Clear this bit<br>1: POR reset occurred.                                                           | R/W       | 1     |
| 3    | EXTRSTF  | External reset flag<br>Set by HW when a reset from the <a href="#">RESET</a> pin occurs.<br>0: Read→No reset from RESET pin occurred<br>Write→Clear this bit<br>1: Reset from RESET pin occurred. | R/W       | 0     |
| 2    | LVDRSTF  | LVD reset flag<br>Set by HW when a LVD reset occurs.<br>0: Read→No LVD reset occurred<br>Write→Clear this bit<br>1: LVD reset occurred.                                                           | R/W       | 0     |
| 1    | WDTRSTF  | WDT reset flag<br>Set by HW when a WDT reset occurs.<br>0: Read→No watchdog reset occurred<br>Write→Clear this bit<br>1: Watchdog reset occurred.                                                 | R/W       | 0     |
| 0    | SWRSTF   | Software reset flag<br>Set by HW when a software reset occurs.<br>0: Read→No software reset occurred<br>Write→Clear this bit<br>1: Software reset occurred.                                       | R/W       | 1     |

### 3.3.7 LVD Control register (SYS0\_LVDCTRL)

Address Offset: 0x18

The LVD control register selects four separate threshold values for generating a LVD interrupt to the NVIC or LVD reset.

| Bit   | Name           | Description                                                                 | Attribute | Reset |
|-------|----------------|-----------------------------------------------------------------------------|-----------|-------|
| 31:16 | Reserved       |                                                                             | R         | 0     |
| 15    | LV DEN         | LVD enable<br>0: Disable<br>1: Enable                                       | R/W       | 0     |
| 14    | LVDRSTEN       | LVD Reset enable<br>0: Disable<br>1: Enable                                 | R/W       | 0     |
| 13:7  | Reserved       |                                                                             | R         | 0     |
| 6:4   | LVDINTLVL[2:0] | LVD interrupt level<br>000: 1.80V<br>001: 2.00V<br>010: 2.40V<br>011: 2.70V | R/W       | 0     |

|            |                |                                                                                                                        |     |   |
|------------|----------------|------------------------------------------------------------------------------------------------------------------------|-----|---|
|            |                | 100: 3.00V<br>101: 3.60V<br>Other: Reserved                                                                            |     |   |
| <b>3</b>   | Reserved       |                                                                                                                        | R   | 0 |
| <b>2:0</b> | LVDRSTLVL[2:0] | LVD reset level<br>000: 1.80V<br>001: 2.00V<br>010: 2.40V<br>011: 2.70V<br>100: 3.00V<br>101: 3.60V<br>Other: Reserved | R/W | 0 |

### 3.3.8 External RESET Pin Control register (SYS0\_EXRSTCTRL)

Address Offset: 0x1C

| Bit         | Name     | Description                                                                                                                                      | Attribute | Reset |
|-------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:1</b> | Reserved |                                                                                                                                                  | R         | 0     |
| <b>0</b>    | RESETDIS | External RESET pin disable bit.<br>0: Enable external <u>RESET</u> pin. (P3.10 acts as <u>RESET</u> pin)<br>1: Disable. (P3.10 acts as GPIO pin) | R/W       | 1     |

### 3.3.9 SWD Pin Control register (SYS0\_SWDCTRL)

Address Offset: 0x20

| Bit         | Name     | Description                                                                                                                                 | Attribute | Reset |
|-------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:1</b> | Reserved |                                                                                                                                             | R         | 0     |
| <b>0</b>    | SWDDIS   | SWD pin disable bit.<br>0: Enable SWD pin. (P0.9 acts as SWDIO pin, P0.8 acts as SWCLK pin)<br>1: Disable. (P0.8 and P0.9 act as GPIO pins) | R/W       | 0     |

## 3.4 SYSTEM CONTROL REGISTERS 1

Base Address: 0x4005 E000

### 3.4.1 AHB Clock Enable register (SYS1\_AHBCLKEN)

Address Offset: 0x00

The SYS\_AHBCLKEN register enables the AHB clock to individual system and peripheral blocks.

**\* Note:**

1. When the clock is disabled, the peripheral register values may not be readable by SW and the value returned is always 0x0.
2. HW will replace GPIO with CLKOUT function directly if CLKOUTSEL is Not 0.

| Bit   | Name           | Description                                                                                                                                         | Attribute | Reset |
|-------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31    | Reserved       |                                                                                                                                                     | R         | 0     |
| 30:28 | CLKOUTSEL[2:0] | Clock output source<br>000: Disable<br>001: ILRC clock<br>010: ELS clock<br>100: HCLK<br>101: IHRC clock<br>110: EHS clock<br>111: PLL clock output | R/W       | 0     |
| 27:25 | Reserved       |                                                                                                                                                     | R         | 0     |
| 24    | WDTCLKEN       | Enable clock for WDT.<br>0: Disable<br>1: Enable                                                                                                    | R/W       | 1     |
| 23    | RTCCLKEN       | Enable clock for RTC.<br>0: Disable<br>1: Enable                                                                                                    | R/W       | 0     |
| 22    | I2SCLKEN       | Enable clock for I2S.<br>0: Disable<br>1: Enable                                                                                                    | R/W       | 0     |
| 21    | I2C0CLKEN      | Enable clock for I2C0.<br>0: Disable<br>1: Enable                                                                                                   | R/W       | 0     |
| 20    | I2C1CLKEN      | Enable clock for I2C1.<br>0: Disable<br>1: Enable                                                                                                   | R/W       | 0     |
| 19:18 | Reserved       |                                                                                                                                                     | R         | 0     |
| 17    | USART1CLKEN    | Enable clock for USART1.<br>0: Disable<br>1: Enable                                                                                                 | R/W       | 0     |
| 16    | USART0CLKEN    | Enable clock for USART0.<br>0: Disable<br>1: Enable                                                                                                 | R/W       | 0     |
| 15:14 | Reserved       |                                                                                                                                                     | R         | 0     |
| 13    | SSP1CLKEN      | Enable clock for SSP1.<br>0: Disable<br>1: Enable                                                                                                   | R/W       | 0     |
| 12    | SSP0CLKEN      | Enable clock for SSP0.<br>0: Disable<br>1: Enable                                                                                                   | R/W       | 0     |
| 11    | ADCCLKEN       | Enable clock for ADC.<br>0: Disable                                                                                                                 | R/W       | 0     |

|     |             |                                                     |     |   |
|-----|-------------|-----------------------------------------------------|-----|---|
|     |             | 1: Enable                                           |     |   |
| 10  | CT32B2CLKEN | Enable clock for CT32B2.<br>0: Disable<br>1: Enable | R/W | 0 |
| 9   | CT32B1CLKEN | Enable clock for CT32B1.<br>0: Disable<br>1: Enable | R/W | 0 |
| 8   | CT32B0CLKEN | Enable clock for CT32B0.<br>0: Disable<br>1: Enable | R/W | 0 |
| 7   | CT16B2CLKEN | Enable clock for CT16B2.<br>0: Disable<br>1: Enable | R/W | 0 |
| 6   | CT16B1CLKEN | Enable clock for CT16B1.<br>0: Disable<br>1: Enable | R/W | 0 |
| 5   | CT16B0CLKEN | Enable clock for CT16B0.<br>0: Disable<br>1: Enable | R/W | 0 |
| 4:3 | Reserved    |                                                     | R   | 0 |
| 2   | LCDCLKEN    | Enable clock for LCD<br>0: Disable<br>1: Enable     | R/W | 0 |
| 1   | Reserved    |                                                     | R   | 0 |
| 0   | GPIOCLKEN   | Enable clock for GPIO.<br>0: Disable<br>1: Enable   | R/W | 1 |

### 3.4.2 APB Clock Prescale register 0 (SYS1\_APB0)

Address Offset: 0x04

**\* Note:** Must reset the corresponding peripheral with SYS1\_PRST register after changing the prescale value.

| Bit   | Name           | Description                                                                                                                            | Attribute | Reset |
|-------|----------------|----------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31    | Reserved       |                                                                                                                                        | R         | 0     |
| 30:28 | CT32B2PRE[2:0] | CT32B2 clock source prescaler<br>000: HCLK / 1<br>001: HCLK / 2<br>010: HCLK / 4<br>011: HCLK / 8<br>100: HCLK / 16<br>Other: Reserved | R/W       | 0     |
| 27    | Reserved       |                                                                                                                                        | R         | 0     |
| 26:24 | SSP1PRE[2:0]   | SSP1 clock source prescaler<br>000: HCLK / 1<br>001: HCLK / 2<br>010: HCLK / 4<br>011: HCLK / 8<br>100: HCLK / 16<br>Other: Reserved   | R/W       | 0     |
| 23    | Reserved       |                                                                                                                                        | R         | 0     |
| 22:20 | SSP0PRE[2:0]   | SSP0 clock source prescaler<br>000: HCLK / 1<br>001: HCLK / 2                                                                          | R/W       | 0     |

|              |                |                                                                                                                                         |     |   |
|--------------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------|-----|---|
|              |                | 010: HCLK / 4<br>011: HCLK / 8<br>100: HCLK / 16<br>Other: Reserved                                                                     |     |   |
| <b>19</b>    | Reserved       |                                                                                                                                         | R   | 0 |
| <b>18:16</b> | ADCPRE[2:0]    | ADC clock source prescaler<br>000: HCLK / 1<br>001: HCLK / 2<br>010: HCLK / 4<br>011: HCLK / 8<br>100: HCLK / 16<br>Other: Reserved     | R/W | 0 |
| <b>15</b>    | Reserved       |                                                                                                                                         | R   | 0 |
| <b>14:12</b> | CT32B1PRE[2:0] | CT32B1 clock source prescaler<br>000: HCLK / 1<br>001: HCLK / 2<br>010: HCLK / 4<br>011: HCLK / 8<br>100: HCLK / 16<br>Other: Reserved  | R/W | 0 |
| <b>11</b>    | Reserved       |                                                                                                                                         | R   | 0 |
| <b>10:8</b>  | CT32B0PRE[2:0] | CT32B0 clock source prescaler.<br>000: HCLK / 1<br>001: HCLK / 2<br>010: HCLK / 4<br>011: HCLK / 8<br>100: HCLK / 16<br>Other: Reserved | R/W | 0 |
| <b>7</b>     | Reserved       |                                                                                                                                         | R   | 0 |
| <b>6:4</b>   | CT16B1PRE[2:0] | CT16B1 clock source prescaler<br>000: HCLK / 1<br>001: HCLK / 2<br>010: HCLK / 4<br>011: HCLK / 8<br>100: HCLK / 16<br>Other: Reserved  | R/W | 0 |
| <b>3</b>     | Reserved       |                                                                                                                                         | R   | 0 |
| <b>2:0</b>   | CT16B0PRE[2:0] | CT16B0 clock source prescaler<br>000: HCLK / 1<br>001: HCLK / 2<br>010: HCLK / 4<br>011: HCLK / 8<br>100: HCLK / 16<br>Other: Reserved  | R/W | 0 |

### 3.4.3 APB Clock Prescale register 1 (SYS1\_APB1CP1)

Address Offset: 0x08

**\* Note: Must reset the corresponding peripheral with SYS1\_PRST register after changing the prescale value.**

| Bit       | Name     | Description | Attribute | Reset |
|-----------|----------|-------------|-----------|-------|
| <b>31</b> | Reserved |             | R         | 0     |

|              |                |                                                                                                                                                                                                                                                                                                 |    |   |
|--------------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|---|
| <b>30:28</b> | CT16B2PRE[2:0] | CT16B2 clock source prescaler<br>000: HCLK / 1<br>001: HCLK / 2<br>010: HCLK / 4<br>011: HCLK / 8<br>100: HCLK / 16<br>Other: Reserved                                                                                                                                                          | RW | 0 |
| <b>27</b>    | Reserved       |                                                                                                                                                                                                                                                                                                 | R  | 0 |
| <b>26:24</b> | I2C1PRE[2:0]   | I2C1 clock source prescaler<br>000: HCLK / 1<br>001: HCLK / 2<br>010: HCLK / 4<br>011: HCLK / 8<br>100: HCLK / 16<br>Other: Reserved                                                                                                                                                            | RW | 0 |
| <b>23</b>    | Reserved       |                                                                                                                                                                                                                                                                                                 | R  | 0 |
| <b>22:20</b> | WDTPRE[2:0]    | WDT clock source prescaler<br>000: WDT_PCLK = WDT clock source / 1<br>001: WDT_PCLK = WDT clock source / 2<br>010: WDT_PCLK = WDT clock source / 4<br>011: WDT_PCLK = WDT clock source / 8<br>100: WDT_PCLK = WDT clock source / 16<br>101: WDT_PCLK = WDT clock source / 32<br>Other: Reserved | RW | 0 |
| <b>19:15</b> | Reserved       |                                                                                                                                                                                                                                                                                                 | R  | 0 |
| <b>14:12</b> | I2SPRE[2:0]    | I2S clock source prescaler<br>000: HCLK / 1<br>001: HCLK / 2<br>010: HCLK / 4<br>011: HCLK / 8<br>100: HCLK / 16<br>111: HCLK / 3<br>Other: Reserved                                                                                                                                            | RW | 0 |
| <b>11</b>    | Reserved       |                                                                                                                                                                                                                                                                                                 | R  | 0 |
| <b>10:8</b>  | I2C0PRE[2:0]   | I2C0 clock source prescaler<br>000: HCLK / 1<br>001: HCLK / 2<br>010: HCLK / 4<br>011: HCLK / 8<br>100: HCLK / 16<br>Other: Reserved                                                                                                                                                            | RW | 0 |
| <b>7</b>     | Reserved       |                                                                                                                                                                                                                                                                                                 | R  | 0 |
| <b>6:4</b>   | USART1PRE[2:0] | USART1 clock source prescaler<br>000: HCLK / 1<br>001: HCLK / 2<br>010: HCLK / 4<br>011: HCLK / 8<br>100: HCLK / 16<br>Other: Reserved                                                                                                                                                          | RW | 0 |
| <b>3</b>     | Reserved       |                                                                                                                                                                                                                                                                                                 | R  | 0 |
| <b>2:0</b>   | USART0PRE[2:0] | USART0 clock source prescaler<br>000: HCLK / 1<br>001: HCLK / 2<br>010: HCLK / 4<br>011: HCLK / 8<br>100: HCLK / 16<br>Other: Reserved                                                                                                                                                          | RW | 0 |

### 3.4.4 APB Clock Prescale register 2 (SYS1\_APBPCP2)

Address Offset: 0x0C

| Bit  | Name           | Description                                                                                                                                                                                                                                                                                                                                                        | Attribute | Reset |
|------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:4 | Reserved       |                                                                                                                                                                                                                                                                                                                                                                    | R         | 0     |
| 3:0  | CLKOUTPRE[3:0] | Clock-out source prescaler<br>0000: Clock-out source / 1<br>0001: Clock-out source / 2<br>0010: Clock-out source / 4<br>0011: Clock-out source / 8<br>0100: Clock-out source / 16<br>0101: Clock-out source / 32<br>0110: Clock-out source / 64<br>0111: Clock-out source / 128<br>1000: Clock-out source / 256<br>1001: Clock-out source / 512<br>Other: Reserved | R/W       | 0     |

### 3.4.5 Peripheral Reset register (SYS1\_PRST)

Address Offset: 0x10

All bits are cleared by HW automatically after setting as "1".

| Bit   | Name      | Description                                     | Attribute | Reset |
|-------|-----------|-------------------------------------------------|-----------|-------|
| 31:25 | Reserved  |                                                 | R         | 0     |
| 24    | WDTRST    | WDT reset<br>0: No effect<br>1: Reset WDT       | R/W       | 0     |
| 23    | RTCRST    | RTC reset<br>0: No effect<br>1: Reset RTC       | R/W       | 0     |
| 22    | I2SRST    | I2S reset<br>0: No effect<br>1: Reset I2S       | R/W       | 0     |
| 21    | I2C0RST   | I2C0 reset<br>0: No effect<br>1: Reset I2C0     | R/W       | 0     |
| 20    | I2C1RST   | I2C1 reset<br>0: No effect<br>1: Reset I2C1     | R/W       | 0     |
| 19:18 | Reserved  |                                                 | R         | 0     |
| 17    | USART1RST | USART1 reset<br>0: No effect<br>1: Reset USART1 | R/W       | 0     |
| 16    | USART0RST | USART0 reset<br>0: No effect<br>1: Reset USART0 | R/W       | 0     |
| 15    | LCDRST    | LCD reset<br>0: No effect<br>1: Reset LCD       | R/W       | 0     |
| 14    | Reserved  |                                                 | R         | 0     |
| 13    | SSP1RST   | SSP1 reset<br>0: No effect<br>1: Reset SSP1     | R/W       | 0     |

|           |           |                                                           |     |   |
|-----------|-----------|-----------------------------------------------------------|-----|---|
| <b>12</b> | SSP0RST   | SSP0 reset<br>0: No effect<br>1: Reset SSP0               | R/W | 0 |
| <b>11</b> | ADCRST    | ADC reset<br>0: No effect<br>1: Reset ADC                 | R/W | 0 |
| <b>10</b> | CT32B2RST | CT32B2 reset<br>0: No effect<br>1: Reset CT32B2           | R/W | 0 |
| <b>9</b>  | CT32B1RST | CT32B1 reset<br>0: No effect<br>1: Reset CT32B1           | R/W | 0 |
| <b>8</b>  | CT32B0RST | CT32B0 reset<br>0: No effect<br>1: Reset CT32B0           | R/W | 0 |
| <b>7</b>  | CT16B2RST | CT16B2 reset<br>0: No effect<br>1: Reset CT16B2           | R/W | 0 |
| <b>6</b>  | CT16B1RST | CT16B1 reset<br>0: No effect<br>1: Reset CT16B1           | R/W | 0 |
| <b>5</b>  | CT16B0RST | CT16B0 reset<br>0: No effect<br>1: Reset CT16B0           | R/W | 0 |
| <b>4</b>  | Reserved  |                                                           | R   | 0 |
| <b>3</b>  | GPIOP3RST | GPIO port 3 reset<br>0: No effect<br>1: Reset GPIO port 3 | R/W | 0 |
| <b>2</b>  | GPIOP2RST | GPIO port 2 reset<br>0: No effect<br>1: Reset GPIO port 2 | R/W | 0 |
| <b>1</b>  | GPIOP1RST | GPIO port 1 reset<br>0: No effect<br>1: Reset GPIO port 1 | R/W | 0 |
| <b>0</b>  | GPIOP0RST | GPIO port 0 reset<br>0: No effect<br>1: Reset GPIO port 0 | R/W | 0 |

### 3.4.6 Divider Dividend register (SYS1\_DIVIDEND)

Address Offset: 0x20

| Bit  | Name           | Description               | Attribute | Reset |
|------|----------------|---------------------------|-----------|-------|
| 31:0 | Dividend[31:0] | Unsigned integer Dividend | R/W       | 0     |

### 3.4.7 Divider Divisor register (SYS1\_DIVISOR)

Address Offset: 0x24

|                                                                                                                                                       |  |  |  |  |
|-------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|
| <p><b>*</b> <i>Note: Quotient is 0xFFFFFFFF when Divisor is 0x0, instead of occurring Hard Fault, since FW shall be able to handle this case.</i></p> |  |  |  |  |
|-------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|

| Bit  | Name          | Description              | Attribute | Reset |
|------|---------------|--------------------------|-----------|-------|
| 31:0 | Divisor[31:0] | Unsigned integer Divisor | R/W       | 0     |

### 3.4.8 Divider Quotient register (SYS1\_QUOTIENT)

Address Offset: 0x28

|                                                                                                                                                       |  |  |  |  |
|-------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|
| <p><b>*</b> <i>Note: Quotient is 0xFFFFFFFF when Divisor is 0x0, instead of occurring Hard Fault, since FW shall be able to handle this case.</i></p> |  |  |  |  |
|-------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|

| Bit  | Name           | Description               | Attribute | Reset |
|------|----------------|---------------------------|-----------|-------|
| 31:0 | Quotient[31:0] | Unsigned integer Quotient | R/W       | 0     |

### 3.4.9 Divider Remainder register (SYS1\_REMAINDER)

Address Offset: 0x2C

| Bit  | Name            | Description                | Attribute | Reset |
|------|-----------------|----------------------------|-----------|-------|
| 31:0 | Remainder[31:0] | Unsigned integer Remainder | R/W       | 0     |

### 3.4.10 Divider Control register (SYS1\_DIVCTRL)

Address Offset: 0x30

| Bit  | Name     | Description                                                                                                                                                                      | Attribute | Reset |
|------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:1 | Reserved |                                                                                                                                                                                  | R         | 0     |
| 0    | DIVS     | Divider start control bit.<br>0: Divider stops/finishes operation.<br>1: Start to execute Dividing. DIVS is cleared by HW automatically when the operation of dividing finishes. | R/W       | 0     |

# 4 SYSTEM OPERATION MODE

## 4.1 OVERVIEW

The chip builds in 3 operating modes for difference clock rate and power saving reason. These modes control oscillators, op-code operation and analog peripheral devices' operation.

- Normal mode
- Sleep mode
- Deep sleep mode

## 4.2 NORMAL MODE

In Normal mode, the ARM Cortex-M0 core, memories, and peripherals are clocked by the system clock. The [SYS1\\_AHBCLKEN](#) register controls which peripherals are running.

Selected peripherals have individual peripheral clocks with their own clock dividers in addition to the system clock. The peripheral clocks can be disabled respectively.

The power to various analog blocks (IHRC, EHS X'TAL, ELS X'TAL, PLL, Flash, LVD, ADC) can be controlled at any time individually through the enable bit of all blocks.

## 4.3 LOW-POWER MODES

There are 2 special modes of processor power reduction: Sleep mode, and Deep-sleep mode. The [PMU\\_CTRL](#) register controls which mode is desired.

The CPU clock rate may also be controlled as needed by changing clock sources, re-configuring PLL values, and/or altering the system clock divider value. This allows a trade-off of power versus processing speed based on application requirements.

Run-time power control allows disable the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider for power control.

**\* Note:**

1. *The debug mode is not supported in Deep-sleep mode.*
2. *The pins which are not pin-out shall be set correctly to decrease power consumption in low-power modes. Strongly recommended to set these pins as input pull-up.*

### 4.3.1 SLEEP MODE

In Sleep mode, the system clock to the ARM Cortex-M0 core is stopped and execution of instructions is suspended.

Peripheral functions, if selected to be clocked in [SYS1\\_AHBCLKEN](#) register, continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

The power state of the analog blocks (IHRC, EHS X'TAL, ELS X'TAL, PLL, Flash, LVD, ADC) is determined by the enable bit of all blocks.

The processor state and registers, peripheral registers, and internal SRAM values are maintained and the logic levels of the pins remain static.

Wake up the chip from Sleep mode by an interrupt occurs.

The RESET pin has keep functionality in Sleep mode.

The Sleep mode is entered by using the following steps:

1. Write 4 to [PMU\\_CTRL](#) register.
2. Execute ARM Cortex-M0 WFI instruction.

### 4.3.2 DEEP-SLEEP MODE

In Deep-sleep mode, the system clock to the ARM Cortex-M0 core is stopped, and execution of instructions is suspended.

The clock to the peripheral functions are stopped because the power state of oscillators are powered down, the clock source are stopped, except RTC or LCD low speed clock source (ELS X'TAL, ILRC) if used.

**\* Note: User SHALL decide to power down low speed clock source (ELS X'TAL, ILRC oscillator) or not if RTC or LCD is enabled.**

The processor state and registers, peripheral registers, and internal SRAM values are maintained and the logic levels of the pins remain static.

All GPIO pins are served as wakeup pins. The user must program the GPIO registers for each pin to set the appropriate edge polarity for the corresponding wakeup event, only edge sensitive is supported to wakeup MCU. The system will exit Deep-sleep mode when GPIO indicates a GPIO interrupt to the ARM core. Furthermore, the interrupts corresponding to each input must be enabled in the NVIC.

**\* Note: Strongly recommended to set the GPIO wake-up condition to both edge sensing.**

The RESET pin has keep functionality in Deep-sleep mode.

The Deep-sleep mode is entered by using the following steps:

1. Write 2 to [PMU\\_CTRL](#) register.
2. Execute ARM WFI instruction.

The advantage of the Deep-sleep mode is that can power down clock generating blocks such as oscillators and PLL, thereby gaining far greater dynamic power savings over Sleep mode. In addition, the Flash can be powered down in Deep-sleep mode resulting in savings in static leakage power, however at the expense of longer wake-up times for the Flash memory.

## 4.4 WAKEUP

### 4.4.1 OVERVIEW

Under low power mode, program doesn't execute. The wakeup trigger can wake the system up to normal mode. The wakeup function builds in interrupt operation and trigger system executing interrupt service routine as system wakeup occurrence.

- \* The wakeup trigger sources of the Sleep mode are all interrupts and the RESET pin.
- \* The wakeup trigger sources of the Deep-sleep mode are the GPIO interrupt, RTC interrupt, LCD interrupt, and the RESET pin.

### 4.4.2 WAKEUP TIME

When the system is in Sleep mode, the high clock is enabled or disabled by FW. If the high clock stops and MCU is waken up from Sleep mode, MCU waits for 2048 external high-speed oscillator clocks and 32 internal high-speed oscillator clocks as the wakeup time to stable the oscillator circuit. After the wakeup time, the system goes into the normal mode.

\* **Note:** Wakeup from Sleep mode spends NO wakeup time if the clock doesn't stop.

When the system is in Deep-sleep mode, the high clock will stop. When MCU is waken up from Deep-sleep mode, MCU waits for  $2T \cdot ILRC$  and  $IHRC/EHS$  warm up time ( $32T \cdot IHRC/2048T \cdot EHS$ ). After the wakeup time, the system goes into the normal mode.

The value of the external high clock oscillator wakeup time from Deep sleep mode is as the following.

**The total Wakeup time of EHS  $X'tal = 2T \cdot ILRC + 1/F_{EHS} \cdot 2048$  (sec) + high clock start-up time**

- Example:  $F_{EHS}=20\text{MHz}$ , the wakeup time from Deep sleep mode is as the following.

$$\begin{aligned} \text{The total Wakeup time} &= 2T \cdot ILRC + 1/F_{EHS} \cdot 2048 + \text{oscillator start-up time} \\ &= 62.5\mu\text{s} + 112.4\mu\text{s} + \text{oscillator start-up time} \quad (F_{EHS} = 20\text{MHz}) \end{aligned}$$

The value of the IHRC wakeup time is as the following.

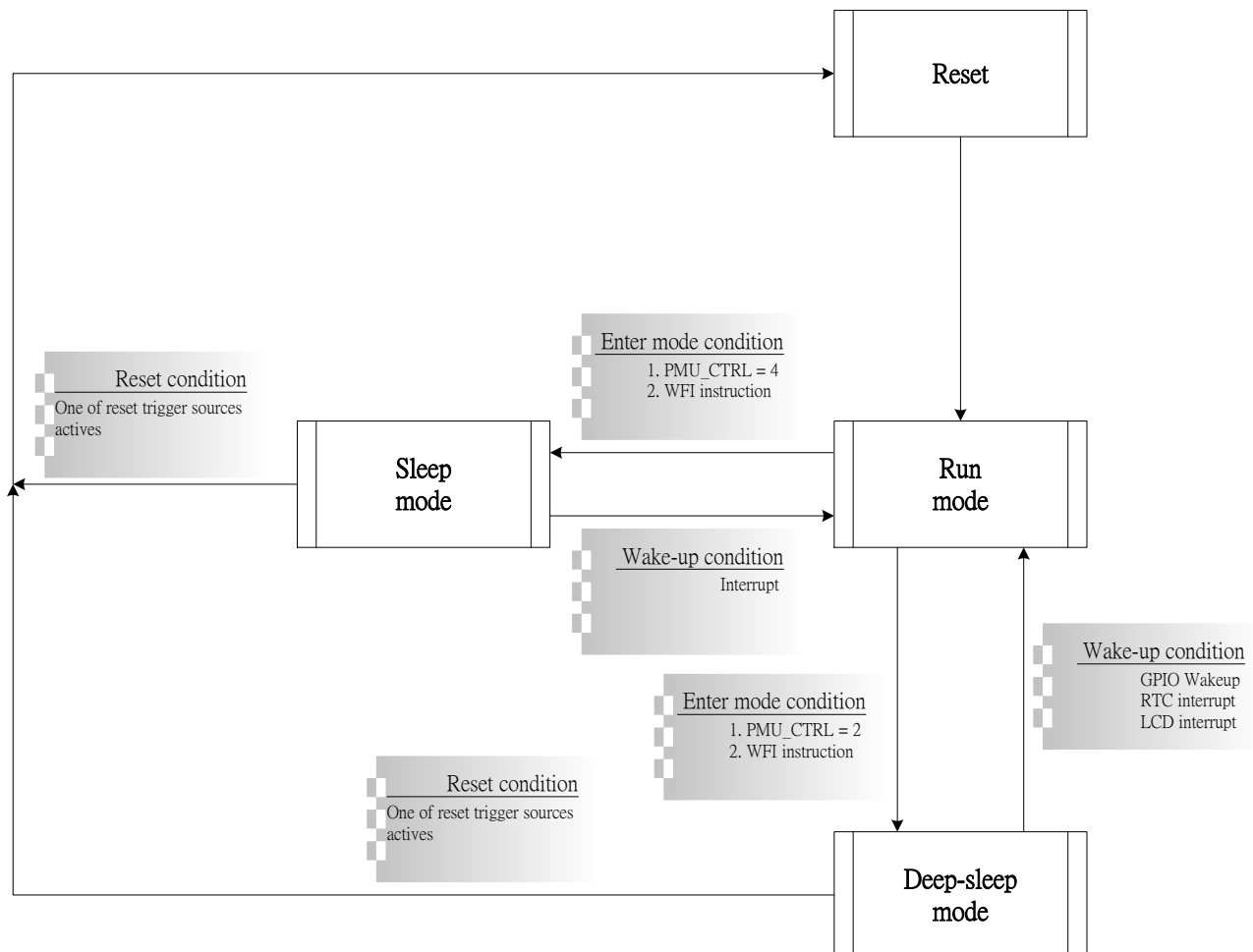
**The total Wakeup time of IHRC  $= 2T \cdot ILRC + 1/F_{IHRC} \cdot 32$  (sec)**

- Example:  $F_{IHRC}=12\text{MHz}$ , the wakeup time is as the following.

$$\text{The total Wakeup time} = 2T \cdot ILRC + 1/F_{IHRC} \cdot 32 = 62.5\mu\text{s} + 2.67\mu\text{s} \quad (F_{IHRC} = 12\text{MHz})$$

\* **Note:** The high clock start-up time is depended on the VDD and oscillator type of high clock.

## 4.5 STATE MACHINE OF PMU



## 4.6 OPERATION MODE COMPARSION TABLE

| Operation Mode | Normal Mode                       | Low-Power Mode            |                                                         |
|----------------|-----------------------------------|---------------------------|---------------------------------------------------------|
|                |                                   | Sleep Mode                | Deep-Sleep Mode                                         |
| IHRC           | By IHRCEN                         |                           | Disable                                                 |
| ILRC           | ON                                |                           | ***                                                     |
| EHS X'TAL      | By EHSEN                          |                           | Disable                                                 |
| ELS X'TAL      | By ELSEN                          |                           | ***                                                     |
| PLL            | By PLEN                           |                           | Disable                                                 |
| Cortex-M0      | Running                           | Stop                      | Stop                                                    |
| Flash ROM      | Enable                            | Disable                   | Disable                                                 |
| RAM            | Enable                            | Maintain                  | Maintain                                                |
| ADC            | By ADENB                          |                           | Disable                                                 |
| LVD            | By LVDEN                          |                           | Disable                                                 |
| LCD            | By LCDENB                         |                           | ***                                                     |
| RTC            | By RTCEN                          |                           | By RTCEN                                                |
| Peripherals    | By Enable bit of each peripherals |                           | Disable HCLK                                            |
| IO status      | -                                 | Maintained                | Maintained                                              |
| Wakeup Source  | N/A                               | All interrupts, RESET pin | GPIO interrupt, RTC interrupt, LCD interrupt, RESET pin |

\*\*\*

| LCDENB | LCDCLK              | RTCENB | RTC_CLKS            | ILRC*  | ELS*   |
|--------|---------------------|--------|---------------------|--------|--------|
| 0      | ---                 | 0      | ---                 | X      | X      |
|        |                     | 1      | 0 (ILRC)<br>1 (ELS) | O<br>X | X<br>O |
| 1      | 0 (ILRC)<br>1 (ELS) | 0      | ---                 | O<br>X | X<br>O |
|        | 0 (ILRC)<br>1 (ELS) |        |                     | O<br>X | X<br>O |
| 1      | 0 (ILRC)<br>1 (ELS) | 1      | 0 (ILRC)<br>1 (ELS) | O<br>X | X<br>O |
|        | 0 (ILRC)<br>1 (ELS) |        | 1 (ELS)<br>0 (ILRC) | O<br>O | O<br>O |

## 4.7 PMU REGISTERS

Base Address: 0x4003 2000

### 4.7.1 Power Control register (PMU\_CTRL)

Address Offset: 0x40

The power control register selects whether one of the ARM Cortex-M0 controlled power-down modes (Sleep mode or Deep-sleep mode) is entered and provides the flags for Sleep or Deep-sleep modes respectively.

**\* Note: The pins which are not pin-out shall be set correctly to decrease power consumption in low-power modes. Strongly recommended to set these pins as input pull-up.**

| Bit  | Name      | Description                                                                                                                                                                                       | Attribute | Reset |
|------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:3 | Reserved  |                                                                                                                                                                                                   | R         | 0     |
| 2:0  | MODE[2:0] | Low power mode selection<br>000: Disable.<br>001: Reserved<br>010: WFI instruction will make MCU enter Deep-sleep mode.<br>100: WFI instruction will make MCU enter Sleep mode.<br>Other: Disable | R/W       | 0     |

# 5 GENERAL PURPOSE I/O PORT (GPIO)

## 5.1 OVERVIEW

Digital ports can be configured input/output by SW

- Each individual port pin can serve as external interrupt input pin.
- Interrupts can be configured on single falling or rising edges and on both edges.
- The I/O configuration registers control the electrical characteristics of the pads.
- Internal pull-up/pull-down resistor.
- Most of the I/O pins are mixed with analog pins and special function pins.

## 5.2 GPIO MODE

All GPIO pins are inputs and floating by default. The MODE bits in the [GPIO<sub>n</sub>\\_CFG](#) (n=0,1,2,3) register allow the selection of on-chip pull-up or pull-down resistors for each pin or select the repeater mode.

The repeater mode enables the pull-up resistor if the pin is logic HIGH and enables the pull-down resistor if the pin is logic LOW. This causes the pin to retain its last known state if it is configured as an input and is not driven externally.

## 5.3 GPIO REGISTERS

Base Address: 0x4004 4000 (GPIO 0)  
 0x4004 6000 (GPIO 1)  
 0x4004 8000 (GPIO 2)  
 0x4004 A000 (GPIO 3)

### 5.3.1 GPIO Port n Data register (GPION\_DATA) (n=0,1,2,3)

Address offset: 0x00

| Bit   | Name       | Description                                                | Attribute | Reset |
|-------|------------|------------------------------------------------------------|-----------|-------|
| 31:16 | Reserved   |                                                            | R         | 0     |
| 15:0  | DATA[15:0] | Input data (read) or output data (write) for Pn.0 to Pn.15 | R/W       | 0     |

### 5.3.2 GPIO Port n Mode register (GPION\_MODE) (n=0,1,2,3)

Address offset: 0x04

**\* Note: HW will switch I/O Mode directly when Specific function (Peripheral, ADC) is enabled, not through GPION\_MODE register.**

| Bit   | Name          | Description                                                                                                          | Attribute | Reset |
|-------|---------------|----------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:16 | CURRENT[15:0] | Driving/Sinking current selection (x = 0 to 15)<br>0: Typical 10mA<br>1: Typical 20mA                                | R/W       | 0     |
| 15:0  | MODE[15:0]    | Selects pin x as input or output (x = 0 to 15)<br>0: Pn.x is configured as input<br>1: Pn.x is configured as output. | R/W       | 0     |

### 5.3.3 GPIO Port n Configuration register (GPION\_CFG) (n=0,1,3)

Address offset: 0x08  
 Reset value: 0xAAAAAAAA

**\* Note: HW will switch I/O Mode directly when Specific function (Peripheral, ADC) is enabled, not through GPION\_MODE register.**

| Bit   | Name       | Description                                                                                                                                                               | Attribute | Reset |
|-------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:30 | CFG15[1:0] | Configuration of Pn.15<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled).<br>11: Repeater mode. | R/W       | 10b   |
| 29:28 | CFG14[1:0] | Configuration of Pn.14<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled).                       | R/W       | 10b   |

|       |            |                                                                                                                                                                           |     |     |
|-------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|
|       |            | 11: Repeater mode.                                                                                                                                                        |     |     |
| 27:26 | CFG13[1:0] | Configuration of Pn.13<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled).<br>11: Repeater mode. | R/W | 10b |
| 25:24 | CFG12[1:0] | Configuration of Pn.12<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled).<br>11: Repeater mode. | R/W | 10b |
| 23:22 | CFG11[1:0] | Configuration of Pn.11<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled).<br>11: Repeater mode. | R/W | 10b |
| 21:20 | CFG10[1:0] | Configuration of Pn.10<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled).<br>11: Repeater mode. | R/W | 10b |
| 19:18 | CFG9[1:0]  | Configuration of Pn.9<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled).<br>11: Repeater mode.  | R/W | 10b |
| 17:16 | CFG8[1:0]  | Configuration of Pn.8<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled).<br>11: Repeater mode.  | R/W | 10b |
| 15:14 | CFG7[1:0]  | Configuration of Pn.7<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled).<br>11: Repeater mode.  | R/W | 10b |
| 13:12 | CFG6[1:0]  | Configuration of Pn.6<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled).<br>11: Repeater mode.  | R/W | 10b |
| 11:10 | CFG5[1:0]  | Configuration of Pn.5<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled).<br>11: Repeater mode.  | R/W | 10b |
| 9:8   | CFG4[1:0]  | Configuration of Pn.4<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled).<br>11: Repeater mode.  | R/W | 10b |
| 7:6   | CFG3[1:0]  | Configuration of Pn.3<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled).<br>11: Repeater mode.  | R/W | 10b |
| 5:4   | CFG2[1:0]  | Configuration of Pn.2<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled).<br>11: Repeater mode.  | R/W | 10b |
| 3:2   | CFG1[1:0]  | Configuration of Pn.1<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled).<br>11: Repeater mode.  | R/W | 10b |
| 1:0   | CFG0[1:0]  | Configuration of Pn.0<br>00: Pull-up resistor enabled.                                                                                                                    | R/W | 10b |

|  |  |                                                                                                                |  |  |
|--|--|----------------------------------------------------------------------------------------------------------------|--|--|
|  |  | 01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled).<br>11: Repeater mode. |  |  |
|--|--|----------------------------------------------------------------------------------------------------------------|--|--|

### 5.3.4 GPIO Port n Configuration register (GPIO<sub>n</sub>\_CFG) (n=2)

Address offset: 0x08

Reset value: 0xAAAAAAAA

**\* Note:** HW will switch I/O Mode directly when Specific function (Peripheral, ADC) is enabled, not through GPIO<sub>n</sub>\_MODE register.

| Bit   | Name       | Description                                                                                                                                                                                                                                                                             | Attribute | Reset |
|-------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:30 | CFG15[1:0] | Configuration of Pn.15<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger enabled).<br>11: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low). | R/W       | 10b   |
| 29:28 | CFG14[1:0] | Configuration of Pn.14<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger enabled).<br>11: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low). | R/W       | 10b   |
| 27:26 | CFG13[1:0] | Configuration of Pn.13<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger enabled).<br>11: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low). | R/W       | 10b   |
| 25:24 | CFG12[1:0] | Configuration of Pn.12<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger enabled).<br>11: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low). | R/W       | 10b   |
| 23:22 | CFG11[1:0] | Configuration of Pn.11<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger enabled).<br>11: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low). | R/W       | 10b   |
| 21:20 | CFG10[1:0] | Configuration of Pn.10<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger enabled).<br>11: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low). | R/W       | 10b   |
| 19:18 | CFG9[1:0]  | Configuration of Pn.9<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger enabled).<br>11: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low).  | R/W       | 10b   |
| 17:16 | CFG8[1:0]  | Configuration of Pn.8<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger enabled).<br>11: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low).  | R/W       | 10b   |

|              |                  |                                                                                                                                                                                                                                                                                        |     |     |
|--------------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|
| <b>15:14</b> | <b>CFG7[1:0]</b> | Configuration of Pn.7<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger enabled).<br>11: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low). | R/W | 10b |
| <b>13:12</b> | <b>CFG6[1:0]</b> | Configuration of Pn.6<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger enabled).<br>11: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low). | R/W | 10b |
| <b>11:10</b> | <b>CFG5[1:0]</b> | Configuration of Pn.5<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger enabled).<br>11: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low). | R/W | 10b |
| <b>9:8</b>   | <b>CFG4[1:0]</b> | Configuration of Pn.4<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger enabled).<br>11: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low). | R/W | 10b |
| <b>7:6</b>   | <b>CFG3[1:0]</b> | Configuration of Pn.3<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger enabled).<br>11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low).      | R/W | 10b |
| <b>5:4</b>   | <b>CFG2[1:0]</b> | Configuration of Pn.2<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger enabled).<br>11: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low). | R/W | 10b |
| <b>3:2</b>   | <b>CFG1[1:0]</b> | Configuration of Pn.1<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger enabled).<br>11: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low). | R/W | 10b |
| <b>1:0</b>   | <b>CFG0[1:0]</b> | Configuration of Pn.0<br>00: Pull-up resistor enabled.<br>01: Pull-down resistor enabled.<br>10: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger enabled).<br>11: Inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low). | R/W | 10b |

### 5.3.5 GPIO Port n Interrupt Sense register (GPIO<sub>n</sub>\_IS) (n=0,1,2,3)

Address offset: 0x0C

| Bit          | Name            | Description                                                                                                                                                                             | Attribute | Reset |
|--------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:16</b> | Reserved        |                                                                                                                                                                                         | R         | 0     |
| <b>15:0</b>  | <b>IS[15:0]</b> | Selects interrupt on pin x as level or edge sensitive (x = 0 to 15).<br>0: Interrupt on Pn.x is configured as edge sensitive.<br>1: Interrupt on Pn.x is configured as event sensitive. | R/W       | 0     |

### 5.3.6 GPIO Port n Interrupt Both-edge Sense register (GPIO<sub>n</sub>\_IBS) (n=0,1,2,3)

Address offset: 0x10

| Bit   | Name      | Description                                                                                                                                                                              | Attribute | Reset |
|-------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:16 | Reserved  |                                                                                                                                                                                          | R         | 0     |
| 15:0  | IBS[15:0] | Selects interrupt on Pn.x to be triggered on both edges (x = 0 to 15).<br>0: Interrupt on Pn.x is controlled through register GPIOn_IIEV.<br>1: Both edges on Pn.x trigger an interrupt. | R/W       | 0     |

### 5.3.7 GPIO Port n Interrupt Event register (GPIOn\_IIEV) (n=0,1,2,3)

Address offset: 0x14

| Bit   | Name       | Description                                                                                                                                                                                                                                                                                             | Attribute | Reset |
|-------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:16 | Reserved   |                                                                                                                                                                                                                                                                                                         | R         | 0     |
| 15:0  | IIEV[15:0] | Selects interrupt on pin x to be triggered rising or falling edges (x = 0 to 15).<br>0: Depending on setting in register GPIOn_IIS, Rising edges or HIGH level on Pn.x trigger an interrupt.<br>1: Depending on setting in register GPIOn_IIS, Falling edges or LOW level on Pn.x trigger an interrupt. | R/W       | 0     |

### 5.3.8 GPIO Port n Interrupt Enable register (GPIOn\_IIE) (n=0,1,2,3)

Address offset: 0x18

Bits set to HIGH in the GPIOn\_IIE register allow the corresponding pins to trigger their individual interrupts. Clearing a bit disables interrupt triggering on that pin.

| Bit   | Name      | Description                                                                                                            | Attribute | Reset |
|-------|-----------|------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:16 | Reserved  |                                                                                                                        | R         | 0     |
| 15:0  | IIE[15:0] | Selects interrupt on pin x to be enabled (x = 0 to 15).<br>0: Disable Interrupt on Pn.x<br>1: Enable Interrupt on Pn.x | R/W       | 0     |

### 5.3.9 GPIO Port n Raw Interrupt Status register (GPIOn\_IRIS) (n=0,1,2,3)

Address offset: 0x1C

This register indicates the status for GPIO control raw interrupts. A GPIO interrupt is sent to the interrupt controller if the corresponding bit in GPIOn\_IIE register is set.

| Bit   | Name       | Description                                                                                                 | Attribute | Reset |
|-------|------------|-------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:16 | Reserved   |                                                                                                             | R         | 0     |
| 15:0  | IRIS[15:0] | GPIO raw interrupt flag (x = 0 to 15).<br>0: No interrupt on Pn.x<br>1: Interrupt requirements met on Pn.x. | R         | 0     |

### 5.3.10 GPIO Port n Interrupt Clear register (GPIOn\_IC) (n=0,1,2,3)

Address offset: 0x20

| Bit   | Name     | Description                                                  | Attribute | Reset |
|-------|----------|--------------------------------------------------------------|-----------|-------|
| 31:16 | Reserved |                                                              | R         | 0     |
| 15:0  | IC[15:0] | Selects interrupt flag on pin x to be cleared (x = 0 to 15). | W         | 0     |

|  |  |                                                 |  |  |
|--|--|-------------------------------------------------|--|--|
|  |  | 0: No effect<br>1: Clear interrupt flag on Pn.x |  |  |
|--|--|-------------------------------------------------|--|--|

### 5.3.11 GPIO Port n Bits Set Operation register (GPIO<sub>n</sub>\_BSET) (n=0,1,2,3)

Address offset: 0x24

In order for SW to set GPIO bits without affecting any other pins in a single write operation, the GPIO bit is set if the corresponding bit in the GPIO<sub>n</sub>\_BSET register is set.

| Bit   | Name       | Description                                                                | Attribute | Reset |
|-------|------------|----------------------------------------------------------------------------|-----------|-------|
| 31:16 | Reserved   |                                                                            | R         | 0     |
| 15:0  | BSET[15:0] | Bit Set enable (x = 0 to 15)<br>0: No effect on Pn.x<br>1: Set Pn.x to "1" | W         | 0     |

### 5.3.12 GPIO Port n Bits Clear Operation register (GPIO<sub>n</sub>\_BCLR) (n=0,1,2,3)

Address offset: 0x28

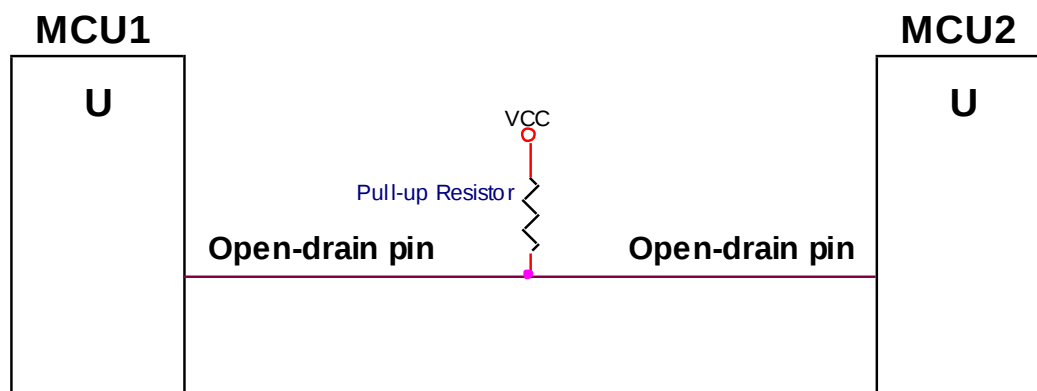
In order for SW to clear GPIO bits without affecting any other pins in a single write operation, the GPIO bit is cleared if the corresponding bit in this register is set.

| Bit   | Name       | Description                                                              | Attribute | Reset |
|-------|------------|--------------------------------------------------------------------------|-----------|-------|
| 31:16 | Reserved   |                                                                          | R         | 0     |
| 15:0  | BCLR[15:0] | Bit clear enable (x = 0 to 15)<br>0: No effect on Pn.x<br>1: Clear Pn.x. | W         | 0     |

### 5.3.13 GPIO Port n Open-Drain Control register (GPION\_ODCTRL) (n=0,1,2,3)

Address offset: 0x2C

Several I/Os have built-in open-drain function and must be set as output mode when enable open-drain function. Open-drain external circuit is as following.



The external pull-up resistor is necessary. The digital output function of I/O only supports sink current capability, so the open-drain output high is driven by pull-up resistor, and output low is sunken by MCU's pin.

- \* **Note:**
1. VCC shall be less than or equal to VDD of MCU1 and MCU2.
  2. Only P0, P1, and P3 support Open-drain.

| Bit   | Name     | Description                                                                                                                                  | Attribute | Reset |
|-------|----------|----------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:16 | Reserved |                                                                                                                                              | R         | 0     |
| 15:0  | OC[15:0] | Open-drain control bit (x = 0 to 15)<br>0: Disable.<br>1: Enable open-drain function of Pn.x. HW also set Pn.x as output mode automatically. | W/R       | 0     |

# 6 PERIPHERAL FUNCTION PIN ASSIGNMENT (PFPA)

## 6.1 OVERVIEW

PFPA registers are used to provide flexible assignment of digital peripheral functions to desired external pins of different packages.

## 6.2 FEATURES

- Flexible assignment of digital peripheral functions to desired pins.
- Supported functions are USART, I2C, SSP, I2S, Capture, and PWM.

## 6.3 PIN ASSIGNMENT LIST

| Peripheral | Pin Name | PA0  | PA1   | PA2   | PA3   | PA4   | PA5   | PA6   | PA7   | PA8  | PA9   |
|------------|----------|------|-------|-------|-------|-------|-------|-------|-------|------|-------|
| UART0      | URXD0    | P0.0 | P0.4  | P1.3  | P3.0  | P3.3  | P3.5  | P3.11 | P3.14 |      |       |
|            | UTXD0    | P0.1 | P0.5  | P1.2  | P3.1  | P3.2  | P3.4  | P3.10 | P3.15 |      |       |
| UART1      | URXD1    | P1.0 | P0.7  | P0.12 | P1.5  | P1.13 | P1.15 | P3.6  | P3.12 |      |       |
|            | UTXD1    | P1.1 | P0.6  | P0.13 | P1.4  | P1.14 | P3.8  | P3.10 | P3.13 |      |       |
| SSP0       | SCK0     | P0.4 | P0.11 | P0.13 | P1.4  | P1.12 | P3.2  | P3.6  | P3.11 | P2.3 | P2.14 |
|            | SEL0     | P0.5 | P0.10 | P0.12 | P1.5  | P1.11 | P3.1  | P3.5  | P3.10 | P2.0 | P2.15 |
|            | MISO0    | P0.2 | P0.0  | P0.6  | P0.15 | P1.0  | P1.14 | P3.3  | P3.15 | P2.1 | P2.12 |
|            | MOSI0    | P0.3 | P0.1  | P0.7  | P0.14 | P1.1  | P1.15 | P3.4  | P3.14 | P2.2 | P2.13 |
| SSP1       | SCK1     | P3.7 | P0.7  | P0.14 | P1.1  | P1.11 | P1.15 | P3.3  | P3.14 | P2.2 | P2.13 |
|            | SEL1     | P3.6 | P0.2  | P0.13 | P1.0  | P1.4  | P1.7  | P1.14 | P3.11 | P2.1 | P2.14 |
|            | MISO1    | P3.9 | P0.4  | P0.10 | P1.3  | P1.10 | P3.0  | P3.4  | P3.12 | P2.1 | P2.12 |
|            | MOSI1    | P3.8 | P0.5  | P0.12 | P1.2  | P1.6  | P1.13 | P3.2  | P3.13 | P2.0 | P2.15 |
| I2C0       | SCL0     | P1.5 | P0.2  | P0.15 | P1.3  | P1.14 | P3.9  | P3.11 | P3.14 |      |       |
|            | SDA0     | P1.4 | P0.3  | P0.10 | P1.2  | P1.13 | P3.7  | P3.13 | P3.15 |      |       |
| I2C1       | SCL1     | P0.6 | P0.0  | P1.1  | P1.9  | P3.0  | P3.3  | P3.6  | P3.13 |      |       |
|            | SDA1     | P0.7 | P0.1  | P1.0  | P1.8  | P3.2  | P3.4  | P3.5  | P3.12 |      |       |
| I2S        | MCLK     | P3.2 | P0.12 | P1.8  | P3.7  | P2.2  | P2.6  |       |       |      |       |
|            | BCLK     | P3.3 | P0.13 | P1.9  | P3.6  | P2.10 | P2.11 |       |       |      |       |
|            | WS       | P3.4 | P0.14 | P1.10 | P2.1  | P2.7  | P2.9  |       |       |      |       |
|            | DOUT     | P3.1 | P0.11 | P1.7  | P3.8  | P2.8  | P2.12 |       |       |      |       |
|            | DIN      | P3.0 | P0.10 | P1.6  | P3.9  | P2.0  | P2.5  |       |       |      |       |
| CT16B0     | CAP0     | P0.2 | P0.8  | P1.0  | P3.0  | P3.2  | P3.10 | P2.0  | P2.13 |      |       |
|            | PWM0     | P0.0 | P1.1  | P1.8  | P1.12 | P3.3  | P3.11 | P2.3  | P2.15 |      |       |
|            | PWM1     | P0.1 | P0.4  | P0.10 | P1.13 | P3.4  | P3.12 | P2.2  | P2.11 |      |       |

|        |      |       |      |       |       |       |       |       |       |  |  |
|--------|------|-------|------|-------|-------|-------|-------|-------|-------|--|--|
|        | PWM2 | P1.12 | P0.9 | P0.11 | P1.6  | P3.6  | P3.15 | P2.4  | P2.10 |  |  |
| CT16B1 | CAP0 | P0.12 | P0.7 | P1.7  | P1.11 | P3.5  | P3.13 | P2.1  | P2.9  |  |  |
|        | PWM0 | P0.10 | P0.5 | P1.9  | P1.15 | P3.7  | P3.14 | P2.0  | P2.12 |  |  |
|        | PWM1 | P0.11 | P0.8 | P0.12 | P1.3  | P1.10 | P3.9  | P2.4  | P2.8  |  |  |
|        | PWM2 | P1.9  | P0.6 | P0.15 | P1.2  | P1.14 | P3.8  | P2.3  | P2.7  |  |  |
| CT16B2 | CAP0 | P1.8  | P0.3 | P0.13 | P1.5  | P3.6  | P3.12 | P2.2  | P2.14 |  |  |
|        | PWM0 | P3.5  | P0.2 | P0.14 | P1.4  | P3.1  | P3.10 | P2.5  | P2.9  |  |  |
|        | PWM1 | P1.4  | P0.0 | P0.9  | P1.11 | P3.5  | P3.15 | P2.1  | P2.6  |  |  |
|        | PWM2 | P3.1  | P0.1 | P1.0  | P1.12 | P3.0  | P3.11 | P2.4  | P2.10 |  |  |
| CT32B0 | CAP0 | P3.9  | P0.0 | P0.9  | P1.1  | P3.1  | P3.3  | P2.3  | P2.15 |  |  |
|        | PWM0 | P1.15 | P0.4 | P0.11 | P1.8  | P1.14 | P3.9  | P2.3  | P2.14 |  |  |
|        | PWM1 | P3.8  | P0.8 | P0.14 | P1.5  | P1.11 | P3.14 | P2.4  | P2.13 |  |  |
|        | PWM2 | P1.14 | P0.5 | P0.9  | P1.9  | P3.7  | P3.13 | P2.0  | P2.11 |  |  |
|        | PWM3 | P1.2  | P0.3 | P0.7  | P0.15 | P1.12 | P3.4  | P2.2  | P2.12 |  |  |
| CT32B1 | CAP0 | P1.3  | P0.2 | P0.8  | P0.15 | P1.6  | P3.8  | P2.4  | P2.10 |  |  |
|        | PWM0 | P1.13 | P0.1 | P0.9  | P1.3  | P3.2  | P3.15 | P2.6  | P2.15 |  |  |
|        | PWM1 | P0.15 | P0.4 | P1.2  | P1.10 | P3.5  | P3.10 | P2.1  | P2.8  |  |  |
|        | PWM2 | P1.6  | P0.5 | P0.8  | P0.11 | P3.12 | P2.5  | P2.12 | P2.14 |  |  |
|        | PWM3 | P1.7  | P0.6 | P0.7  | P1.2  | P3.9  | P3.11 | P2.4  | P2.13 |  |  |
| CT32B2 | CAP0 | P3.7  | P0.9 | P0.10 | P1.4  | P1.13 | P3.14 | P2.5  | P2.12 |  |  |
|        | PWM0 | P0.13 | P0.3 | P0.8  | P1.1  | P1.7  | P1.15 | P2.11 | P2.15 |  |  |
|        | PWM1 | P0.14 | P0.2 | P0.15 | P1.5  | P3.0  | P3.7  | P2.7  | P2.13 |  |  |
|        | PWM2 | P0.3  | P0.0 | P0.9  | P1.6  | P3.1  | P3.13 | P3.15 | P2.14 |  |  |
|        | PWM3 | P0.6  | P1.0 | P1.7  | P3.10 | P2.3  | P2.8  | P2.9  | P2.15 |  |  |

## 6.4 PFPA REGISTERS

Base Address: 0x4004 2000

### 6.4.1 PFPA for UART register (PFPA\_UART)

Address offset: 0x00

| Bit   | Name       | Description                                                                                                                                                         | Attribute | Reset |
|-------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:16 | Reserved   |                                                                                                                                                                     | R         | 0     |
| 15:12 | URXD1[3:0] | Pin to be assigned as URXD1.<br>0000: P1.0<br>0001: P0.7<br>0010: P0.12<br>0011: P1.5<br>0100: P1.13<br>0101: P1.15<br>0110: P3.6<br>0111: P3.12<br>Other: Reserved | R/W       | 0000b |

|             |                   |                                                                                                                                                                     |     |       |
|-------------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|
| <b>11:8</b> | <b>UTXD1[3:0]</b> | Pin to be assigned as UTXD1.<br>0000: P1.1<br>0001: P0.6<br>0010: P0.13<br>0011: P1.4<br>0100: P1.14<br>0101: P3.8<br>0110: P3.10<br>0111: P3.13<br>Other: Reserved | R/W | 0000b |
| <b>7:4</b>  | <b>URXD0[3:0]</b> | Pin to be assigned as URXD0.<br>0000: P0.0<br>0001: P0.4<br>0010: P1.3<br>0011: P3.0<br>0100: P3.3<br>0101: P3.5<br>0110: P3.11<br>0111: P3.14<br>Other: Reserved   | R/W | 0000b |
| <b>3:0</b>  | <b>UTXD0[3:0]</b> | Pin to be assigned as UTXD0.<br>0000: P0.1<br>0001: P0.5<br>0010: P1.2<br>0011: P3.1<br>0100: P3.2<br>0101: P3.4<br>0110: P3.10<br>0111: P3.15<br>Other: Reserved   | R/W | 0000b |

## 6.4.2 PFPA for I2C register (PFPA\_I2C)

Address offset: 0x04

| Bit          | Name             | Description                                                                                                                                                     | Attribute | Reset |
|--------------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:16</b> | Reserved         |                                                                                                                                                                 | R         | 0     |
| <b>15:12</b> | <b>SCL1[3:0]</b> | Pin to be assigned as SCL1.<br>0000: P0.6<br>0001: P0.0<br>0010: P1.1<br>0011: P1.9<br>0100: P3.0<br>0101: P3.3<br>0110: P3.6<br>0111: P3.13<br>Other: Reserved | R/W       | 0000b |
| <b>11:8</b>  | <b>SDA1[3:0]</b> | Pin to be assigned as SDA1.<br>0000: P0.7<br>0001: P0.1<br>0010: P1.0<br>0011: P1.8<br>0100: P3.2<br>0101: P3.4<br>0110: P3.5<br>0111: P3.12<br>Other: Reserved | R/W       | 0000b |
| <b>7:4</b>   | <b>SCL0[3:0]</b> | Pin to be assigned as SCL0.<br>0000: P1.5<br>0001: P0.2<br>0010: P0.15<br>0011: P1.3<br>0100: P1.14<br>0101: P3.9<br>0110: P3.11<br>0111: P3.14                 | R/W       | 0000b |

|            |           |                                                                                                                                                                    |     |       |
|------------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|
|            |           | Other: Reserved                                                                                                                                                    |     |       |
| <b>3:0</b> | SDA0[3:0] | Pin to be assigned as SDA0.<br>0000: P1.4<br>0001: P0.3<br>0010: P0.10<br>0011: P1.2<br>0100: P1.13<br>0101: P3.7<br>0110: P3.13<br>0111: P3.15<br>Other: Reserved | R/W | 0000b |

### 6.4.3 PFPA for SSP register (PFPA\_SSP)

Address offset: 0x08

| Bit          | Name       | Description                                                                                                                                                                                     | Attribute | Reset |
|--------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:28</b> | SEL1[3:0]  | Pin to be assigned as SEL1.<br>0000: P3.6<br>0001: P0.2<br>0010: P0.13<br>0011: P1.0<br>0100: P1.4<br>0101: P1.7<br>0110: P1.14<br>0111: P3.11<br>1000: P2.1<br>1001: P2.14<br>Other: Reserved  | R/W       | 0000b |
| <b>27:24</b> | SCK1[3:0]  | Pin to be assigned as SCK1.<br>0000: P3.7<br>0001: P0.7<br>0010: P0.14<br>0011: P1.1<br>0100: P1.11<br>0101: P1.15<br>0110: P3.3<br>0111: P3.14<br>1000: P2.2<br>1001: P2.13<br>Other: Reserved | R/W       | 0000b |
| <b>23:20</b> | MOSI1[3:0] | Pin to be assigned as MOSI1.<br>0000: P3.8<br>0001: P0.5<br>0010: P0.12<br>0011: P1.2<br>0100: P1.6<br>0101: P1.13<br>0110: P3.2<br>0111: P3.13<br>1000: P2.0<br>1001: P2.15<br>Other: Reserved | R/W       | 0000b |
| <b>19:16</b> | MISO1[3:0] | Pin to be assigned as MISO1.<br>0000: P3.9<br>0001: P0.4<br>0010: P0.10<br>0011: P1.3<br>0100: P1.10<br>0101: P3.0<br>0110: P3.4<br>0111: P3.12<br>1000: P2.1<br>1001: P2.12<br>Other: Reserved | R/W       | 0000b |
| <b>15:12</b> | SEL0[3:0]  | Pin to be assigned as SEL0.<br>0000: P0.5                                                                                                                                                       | R/W       | 0000b |

|             |                   |                                                                                                                                                                                                 |     |       |
|-------------|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|
|             |                   | 0001: P0.10<br>0010: P0.12<br>0011: P1.5<br>0100: P1.11<br>0101: P3.1<br>0110: P3.5<br>0111: P3.10<br>1000: P2.0<br>1001: P2.15<br>Other: Reserved                                              |     |       |
| <b>11:8</b> | <b>SCK0[3:0]</b>  | Pin to be assigned as SCK0.<br>0000: P0.4<br>0001: P0.11<br>0010: P0.13<br>0011: P1.4<br>0100: P1.12<br>0101: P3.2<br>0110: P3.6<br>0111: P3.11<br>1000: P2.3<br>1001: P2.14<br>Other: Reserved | R/W | 0000b |
| <b>7:4</b>  | <b>MOSI0[3:0]</b> | Pin to be assigned as MOSI0.<br>0000: P0.3<br>0001: P0.1<br>0010: P0.7<br>0011: P0.14<br>0100: P1.1<br>0101: P1.15<br>0110: P3.4<br>0111: P3.14<br>1000: P2.2<br>1001: P2.13<br>Other: Reserved | R/W | 0000b |
| <b>3:0</b>  | <b>MISO0[3:0]</b> | Pin to be assigned as MISO0.<br>0000: P0.2<br>0001: P0.0<br>0010: P0.6<br>0011: P0.15<br>0100: P1.0<br>0101: P1.14<br>0110: P3.3<br>0111: P3.15<br>1000: P2.1<br>1001: P2.12<br>Other: Reserved | R/W | 0000b |

#### 6.4.4 PFPA for I2S register (PFPA\_I2S)

Address offset: 0x0C

| Bit          | Name             | Description                                                                                                                           | Attribute | Reset |
|--------------|------------------|---------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:20</b> | Reserved         |                                                                                                                                       | R         | 0     |
| <b>19:16</b> | <b>DIN[3:0]</b>  | Pin to be assigned as I2SDIN.<br>0000: P3.0<br>0001: P0.10<br>0010: P1.6<br>0011: P3.9<br>0100: P2.0<br>0101: P2.5<br>Other: Reserved | R/W       | 0000b |
| <b>15:12</b> | <b>DOUT[3:0]</b> | Pin to be assigned as I2SDOUT.<br>0000: P3.1<br>0001: P0.11<br>0010: P1.7<br>0011: P3.8                                               | R/W       | 0000b |

|             |                  |                                                                                                                                          |     |       |
|-------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|
|             |                  | 0100: P2.8<br>0101: P2.12<br>Other: Reserved                                                                                             |     |       |
| <b>11:8</b> | <b>WS[3:0]</b>   | Pin to be assigned as I2SWS.<br>0000: P3.4<br>0001: P0.14<br>0010: P1.10<br>0011: P2.1<br>0100: P2.7<br>0101: P2.9<br>Other: Reserved    | R/W | 0000b |
| <b>7:4</b>  | <b>BCLK[3:0]</b> | Pin to be assigned as I2SBCLK.<br>0000: P3.3<br>0001: P0.13<br>0010: P1.9<br>0011: P3.6<br>0100: P2.10<br>0101: P2.11<br>Other: Reserved | R/W | 0000b |
| <b>3:0</b>  | <b>MCLK[3:0]</b> | Pin to be assigned as I2SMCLK.<br>0000: P3.2<br>0001: P0.12<br>0010: P1.8<br>0011: P3.7<br>0100: P2.2<br>0101: P2.6<br>Other: Reserved   | R/W | 0000b |

### 6.4.5 PFPA for CT16B0 register (PFPA\_CT16B0)

Address offset: 0x10

| Bit          | Name             | Description                                                                                                                                                               | Attribute | Reset |
|--------------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:16</b> | Reserved         |                                                                                                                                                                           | R         | 0     |
| <b>15:12</b> | <b>PWM2[3:0]</b> | Pin to be assigned as CT16B0_PWM2.<br>0000: P1.12<br>0001: P0.9<br>0010: P0.11<br>0011: P1.6<br>0100: P3.6<br>0101: P3.15<br>0110: P2.4<br>0111: P2.10<br>Other: Reserved | R/W       | 0000b |
| <b>11:8</b>  | <b>PWM1[3:0]</b> | Pin to be assigned as CT16B0_PWM1.<br>0000: P0.1<br>0001: P0.4<br>0010: P0.10<br>0011: P1.13<br>0100: P3.4<br>0101: P3.12<br>0110: P2.2<br>0111: P2.11<br>Other: Reserved | R/W       | 0000b |
| <b>7:4</b>   | <b>PWM0[3:0]</b> | Pin to be assigned as CT16B0_PWM0.<br>0000: P0.0<br>0001: P1.1<br>0010: P1.8<br>0011: P1.12<br>0100: P3.3<br>0101: P3.11<br>0110: P2.3<br>0111: P2.15<br>Other: Reserved  | R/W       | 0000b |

|            |                  |                                                                                                                                                                         |     |       |
|------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|
| <b>3:0</b> | <b>CAP0[3:0]</b> | Pin to be assigned as CT16B0_CAP0.<br>0000: P0.2<br>0001: P0.8<br>0010: P1.0<br>0011: P3.0<br>0100: P3.2<br>0101: P3.10<br>0110: P2.0<br>0111: P2.13<br>Other: Reserved | R/W | 0000b |
|------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|

### 6.4.6 PFPA for CT16B1 register (PFPA\_CT16B1)

Address offset: 0x14

| Bit          | Name             | Description                                                                                                                                                               | Attribute | Reset |
|--------------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:16</b> | Reserved         |                                                                                                                                                                           | R         | 0     |
| <b>15:12</b> | <b>PWM2[3:0]</b> | Pin to be assigned as CT16B1_PWM2.<br>0000: P1.9<br>0001: P0.6<br>0010: P0.15<br>0011: P1.2<br>0100: P1.14<br>0101: P3.8<br>0110: P2.3<br>0111: P2.7<br>Other: Reserved   | R/W       | 0000b |
| <b>11:8</b>  | <b>PWM1[3:0]</b> | Pin to be assigned as CT16B1_PWM1.<br>0000: P0.11<br>0001: P0.8<br>0010: P0.12<br>0011: P1.3<br>0100: P1.10<br>0101: P3.9<br>0110: P2.4<br>0111: P2.8<br>Other: Reserved  | R/W       | 0000b |
| <b>7:4</b>   | <b>PWM0[3:0]</b> | Pin to be assigned as CT16B1_PWM0.<br>0000: P0.10<br>0001: P0.5<br>0010: P1.9<br>0011: P1.15<br>0100: P3.7<br>0101: P3.14<br>0110: P2.0<br>0111: P2.12<br>Other: Reserved | R/W       | 0000b |
| <b>3:0</b>   | <b>CAP0[3:0]</b> | Pin to be assigned as CT16B1_CAP0.<br>0000: P0.12<br>0001: P0.7<br>0010: P1.7<br>0011: P1.11<br>0100: P3.5<br>0101: P3.13<br>0110: P2.1<br>0111: P2.9<br>Other: Reserved  | R/W       | 0000b |

### 6.4.7 PFPA for CT16B2 register (PFPA\_CT16B2)

Address offset: 0x18

| Bit   | Name      | Description                                                                                                                                                              | Attribute | Reset |
|-------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:16 | Reserved  |                                                                                                                                                                          | R         | 0     |
| 15:12 | PWM2[3:0] | Pin to be assigned as CT16B2_PWM2.<br>0000: P3.1<br>0001: P0.1<br>0010: P1.0<br>0011: P1.12<br>0100: P3.0<br>0101: P3.11<br>0110: P2.4<br>0111: P2.10<br>Other: Reserved | R/W       | 0000b |
| 11:8  | PWM1[3:0] | Pin to be assigned as CT16B2_PWM1.<br>0000: P1.4<br>0001: P0.0<br>0010: P0.9<br>0011: P1.11<br>0100: P3.5<br>0101: P3.15<br>0110: P2.1<br>0111: P2.6<br>Other: Reserved  | R/W       | 0000b |
| 7:4   | PWM0[3:0] | Pin to be assigned as CT16B2_PWM0.<br>0000: P3.5<br>0001: P0.2<br>0010: P0.14<br>0011: P1.4<br>0100: P3.1<br>0101: P3.10<br>0110: P2.5<br>0111: P2.9<br>Other: Reserved  | R/W       | 0000b |
| 3:0   | CAP0[3:0] | Pin to be assigned as CT16B2_CAP0.<br>0000: P1.8<br>0001: P0.3<br>0010: P0.13<br>0011: P1.5<br>0100: P3.6<br>0101: P3.12<br>0110: P2.2<br>0111: P2.14<br>Other: Reserved | R/W       | 0000b |

### 6.4.8 PFPA for CT32B0 register (PFPA\_CT32B0)

Address offset: 0x20

| Bit   | Name      | Description                                                                                                                                                              | Attribute | Reset |
|-------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:20 | Reserved  |                                                                                                                                                                          | R         | 0     |
| 19:16 | PWM3[3:0] | Pin to be assigned as CT32B0_PWM3.<br>0000: P1.2<br>0001: P0.3<br>0010: P0.7<br>0011: P0.15<br>0100: P1.12<br>0101: P3.4<br>0110: P2.2<br>0111: P2.12<br>Other: Reserved | R/W       | 0000b |

|              |                  |                                                                                                                                                                           |     |       |
|--------------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|
| <b>15:12</b> | <b>PWM2[3:0]</b> | Pin to be assigned as CT32B0_PWM2.<br>0000: P1.14<br>0001: P0.5<br>0010: P0.9<br>0011: P1.9<br>0100: P3.7<br>0101: P3.13<br>0110: P2.0<br>0111: P2.11<br>Other: Reserved  | R/W | 0000b |
| <b>11:8</b>  | <b>PWM1[3:0]</b> | Pin to be assigned as CT32B0_PWM1.<br>0000: P3.8<br>0001: P0.8<br>0010: P0.14<br>0011: P1.5<br>0100: P1.11<br>0101: P3.14<br>0110: P2.4<br>0111: P2.13<br>Other: Reserved | R/W | 0000b |
| <b>7:4</b>   | <b>PWM0[3:0]</b> | Pin to be assigned as CT32B0_PWM0.<br>0000: P1.15<br>0001: P0.4<br>0010: P0.11<br>0011: P1.8<br>0100: P1.14<br>0101: P3.9<br>0110: P2.3<br>0111: P2.14<br>Other: Reserved | R/W | 0000b |
| <b>3:0</b>   | <b>CAP0[3:0]</b> | Pin to be assigned as CT32B0_CAP0.<br>0000: P3.9<br>0001: P0.0<br>0010: P0.9<br>0011: P1.1<br>0100: P3.1<br>0101: P3.3<br>0110: P2.3<br>0111: P2.15<br>Other: Reserved    | R/W | 0000b |

### 6.4.9 PFPA for CT32B1 register (PFPA\_CT32B1)

Address offset: 0x24

| Bit          | Name             | Description                                                                                                                                                             | Attribute | Reset |
|--------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:20</b> | Reserved         |                                                                                                                                                                         | R         | 0     |
| <b>19:16</b> | <b>PWM3[3:0]</b> | Pin to be assigned as CT32B1_PWM3.<br>0000: P1.7<br>0001: P0.6<br>0010: P0.7<br>0011: P1.2<br>0100: P3.9<br>0101: P3.11<br>0110: P2.4<br>0111: P2.13<br>Other: Reserved | R/W       | 0000b |
| <b>15:12</b> | <b>PWM2[3:0]</b> | Pin to be assigned as CT32B1_PWM2.<br>0000: P1.6<br>0001: P0.5<br>0010: P0.8<br>0011: P0.11<br>0100: P3.12<br>0101: P2.5<br>0110: P2.12<br>0111: P2.14                  | R/W       | 0000b |

|             |           |                                                                                                                                                                          |     |       |
|-------------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|
|             |           | Other: Reserved                                                                                                                                                          |     |       |
| <b>11:8</b> | PWM1[3:0] | Pin to be assigned as CT32B1_PWM1.<br>0000: P0.15<br>0001: P0.4<br>0010: P1.2<br>0011: P1.10<br>0100: P3.5<br>0101: P3.10<br>0110: P2.1<br>0111: P2.8<br>Other: Reserved | R/W | 0000b |
| <b>7:4</b>  | PWM0[3:0] | Pin to be assigned as CT32B1_PWM0.<br>0000: P1.13<br>0001: P0.1<br>0010: P0.9<br>0011: P1.3<br>0100: P3.2<br>0101: P3.15<br>0110: P2.6<br>0111: P2.15<br>Other: Reserved | R/W | 0000b |
| <b>3:0</b>  | CAP0[3:0] | Pin to be assigned as CT32B1_CAP0.<br>0000: P1.3<br>0001: P0.2<br>0010: P0.8<br>0011: P0.15<br>0100: P1.6<br>0101: P3.8<br>0110: P2.4<br>0111: P2.10<br>Other: Reserved  | R/W | 0000b |

### 6.4.10 PFPA for CT32B2 register (PFPA\_CT32B2)

Address offset: 0x28

| Bit          | Name      | Description                                                                                                                                                              | Attribute | Reset |
|--------------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:20</b> | Reserved  |                                                                                                                                                                          | R         | 0     |
| <b>19:16</b> | PWM3[3:0] | Pin to be assigned as CT32B2_PWM3.<br>0000: P0.6<br>0001: P1.0<br>0010: P1.7<br>0011: P3.10<br>0100: P2.3<br>0101: P2.8<br>0110: P2.9<br>0111: P2.15<br>Other: Reserved  | R/W       | 0000b |
| <b>15:12</b> | PWM2[3:0] | Pin to be assigned as CT32B2_PWM2.<br>0000: P0.3<br>0001: P0.0<br>0010: P0.9<br>0011: P1.6<br>0100: P3.1<br>0101: P3.13<br>0110: P3.15<br>0111: P2.14<br>Other: Reserved | R/W       | 0000b |
| <b>11:8</b>  | PWM1[3:0] | Pin to be assigned as CT32B2_PWM1.<br>0000: P0.14<br>0001: P0.2<br>0010: P0.15<br>0011: P1.5<br>0100: P3.0<br>0101: P3.7                                                 | R/W       | 0000b |

|            |           |                                                                                                                                                                           |     |       |
|------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|
|            |           | 0110: P2.7<br>0111: P2.13<br>Other: Reserved                                                                                                                              |     |       |
| <b>7:4</b> | PWM0[3:0] | Pin to be assigned as CT32B2_PWM0.<br>0000: P0.13<br>0001: P0.3<br>0010: P0.8<br>0011: P1.1<br>0100: P1.7<br>0101: P1.15<br>0110: P2.11<br>0111: P2.15<br>Other: Reserved | R/W | 0000b |
| <b>3:0</b> | CAP0[3:0] | Pin to be assigned as CT32B2_CAP0.<br>0000: P3.7<br>0001: P0.9<br>0010: P0.10<br>0011: P1.4<br>0100: P1.13<br>0101: P3.14<br>0110: P2.5<br>0111: P2.12<br>Other: Reserved | R/W | 0000b |

# 7 14+1 CHANNEL ANALOG TO DIGITAL CONVERTOR (ADC)

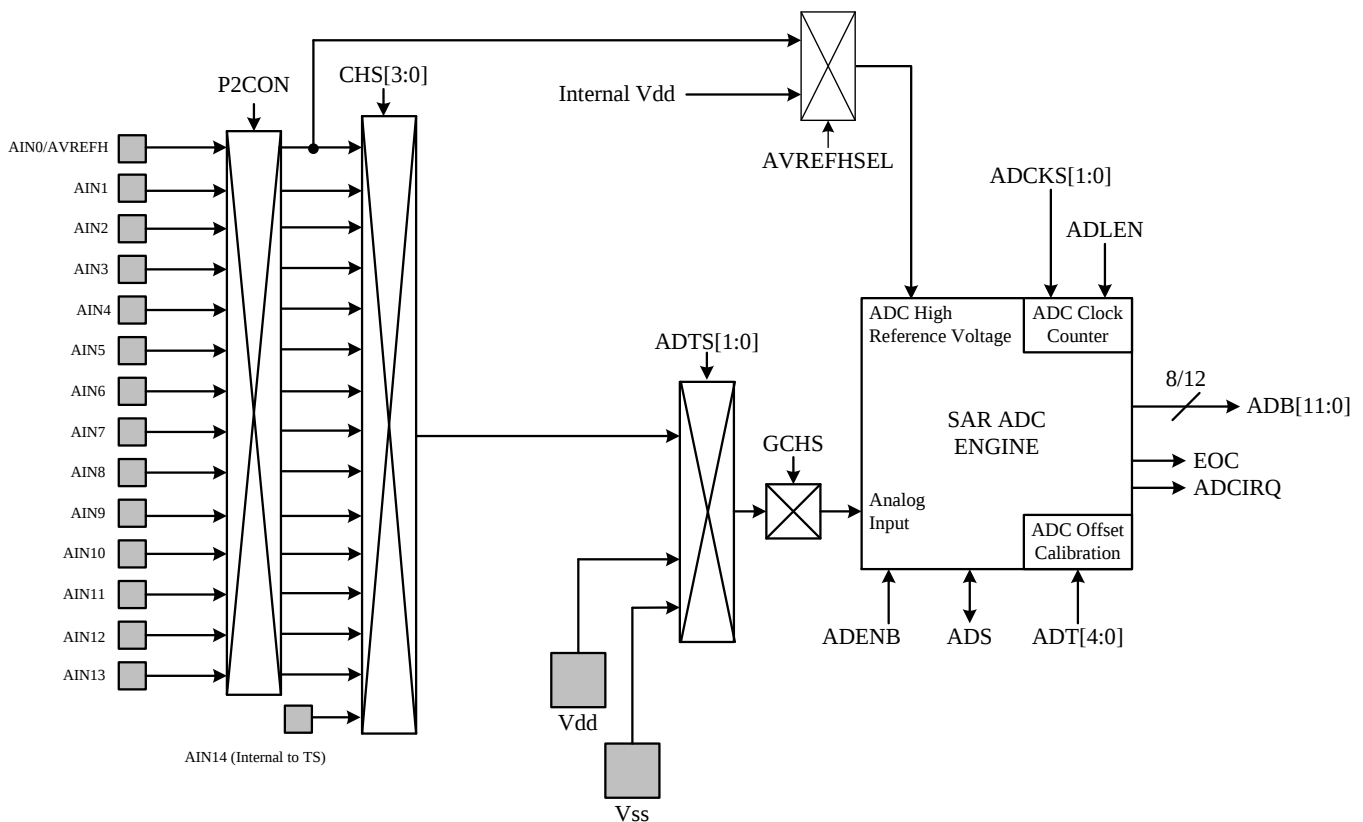
## 7.1 OVERVIEW

This analog to digital converter has 14 external channels and 1 internal channel to Temperature sensor, with up to 4096-step resolution to transfer analog signal into 12-bits digital data. The sequence of ADC operation is to select input source (AIN0 ~ AIN13) at first, then set GCHS and ADS bit to "1" to start conversion. When the conversion is complete, the ADC circuit will set EOC bit to "1" and final value output in ADB register.

Use CHS[3:0] to select AIN pin and GCHS enables global ADC channel, the analog signal inputs to ADC engine.

The ADC reference high voltage includes two source, one is internal Vdd (AVREFHSEL=0), and the other one is external reference voltage input pin from P2.0 pin (AVREFHSEL=1).

The ADC resolution can be selected 8-bit or 12-bit through ADLEN bit in ADR register. The ADC converting rate can be selected by ADCKS[1:0] bits. The two parameters decide ADC converting time.



**\* Note:**

1. For 8-bit resolution the conversion time is 12 steps. For 12-bit resolution the conversion time is 16 steps

2. **ADC\_PCLK shall be less than 16MHz.**
3. **The analog input level must be between the AVREFH and AVREFL.**
4. **The AVREFH level must be between the AVDD and AVREFL + 2.0V.**
5. **ADC programming notice**
  - **Disable ADC (set ADENB = "0") before enter low-power (Sleep/Deep-sleep) mode to save power consumption.**
  - **Delay 100us after enable ADC (set ADENB = "1") to wait ADC circuit ready for conversion.**

## 7.2 ADC CONVERTING TIME

The ADC converting time is from ADS=1 (Start to ADC convert) to EOC=1 (End of ADC convert). The converting time duration is depend on ADC resolution and ADC clock rate.

ADC clock source is controlled by ADCKS[2:0] bits. The ADC converting time affects ADC performance. If input high rate analog signal, it is necessary to select a high ADC converting rate. If the ADC converting time is slower than analog signal variation rate, the ADC result would be error. So to select a correct ADC clock rate and ADC resolution to decide a right ADC converting rate is very important.

**12-bit ADC conversion time = 1/(ADC clock /4)\*16 sec**

| ADLEN | ADCKS [2:0] | ADC Clock   | ADC_PCLK = 4 MHz         |                           | ADC_PCLK = 12 MHz        |                           | ADC_PCLK = 16 MHz        |                           |
|-------|-------------|-------------|--------------------------|---------------------------|--------------------------|---------------------------|--------------------------|---------------------------|
|       |             |             | ADC Conversion Time (us) | ADC Conversion Rate (KHz) | ADC Conversion Time (us) | ADC Conversion Rate (KHz) | ADC Conversion Time (us) | ADC Conversion Rate (KHz) |
| 1     | 000         | ADC_PCLK    | 16                       | 62.5                      | 5.33                     | 187.5                     | 4                        | 250                       |
|       | 001         | ADC_PCLK/2  | 32                       | 31.25                     | 10.67                    | 93.75                     | 8                        | 125                       |
|       | 010         | ADC_PCLK/4  | 64                       | 15.625                    | 21.33                    | 46.875                    | 16                       | 62.5                      |
|       | 011         | ADC_PCLK/8  | 128                      | 7.813                     | 42.67                    | 23.437                    | 32                       | 31.25                     |
|       | 100         | ADC_PCLK/16 | 256                      | 3.906                     | 85.3                     | 11.718                    | 64                       | 15.625                    |
|       | 101         | ADC_PCLK/32 | 512                      | 1.953                     | 170.67                   | 5.859                     | 128                      | 7.813                     |

**8-bit ADC conversion time = 1/(ADC clock /4)\*12 sec**

| ADLEN | ADCKS [2:0] | ADC Clock   | ADC_PCLK = 4 MHz         |                           | ADC_PCLK = 12 MHz        |                           | ADC_PCLK = 16 MHz        |                           |
|-------|-------------|-------------|--------------------------|---------------------------|--------------------------|---------------------------|--------------------------|---------------------------|
|       |             |             | ADC Conversion Time (us) | ADC Conversion Rate (KHz) | ADC Conversion Time (us) | ADC Conversion Rate (KHz) | ADC Conversion Time (us) | ADC Conversion Rate (KHz) |
| 0     | 000         | ADC_PCLK    | 12                       | 83.333                    | 4                        | 250                       | 3                        | 333.333                   |
|       | 001         | ADC_PCLK/2  | 24                       | 41.667                    | 8                        | 125                       | 6                        | 166.667                   |
|       | 010         | ADC_PCLK/4  | 48                       | 20.83                     | 16                       | 62.5                      | 12                       | 83.333                    |
|       | 011         | ADC_PCLK/8  | 96                       | 10.416                    | 32                       | 31.25                     | 24                       | 41.667                    |
|       | 100         | ADC_PCLK/16 | 192                      | 5.208                     | 64                       | 15.625                    | 48                       | 20.83                     |
|       | 101         | ADC_PCLK/32 | 384                      | 2.604                     | 128                      | 7.813                     | 96                       | 10.416                    |

## 7.3 ADC CONTROL NOTICE

### 7.3.1 ADC SIGNAL

The ADC high reference voltage is internal Vdd or external voltage source. The ADC low reference voltage is ground. The ADC input signal voltage range must be from high reference voltage to low reference voltage.

**The external high reference voltage from P2.0 must be higher than “Low reference voltage + 2V”. The low reference voltage is ground. So the external reference voltage range must be under 2V~Vdd.**

### 7.3.2 ADC PROGRAM

The first step of ADC execution is to setup ADC configuration. The ADC program setup sequence and notices are as following.

- **Step 1:** Enable ADC. ADENB is ADC control bit to control. ADENB = 1 is to enable ADC. ADENB = 0 is to disable ADC. **When ADENB is enabled, the system must be delay 100us to be the ADC warm-up time by program, and then set ADS to do ADC converting. The 100us delay time is necessary after ADENB setting (not ADS setting), or the ADC converting result would be error.** Normally, the ADENB is set one time when the system under normal run condition, and do the delay time only one time.
- **Step 2:** If the ADC high reference voltage is from external voltage source, set the AVREFHSEL = 1. The ADC external high reference voltage inputs from P2.0 pin. **It is necessary to set P2.0 as input mode without pull-up resistor.**
- **Step 3:** Select the ADC input pin by CHS[3:0], and enable ADC global input. **When one AIN pin is selected to be analog signal input pin, it is necessary to setup the pin as input mode and disable the pull-up resistor by program.** **Step 4:** Start to execute ADC conversion by setting ADS = 1.
- **Step 5:** Wait the end of ADC converting through checking EOC = 1 or ADCIF = 1. If ADC interrupt function is enabled, the program executes ADC interrupt service when ADC interrupt occurrence. **ADS is cleared when the end of ADC converting automatically. EOC bit indicates ADC processing status immediately and is cleared when ADS = 1. Users needn't to clear it by program.**

### 7.3.3 ADC PIN CONFIGURATION

ADC input pins are shared with Port 2 digital I/O pins. ADC channel selection is through CHS[3:0] bits in [ADC ADM](#) register. CHS[3:0] value points to the ADC input channel directly, CHS[3:0]=0000b selects AIN0, CHS[3:0]=0001b selects AIN1, etc.

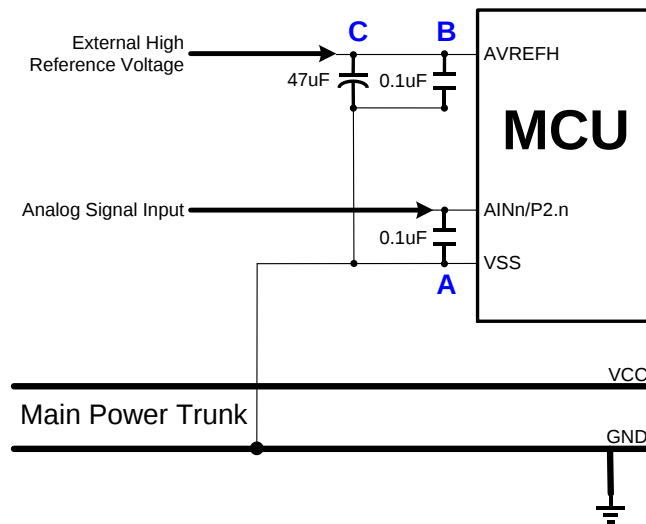
Connect an analog signal to COMS digital input pin, especially, the analog signal level is about 1/2 VDD will cause extra current leakage. In the power down mode, the above leakage current will be a big problem. Unfortunately, if users connect more than one analog input signal to Port 2 will encounter above current leakage situation.

The P2.0/AIN0 can be ADC external high reference voltage input pin when AVREFHSEL =1. In the condition, P2.0 GPIO mode must be set as input mode and inactive (no pull-down/up resistor enabled, Schmitt trigger disabled) with [GPIO2\\_MODE](#) and [GPIO2\\_CFG](#) register by program.

Only one pin of Port 2 can be configured as ADC input in the same time. The pins of Port 2 configured as ADC input channel must be set as input mode, inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low) with [GPIO2\\_MODE](#) and [GPIO2\\_CFG](#) register by program to avoid current leakage.

**\* Note: The GPIO mode of ADC input channels used must be set as input mode and inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low) with GPIO2\_MODE and GPIO2\_CFG register by program.**

## 7.4 ADC CIRCUIT



The analog signal is inputted to ADC input pin "AINn/P2.n". The ADC input signal must be through a 0.1uF capacitor "A". The 0.1uF capacitor is set between ADC input pin and VSS pin, and must be on the side of the ADC input pin as possible. Don't connect the capacitor's ground pin to ground plain directly, and must be through VSS pin. The capacitor can reduce the power noise effective coupled with the analog signal.

If the ADC high reference voltage is from external voltage source, the external high reference is connected to AVREFH pin (P2.0). The external high reference source must be through a 47uF "C" capacitor first, and then 0.1uF capacitor "B". These capacitors are set between AVREFH pin and VSS pin, and must be on the side of the AVREFH pin as possible. Don't connect the capacitor's ground pin to ground plain directly, and must be through VSS pin.

## 7.5 TEMPERATURE SENSOR (TS)

In applications, sensor characteristic might change in different temperature also. To get the temperature information, a temperature sensor (TS) is built-in for temperature measurement, and is internally connected to the AIN14 input channel which is used to convert the sensor output voltage into a digital value.

If TSENB = 1, the temperature sensor is enabled. When not in use, this sensor can be put in power down mode if TSENB = 0.

**\* Note: The Temperature Sensor was just a reference data not real air temperature. For precision application, please use external thermistor sensor.**

In 25°C, V(TS) will be about 1V typically, and if the temperature rises 10°C, V(TS) will increase about 35mV ( $V_{TS} = 1.035V$ ); if the temperature drops 10°C, V(TS) will decrease about 35mV ( $V_{TS} = 0.965V$ ).

Example:

| Temperature | V(TS)  | AVrefH | ADC output (12-Bit) |
|-------------|--------|--------|---------------------|
| 15°C        | 0.965  | 3.0V   | 1250                |
| 25°C        | 1.000V | 3.0V   | 1306                |
| 35°C        | 1.035V | 3.0V   | 1352                |

By ADC output of V(TS), can get temperature information and compensation the system.

**\* Note:**

- 1. The  $V(TS)$  voltage and temperature curve of each chip might different. Calibration in room temperature is necessary when temperature sensor is used.*
- 2.  $3.53mV/^{\circ}C$  is only the typical temperature parameter, every single chip is different to each other.*

## 7.6 ADC REGISTERS

Base Address: 0x4002 6000

### 7.6.1 ADC Management register (ADC\_ADM)

Address Offset: 0x00

**\* Note:**

1. When ADC is enabled (ADENB=1) and global channel is enabled (GCHS=1), the ADC shared pins transfers to ADC purpose and disable GPIO function and disable pull-up/pull-down resistor by HW automatically, the P2.n/AINn's digital I/O function including pull-up is isolated.
2. When ADC is disabled (ADENB=0) or global channel is disabled (GCHS=0), the ADC pins returns to last GPIO status.
3. If P2.0 is used as external reference voltage input pin, users should set P2.0 as input mode without pull-up.

| Bit   | Name       | Description                                                                                                                                                                                                                                                                                                         | Attribute | Reset |
|-------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:18 | Reserved   |                                                                                                                                                                                                                                                                                                                     | R         | 0     |
| 17    | TSENB      | Temperature sensor enable bit<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                            | R/W       | 0     |
| 16:13 | Reserved   |                                                                                                                                                                                                                                                                                                                     | R         | 0     |
| 12    | AVREFHSEL  | ADC high reference voltage source select bit<br>0: Internal VDD. (P2.0 is GPIO or AIN0 pin)<br>1: Enable external reference voltage from P2.0                                                                                                                                                                       | R/W       | 0     |
| 11    | ADENB      | ADC Enable bit<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                           | R/W       | 0     |
| 10:8  | ADCKS[2:0] | ADC Clock source divider<br>000: ADC_PCLK / 1<br>001: ADC_PCLK / 2<br>010: ADC_PCLK / 4<br>011: ADC_PCLK / 8<br>101: ADC_PCLK / 16<br>110: ADC_PCLK / 32<br>Other: Reversed                                                                                                                                         | R/W       | 0     |
| 7     | ADLEN      | ADC resolution control bit.<br>0: 8-bit ADC.<br>1:12-bit ADC.                                                                                                                                                                                                                                                       | R/W       | 0     |
| 6     | ADS        | ADC start control bit.<br>0: ADC converting stops.<br>1: Start to execute ADC converting. ADS is cleared when the end of ADC converting automatically.                                                                                                                                                              | R/W       | 0     |
| 5     | EOC        | ADC status bit Indicates ADC processing status immediately and is cleared when ADS = 1.<br>0: ADC progressing.<br>1: End of converting and reset ADS bit.                                                                                                                                                           | R/W       | 0     |
| 4     | GCHS       | ADC global channel select bit.<br>0: Disable AIN channel<br>1: Enable AIN channel                                                                                                                                                                                                                                   | R/W       | 0     |
| 3:0   | CHS[3:0]   | ADC input channels select bit.<br>0000: AIN0      0001: AIN1      0010: AIN2      0011: AIN3<br>0100: AIN4      0101: AIN5      0110: AIN6      0111: AIN7<br>1000: AIN8      1001: AIN9      1010: AIN10      1011: AIN11<br>1100: AIN12      1101: AIN13      1110: AIN14 (Temperature Sensor)<br>Other: Reserved | R/W       | 0     |

## 7.6.2 ADC Data register (ADC\_ADB)

Address Offset: 0x04

ADB is ADC data buffer to store AD converter result.

**\* Note: The initial value of ADC buffer (ADB) after reset is unknown.**

| Bit   | Name      | Description                                                     | Attribute | Reset |
|-------|-----------|-----------------------------------------------------------------|-----------|-------|
| 31:12 | Reserved  |                                                                 | R         | 0     |
| 11:0  | ADB[11:0] | ADB11~ADB4 bits for 8-bit ADC<br>ADB11~ADB0 bits for 12-bit ADC | R         | 0     |

The AIN's input voltage vs. ADB's output data

| AIN n           | ADB11 | ADB10 | ADB9 | ADB8 | ADB7 | ADB6 | ADB5 | ADB4 | ADB3 | ADB2 | ADB1 | ADB0 |
|-----------------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| 0/4096*VREFH    | 0     | 0     | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| 1/4096*VREFH    | 0     | 0     | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 1    |
| .               | .     | .     | .    | .    | .    | .    | .    | .    | .    | .    | .    | .    |
| .               | .     | .     | .    | .    | .    | .    | .    | .    | .    | .    | .    | .    |
| .               | .     | .     | .    | .    | .    | .    | .    | .    | .    | .    | .    | .    |
| 4094/4096*VREFH | 1     | 1     | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 0    |
| 4095/4096*VREFH | 1     | 1     | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |

For different applications, users maybe need more than 8-bit resolution but less than 12-bit ADC converter. First, the AD resolution must be set 12-bit mode and then to execute ADC converter routine. Then delete the LSB of ADC data and get the new resolution result. The table is as following.

|         | ADB11 | ADB10 | ADB9 | ADB8 | ADB7 | ADB6 | ADB5 | ADB4 | ADB3 | ADB2 | ADB1 | ADB0 |
|---------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| 8-bit   | O     | O     | O    | O    | O    | O    | O    | O    | X    | X    | X    | X    |
| 9-bit   | O     | O     | O    | O    | O    | O    | O    | O    | O    | X    | X    | X    |
| 10-bit  | O     | O     | O    | O    | O    | O    | O    | O    | O    | O    | X    | X    |
| 11-bit  | O     | O     | O    | O    | O    | O    | O    | O    | O    | O    | O    | X    |
| 12-bit. | O     | O     | O    | O    | O    | O    | O    | O    | O    | O    | O    | O    |

O = Selected, X = Delete

## 7.6.3 Port 2 Control register (ADC\_P2CON)

Address Offset: 0x08

ADC input pins are shared with Port 2 digital I/O pins. Connect an analog signal to COMS digital input pin, especially, the analog signal level is about 1/2 VDD will cause extra current leakage. In the power down mode, the above leakage current will be a big problem. Unfortunately, if users connect more than one analog input signal to Port 2 will encounter above current leakage situation. The pins of Port 2 configured as ADC input channel must be set as input mode, inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low) with [GPIO2\\_MODE](#) and [GPIO2\\_CFG](#) register by program to avoid current leakage.

Only one pin of Port 2 can be configured as ADC input in the same time. P2CON is Port2 Configuration status register. When ADC is enabled, HW will configure P2CON [15:0] to make the selected port 2 pin as pure analog input pin to avoid current leakage.

**\* Note: The GPIO mode of ADC input channels used must be set as input mode and inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low) with**

**GPIO2\_MODE and GPIO2\_CFG register by program.**

| Bit   | Name        | Description                                                                                                                                                                  | Attribute | Reset |
|-------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:16 | Reserved    |                                                                                                                                                                              | R         | 0     |
| 15:0  | P2CON[15:0] | P2.x configuration control bits. (x=0 to 15)<br>0: P2.x can be an analog input (ADC input) or digital I/O pins.<br>1: P2.x is pure analog input, can't be a digital I/O pin. | R         | 0     |

**7.6.4 ADC Interrupt Enable register (ADC\_IE)**

Address offset: 0x0C

This register allows control over which A/D channels generate an interrupt when a conversion is complete. For example, it may be desirable to use some A/D channels to monitor sensors by continuously performing conversions on them. The most recent results are read by the application program whenever they are needed. In this case, an interrupt is not desirable at the end of each conversion for some A/D channels.

| Bit   | Name     | Description                                                                                                                                                                        | Attribute | Reset |
|-------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:15 | Reserved |                                                                                                                                                                                    | R         | 0     |
| 14:0  | IE[14:0] | These bits allow control over which A/D channels generate interrupts for conversion completion. When bit x is one, completion of a conversion on AIN x will generate an interrupt. | R/W       | 0     |

**7.6.5 ADC Raw Interrupt Status register (ADC\_RIS)**

Address offset: 0x10

| Bit   | Name     | Description                                                                                                                                                                                                                                                | Attribute | Reset |
|-------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:15 | Reserved |                                                                                                                                                                                                                                                            | R         | 0     |
| 14:0  | IF[14:0] | ADC raw interrupt flag. (x = 0 to 14).<br>0: Read→No interrupt on AINx<br>Write→Write "0" to the corresponding bit will clear the bit and reset the Interrupt if the corresponding IE bit is set.<br>1: Interrupt requirements met on AINx ADC conversion. | R/W       | 0     |

# 8

## 16-BIT TIMER WITH CAPTURE FUNCTION

### 8.1 OVERVIEW

Each Counter/timer is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and can optionally generate interrupts or perform other actions at specified timer values based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

In PWM mode, up to three match registers can be used to provide a single-edge controlled PWM output on the match output pins.

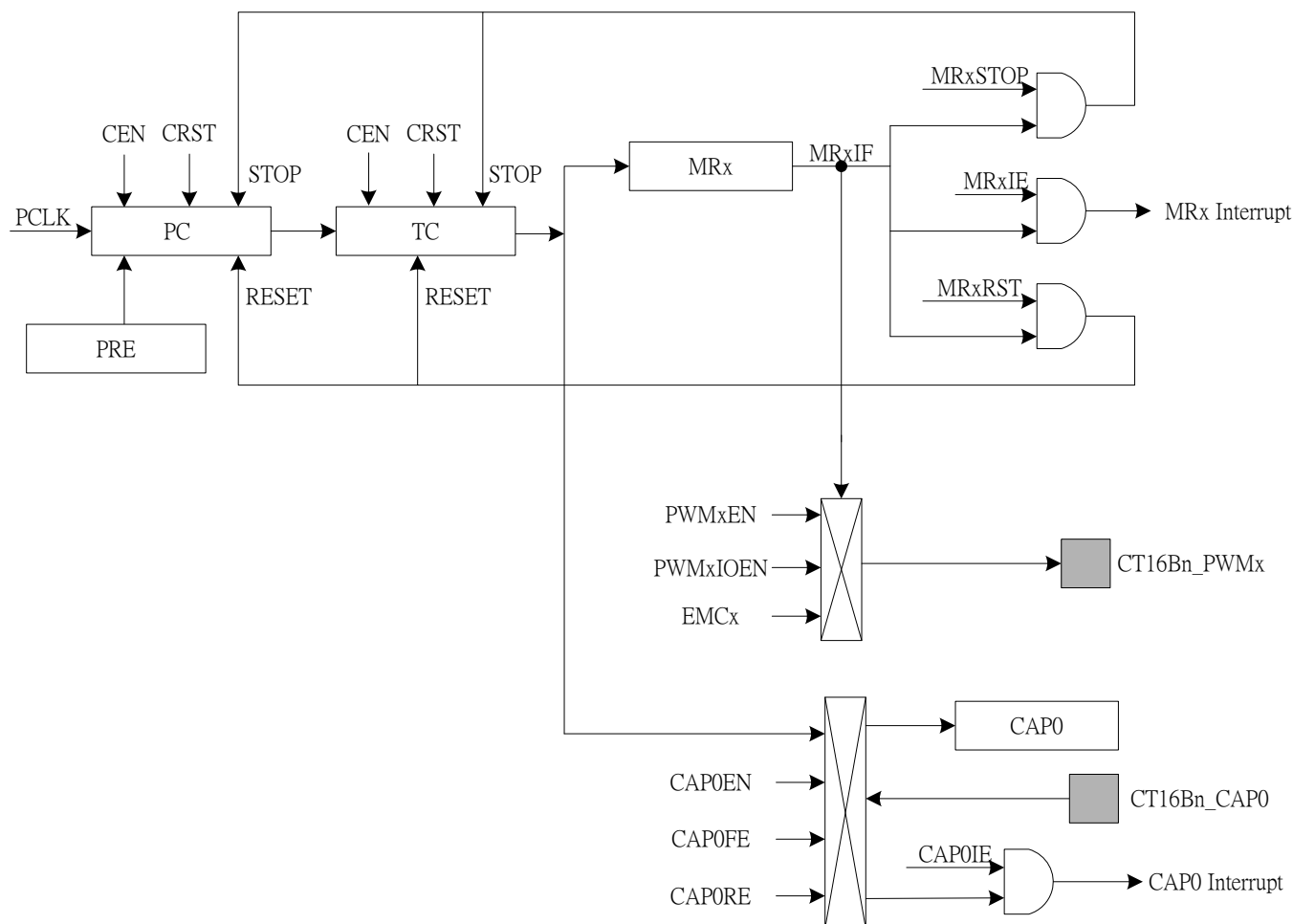
### 8.2 FEATURES

- \* Three 16-bit counter/timers with a programmable 16-bit prescaler.
- \* Counter or timer operation
- \* Three 16-bit capture channels that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- \* The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- \* For each timer, 16-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
  - Configured as PWM allowing using up to three match outputs as single edge controlled PWM outputs.
- \* For each timer, up to three PWM outputs corresponding to match registers with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

### 8.3 PIN DESCRIPTION

| Pin Name    | Type | Description                           | GPIO Configuration                |
|-------------|------|---------------------------------------|-----------------------------------|
| CT16Bn_CAP0 | I    | Capture channel input 0               | Depends on GPIO <sub>n</sub> _CFG |
| CT16Bn_PWMx | O    | Output channel x of Match/PWM output. |                                   |

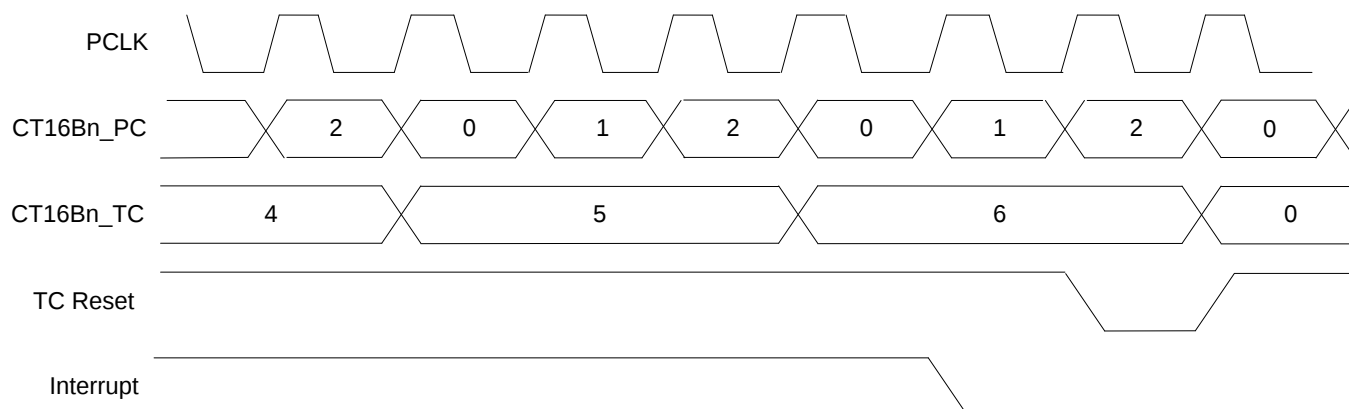
## 8.4 BLOCK DIAGRAM



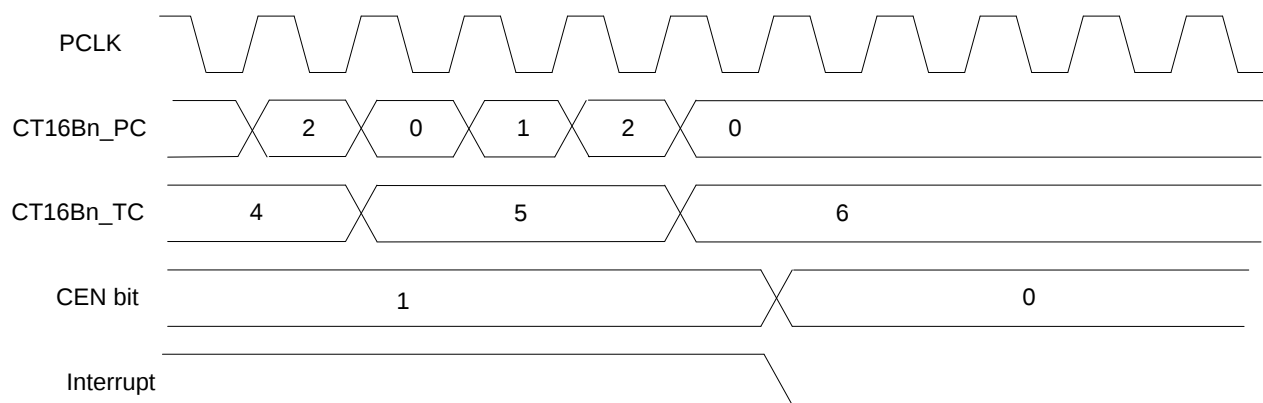
## 8.5 TIMER OPERATION

### 8.5.1 Edge-aligned Up-counting Mode

The following figure shows a timer configured to reset the count (TC) and generate an interrupt on match in Edge-aligned up-counting mode. The [CT16Bn\\_PRE](#) register is set to 2, and the [CT16Bn\\_MRx](#) register is set to 6. At the end of the timer cycle where the match occurs, the timer count is reset. This gives a full length cycle to the match value. The interrupt indicating that a match occurred is generated in the next clock after the timer reached the match value.



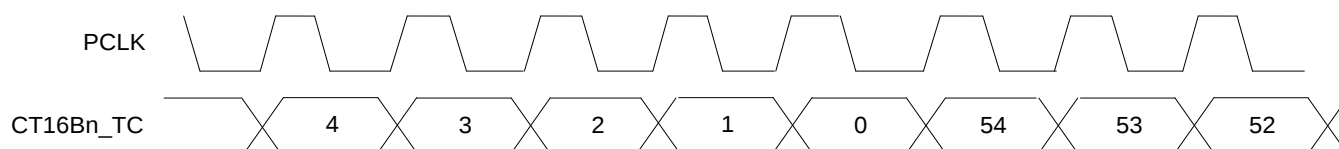
The following figure shows a timer configured to stop and generate an interrupt on match in Edge-aligned up-counting mode. The [CT16Bn\\_PRE](#) register is set to 2, and the [CT16Bn\\_MRx](#) register is set to 6. In the next clock after the timer reaches the match value, the CEN bit in [CT16Bn\\_TMRCTRL](#) register is cleared, and the interrupt indicating that a match occurred is generated.



## 8.5.2 Edge-aligned Down-counting Mode

The timer count TC[15:0] will be reset to the value of CT16Bn\_MR3 after resetting counter or TC reaches 0. Besides, TC is blocked while the value of CT16Bn\_MR3 is zero.

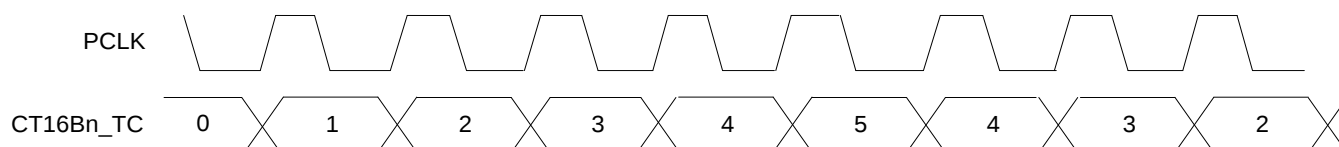
The following figure shows a timer configured to reset the count in Edge-aligned down-counting mode. The [CT16Bn\\_PRE](#) register is set to 0, and the [CT16Bn\\_MR3](#) register is set to 54. After TC reaches 0, the timer count is reset and loaded from the value of CT16Bn\_MR3.



## 8.5.3 Center-aligned Counting Mode

In Center-aligned counting mode, TC counts up from 0 to the value of CT16Bn\_MR3, and then counts down to 0 alternatively. Besides, TC is blocked while the value of CT16Bn\_MR3 is zero.

The following figure shows a timer in Center-aligned counting mode. The [CT16Bn\\_PRE](#) register is set to 0, and the [CT16Bn\\_MR3](#) register is set to 5.



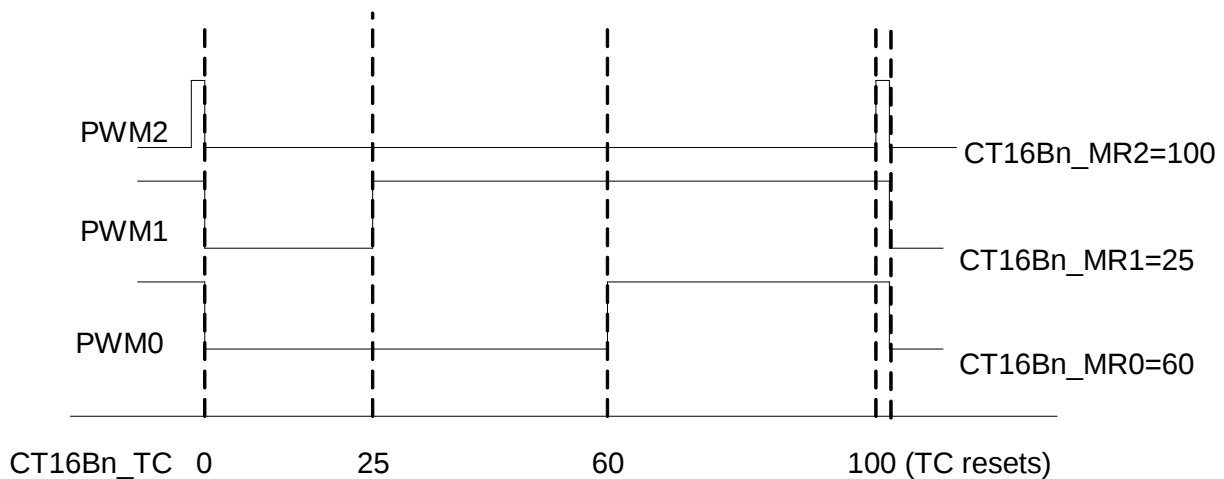
## 8.6 PWM

### 8.6.1 PWM Mode 1

- \* PWMn is 0 when  $TC < MRn$  during Up-counting period
- \* PWMn is 0 when  $TC \leq MRn$  during Down-counting period

Take Edge-aligned up-counting Mode as example,

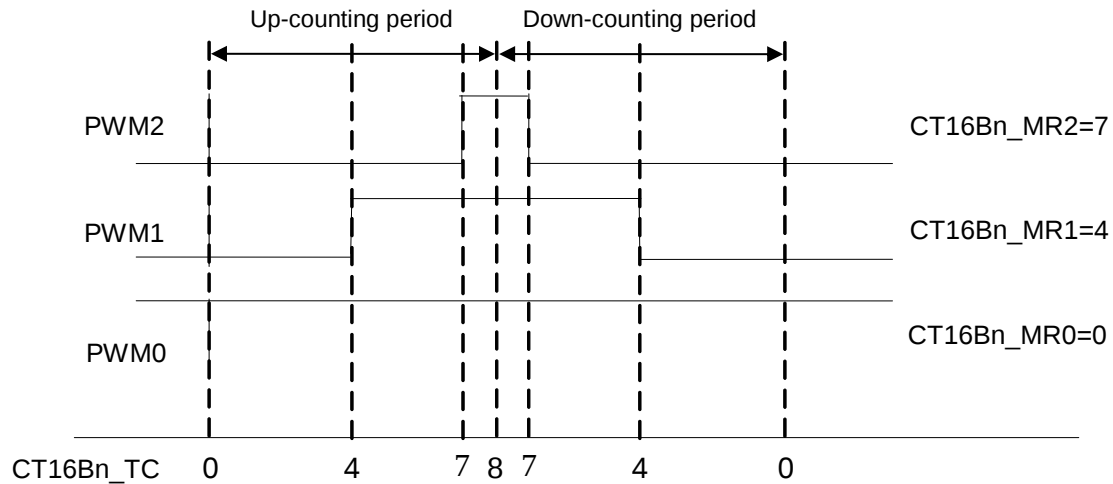
1. All single edge controlled PWM outputs go LOW at the beginning of each PWM cycle (timer is set to zero) unless their match value in CT16Bn\_MR0~3 registers is equal to zero.
2. Each PWM output will go HIGH when its match value is reached. If no match occurs, the PWM output remains continuously LOW.
3. If a match value larger than the PWM cycle length is written to the CT16Bn\_MR0~3 registers, and the PWM signal is HIGH already, then the PWM signal will be cleared on the next start of the next PWM cycle.
4. If a match register contains the same value as the timer reset value (the PWM cycle length), then the PWM output will be reset to LOW on the next clock tick. Therefore, the PWM output will always consist of a one clock tick wide positive pulse with a period determined by the PWM cycle length.
5. If a match register is set to zero, then the PWM output will go HIGH the first time the timer goes back to zero and will stay HIGH continuously.



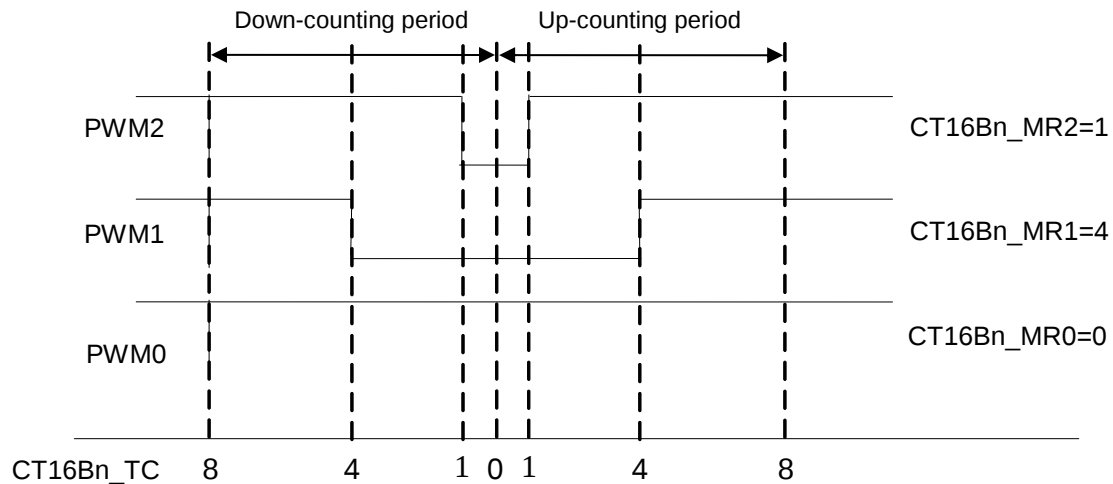
\* **Note:** When the match outputs are selected to perform as PWM outputs, the timer reset (MRnRST) and timer stop (MRnSTOP) bits in [CT16Bn\\_MCTRL](#) register must be set to zero except for the match register setting the PWM cycle length. For this register, set the MRnR bit to one to enable the timer reset when the timer value matches the value of the corresponding match register.

The following figure shows the PWM mode 1 wave form in Center-aligned counting mode.

Case1: The [CT16Bn\\_PRE](#) register is set to 0, the [CT16Bn\\_MR3](#) register is set to 8, the [CT16Bn\\_MR2](#) register is set to 7, the [CT16Bn\\_MR1](#) register is set to 4, and the [CT16Bn\\_MR0](#) register is set to 0.



Case 2: The [CT16Bn\\_PRE](#) register is set to 0, the [CT16Bn\\_MR3](#) register is set to 8, the [CT16Bn\\_MR2](#) register is set to 1, the [CT16Bn\\_MR1](#) register is set to 4, and the [CT16Bn\\_MR0](#) register is set to 0.



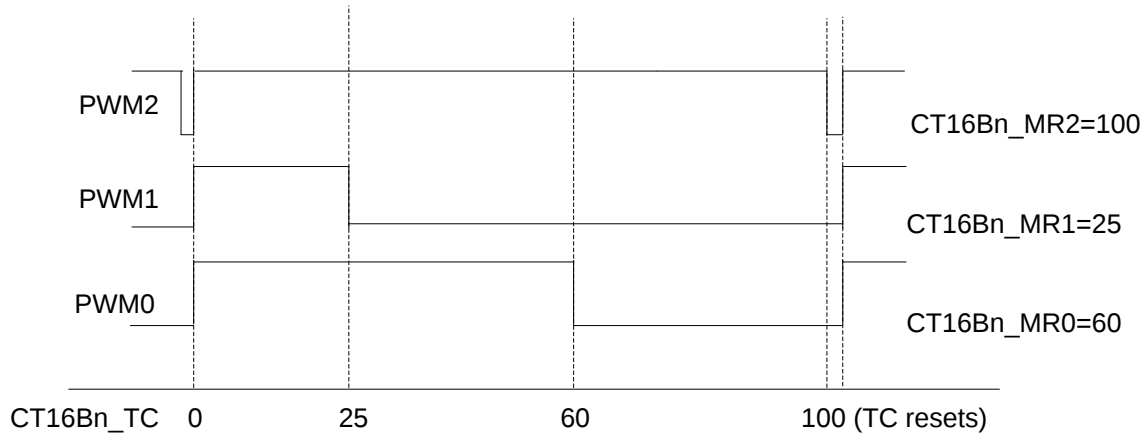
## 8.6.2 PWM Mode 2

- \* PWMn is 1 when TC<MRn during Up-counting period
- \* PWMn is 1 when TC≤MRn during Down-counting period
- \* Not support in Center-aligned counting mode

Take Edge-aligned up-counting Mode as example,

1. All single edge controlled PWM outputs go HIGH at the beginning of each PWM cycle (timer is set to zero) unless their match value in CT16Bn\_MR0~3 registers is equal to zero.
2. Each PWM output will go LOW when its match value is reached. If no match occurs, the PWM output remains continuously HIGH.
3. If a match value larger than the PWM cycle length is written to the CT16Bn\_MR0~3 registers, and the PWM signal is LOW already, then the PWM signal will go HIGH on the next start of the next PWM cycle.
4. If a match register contains the same value as the timer reset value (the PWM cycle length), then the PWM output will be reset to HIGH on the next clock tick. Therefore, the PWM output will always consist of a one clock tick wide low pulse with a period determined by the PWM cycle length.

5. If a match register is set to zero, then the PWM output will go LOW the first time the timer goes back to zero and will stay LOW continuously.



\* **Note:** When the match outputs are selected to perform as PWM outputs, the timer reset (MRnRST) and timer stop (MRnSTOP) bits in [CT16Bn\\_MCTRL](#) register must be set to zero except for the match register setting the PWM cycle length. For this register, set the MRnR bit to one to enable the timer reset when the timer value matches the value of the corresponding match register.

## 8.7 CT16Bn REGISTERS

Base Address: 0x4000 0000 (CT16B0)  
0x4000 2000 (CT16B1)  
0x4000 4000 (CT16B2)

### 8.7.1 CT16Bn Timer Control register (CT16Bn\_TMRCTRL) (n=0,1,2)

Address Offset: 0x00

**\* Note:** CEN bit shall be set at last!

| Bit  | Name     | Description                                                                                                                                                                                                                                                                                                                                                                                                                          | Attribute | Reset |
|------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:7 | Reserved |                                                                                                                                                                                                                                                                                                                                                                                                                                      | R         | 0     |
| 6:4  | CM[2:0]  | Counting mode selection<br>000: Edge-aligned Up-counting mode<br>001: Edge-aligned Down-counting mode<br>010: Center-aligned mode 1. The match interrupt flag is set during the down-counting period<br>100: Center-aligned mode 2. The match interrupt flag is set during the up-counting period<br>110: Center-aligned mode 3. The match interrupt flag is set during both up-counting and down-counting period<br>Other: Reserved | R/W       | 000b  |
| 3:2  | Reserved |                                                                                                                                                                                                                                                                                                                                                                                                                                      | R         | 0     |
| 1    | CRST     | Counter Reset.<br>0: Disable counter reset.<br>1: Timer Counter and the Prescale Counter are synchronously reset on the next positive edge of PCLK. This is cleared by HW when the counter reset operation finishes.                                                                                                                                                                                                                 | R/W       | 0     |
| 0    | CEN      | Counter Enable<br>0: Disable Counter.<br>1: Enable Timer Counter and Prescale Counter for counting.                                                                                                                                                                                                                                                                                                                                  | R/W       | 0     |

### 8.7.2 CT16Bn Timer Counter register (CT16Bn\_TC) (n=0,1,2)

Address Offset: 0x04

In Edge-aligned up-counting mode (CM[2:0]=000b), unless it is reset before reaching its upper limit, the TC will count up to the value 0x0000FFFF and then wrap back to the value 0x00000000. This event does not cause an interrupt, but a Match register can be used to detect an overflow if needed.

In Edge-aligned down-counting mode (CM[2:0]=001b), the TC[15:0] should be reset to the value of CT16Bn\_MR3 after resetting counter (SW set CRST to 1).

| Bit   | Name     | Description   | Attribute | Reset |
|-------|----------|---------------|-----------|-------|
| 31:16 | Reserved |               | R         | 0     |
| 15:0  | TC[15:0] | Timer Counter | R/W       | 0     |

### 8.7.3 CT16Bn Prescale register (CT16Bn\_PRE) (n=0,1,2)

Address Offset: 0x08

\* **Note:** If Counter mode is selected in the CNTCTRL register, PRE[7:0] must be set to 0x0.

| Bit   | Name     | Description         | Attribute | Reset |
|-------|----------|---------------------|-----------|-------|
| 31:16 | Reserved |                     | R         | 0     |
| 15:0  | PR[15:0] | Prescale max value. | R/W       | 0     |

### 8.7.4 CT16Bn Prescale Counter register (CT16Bn\_PC) (n=0,1,2)

Address Offset: 0x0C

The 16-bit Prescale Counter controls division of PCLK by some constant value before it is applied to the Timer Counter. This allows control of the relationship between the resolution of the timer and the maximum time before the timer overflows. The Prescale Counter is incremented on every PCLK. When it reaches the value stored in the Prescale Register, the Timer Counter is incremented, and the Prescale Counter is reset on the next PCLK. This causes the TC to increment on every PCLK when PR = 0, every 2 PCLKs when PR = 1, etc.

| Bit   | Name     | Description      | Attribute | Reset |
|-------|----------|------------------|-----------|-------|
| 31:16 | Reserved |                  | R         | 0     |
| 15:0  | PC[15:0] | Prescale Counter | R/W       | 0     |

### 8.7.5 CT16Bn Count Control register (CT16Bn\_CNTCTRL) (n=0,1,2)

Address Offset: 0x10

This register is used to select between Timer and Counter mode, and in Counter mode to select the pin and edges for counting.

When Counter Mode is chosen as a mode of operation, the CAP input (selected by the CIS bits) is sampled on every rising edge of the PCLK clock. After comparing two consecutive samples of this CAP input, one of the following four events is recognized: rising edge, falling edge, either of edges or no changes in the level of the selected CAP input. Only if the identified event occurs, and the event corresponds to the one selected by CTM bits in this register, will the Timer Counter register be incremented.

Effective processing of the externally supplied clock to the counter has some limitations. Since two successive rising edges of the PCLK clock are used to identify only one edge on the CAP selected input, the frequency of the CAP input cannot exceed one half of the PCLK clock. Consequently, the duration of the HIGH/LOW levels on the same CAP input in this case cannot be shorter than  $1/(2 \times \text{PCLK})$ .

\* **Note:** If Counter mode is selected in the CNTCTRL register, bit 2 to 0 of Capture Control (CAPCTRL) register and bit 7 to 0 of Prescale (PRE) register must be set to 0x0.

| Bit  | Name     | Description                                                                                                                  | Attribute | Reset |
|------|----------|------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:4 | Reserved |                                                                                                                              | R         | 0     |
| 3:2  | CIS[1:0] | Count Input Select.<br>In counter mode (when CTM[1:0] are not 00), these bits select which CAP0 pin is sampled for clocking. | R/W       | 0     |

|            |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |     |   |
|------------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---|
|            |                 | 00: CT16Bn_CAP0<br>Other: Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                |     |   |
| <b>1:0</b> | <b>CTM[1:0]</b> | Counter/Timer Mode.<br>This field selects which rising PCLK edges can increment Timer's Prescale Counter (PC), or clear PC and increment Timer Counter (TC).<br>00: Timer Mode: every rising PCLK edge<br>01: Counter Mode: TC is incremented on rising edges on the CAP0 input selected by CIS bits.<br>10: Counter Mode: TC is incremented on falling edges on the CAP0 input selected by CIS bits.<br>11: Counter Mode: TC is incremented on both edges on the CAP0 input selected by CIS bits. | R/W | 0 |

### 8.7.6 CT16Bn Match Control register (CT16Bn\_MCTRL) (n=0,1,2)

Address Offset: 0x14

| Bit          | Name           | Description                                                                                                      | Attribute | Reset |
|--------------|----------------|------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:12</b> | Reserved       |                                                                                                                  | R         | 0     |
| <b>11</b>    | <b>MR3STOP</b> | Stop MR3: TC and PC will stop and CEN bit will be cleared if MR3 matches TC.<br>0: Disable<br>1: Enable          | R/W       | 0     |
| <b>10</b>    | <b>MR3RST</b>  | Enable reset TC when MR3 matches TC.<br>0: Disable<br>1: Enable                                                  | R/W       | 0     |
| <b>9</b>     | <b>MR3IE</b>   | Enable generating an interrupt based on CM[2:0] when MR3 matches the value in the TC.<br>0: Disable<br>1: Enable | R/W       | 0     |
| <b>8</b>     | <b>MR2STOP</b> | Stop MR2: TC and PC will stop and CEN bit will be cleared if MR2 matches TC.<br>0: Disable<br>1: Enable          | R/W       | 0     |
| <b>7</b>     | <b>MR2RST</b>  | Enable reset TC when MR2 matches TC.<br>0: Disable<br>1: Enable                                                  | R/W       | 0     |
| <b>6</b>     | <b>MR2IE</b>   | Enable generating an interrupt based on CM[2:0] when MR2 matches the value in the TC.<br>0: Disable<br>1: Enable | R/W       | 0     |
| <b>5</b>     | <b>MR1STOP</b> | Stop MR1: TC and PC will stop and CEN bit will be cleared if MR1 matches TC.<br>0: Disable<br>1: Enable          | R/W       | 0     |
| <b>4</b>     | <b>MR1RST</b>  | Enable reset TC when MR1 matches TC.<br>0: Disable<br>1: Enable                                                  | R/W       | 0     |
| <b>3</b>     | <b>MR1IE</b>   | Enable generating an interrupt based on CM[2:0] when MR1 matches the value in the TC.<br>0: Disable<br>1: Enable | R/W       | 0     |
| <b>2</b>     | <b>MR0STOP</b> | Stop MR0: TC and PC will stop and CEN bit will be cleared if MR0 matches TC.<br>0: Disable<br>1: Enable          | R/W       | 0     |
| <b>1</b>     | <b>MR0RST</b>  | Enable reset TC when MR0 matches TC.<br>0: Disable<br>1: Enable                                                  | R/W       | 0     |
| <b>0</b>     | <b>MR0IE</b>   | Enable generating an interrupt based on CM[2:0] when MR0 matches the value in the TC.<br>0: Disable<br>1: Enable | R/W       | 0     |

### 8.7.7 CT16Bn Match register 0~3 (CT16Bn\_MR0~3) (n=0,1,2)

Address Offset: 0x18, 0x1C, 0x20, 0x24

The Match register values are continuously compared to the Timer Counter (TC) value. When the two values are equal, actions can be triggered automatically. The action possibilities are to generate an interrupt, reset the Timer Counter, or stop the timer. Actions are controlled by the settings in the CT16Bn\_MCTRL register.

| Bit   | Name     | Description               | Attribute | Reset |
|-------|----------|---------------------------|-----------|-------|
| 31:16 | Reserved |                           | R         | 0     |
| 15:0  | MR[15:0] | Timer counter match value | R/W       | 0     |

### 8.7.8 CT16Bn Capture Control register (CT16Bn\_CAPCTRL) (n=0,1,2)

Address Offset: 0x28

The Capture Control register is used to control whether the Capture register is loaded with the value in the Counter/timer when the capture event occurs, and whether an interrupt is generated by the capture event. Setting both the rising and falling bits at the same time is a valid configuration, resulting in a capture event for both edges.

**\* Note: HW will switch I/O Configuration directly when CAP0EN=1.**

| Bit  | Name     | Description                                                                                                                                                 | Attribute | Reset |
|------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:4 | Reserved |                                                                                                                                                             | R         | 0     |
| 3    | CAP0EN   | Capture 0 function enable bit<br>0: Disable<br>1: Enable.                                                                                                   | R/W       | 0     |
| 2    | CAP0IE   | Interrupt on CT16Bn_CAP0 event: a CAP0 load due to a CT16Bn_CAP0 event will generate an interrupt.<br>0: Disable<br>1: Enable                               | R/W       | 0     |
| 1    | CAP0FE   | Capture on CT16Bn_CAP0 falling edge: a sequence of 1 then 0 on CT16Bn_CAP0 will cause CAP0 to be loaded with the contents of TC.<br>0: Disable<br>1: Enable | R/W       | 0     |
| 0    | CAP0RE   | Capture on CT16Bn_CAP0 rising edge: a sequence of 0 then 1 on CT16Bn_CAP0 will cause CAP0 to be loaded with the contents of TC.<br>0: Disable<br>1: Enable  | R/W       | 0     |

### 8.7.9 CT16Bn Capture 0 register (CT16Bn\_CAP0) (n=0,1,2)

Address Offset: 0x2C

Each Capture register is associated with a device pin and may be loaded with the counter/timer value when a specified event occurs on that pin. The settings in the Capture Control register determine whether the capture function is enabled, and whether a capture event happens on the rising edge of the associated pin, the falling edge, or on both edges.

| Bit   | Name       | Description                 | Attribute | Reset |
|-------|------------|-----------------------------|-----------|-------|
| 31:16 | Reserved   |                             | R         | 0     |
| 15:0  | CAP0[15:0] | Timer counter capture value | R         | 0     |

### 8.7.10 CT16Bn External Match register (CT16Bn\_EM) (n=0,1,2)

Address Offset: 0x30

The External Match register provides both control and status of CT16Bn\_PWM[2:0]. If the match outputs are configured as PWM output, the function of the external match registers is determined by the [PWM rules](#).

| Bit   | Name      | Description                                                                                                                                                 | Attribute | Reset |
|-------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:10 | Reserved  |                                                                                                                                                             | R         | 0     |
| 9:8   | EMC2[1:0] | Determines the functionality of CT16Bn_PWM2.<br>00: Do Nothing.<br>01: CT16Bn_PWM2 pin is LOW<br>10: CT16Bn_PWM2 pin is HIGH<br>11: Toggle CT16Bn_PWM2 pin. | R/W       | 0     |
| 7:6   | EMC1[1:0] | Determines the functionality of CT16Bn_PWM1.<br>00: Do Nothing.<br>01: CT16Bn_PWM1 pin is LOW<br>10: CT16Bn_PWM1 pin is HIGH.<br>11: Toggle CT16Bn_PWM1.    | R/W       | 0     |
| 5:4   | EMC0[1:0] | Determines the functionality of CT16Bn_PWM0.<br>00: Do Nothing.<br>01: CT16Bn_PWM0 pin is LOW<br>10: CT16Bn_PWM0 pin is HIGH<br>11: Toggle CT16Bn_PWM0.     | R/W       | 0     |
| 3     | Reserved  |                                                                                                                                                             | R         | 0     |
| 2     | EM2       | When the TC and MR2 are equal, this bit will act according to EMC2 bits, and also drive the state of CT16Bn_PWM2 output.                                    | R/W       | 0     |
| 1     | EM1       | When the TC and MR1 are equal, this bit will act according to EMC1 bits, and also drive the state of CT16Bn_PWM1 output.                                    | R/W       | 0     |
| 0     | EM0       | When the TC and MR0 are equal, this bit will act according to EMC0 bits, and also drive the state of CT16Bn_PWM0 output.                                    | R/W       | 0     |

### 8.7.11 CT16Bn PWM Control register (CT16Bn\_PWMCTRL) (n=0,1,2)

Address Offset: 0x34

The PWM Control register is used to configure the match outputs as PWM outputs. Each match output can be in-dependently set to perform either as PWM output or as match output whose function is controlled by [CT16Bn\\_EM](#) register.

For each timer, a maximum of three single edge controlled PWM outputs can be selected on the CT16Bn\_PWMCTRL [2:0] outputs. One additional match register determines the PWM cycle length. When a match occurs in any of the other match registers, the PWM output is set to HIGH. The timer is reset by the match register that is configured to set the PWM cycle length. When the timer is reset to zero, all currently HIGH match outputs configured as PWM outputs are cleared.

| Bit   | Name     | Description                                                                                                                                          | Attribute | Reset |
|-------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:23 | Reserved |                                                                                                                                                      | R         | 0     |
| 22    | PWM2IOEN | CT16Bn_PWM2/GPIO selection bit<br>0: CT16Bn_PWM2 pin act as GPIO<br>1: CT16Bn_PWM2 pin act as match output, and output signal depends on PWM2EN bit. | R/W       | 0     |
| 21    | PWM1IOEN | CT16Bn_PWM1/GPIO selection bit<br>0: CT16Bn_PWM1 pin act as GPIO<br>1: CT16Bn_PWM1 pin act as match output, and output signal depends on PWM1EN bit. | R/W       | 0     |
| 20    | PWM0IOEN | CT16Bn_PWM0/GPIO selection bit<br>0: CT16Bn_PWM0 pin act as GPIO<br>1: CT16Bn_PWM0 pin act as match output, and output signal depends on PWM0EN bit. | R/W       | 0     |

|              |               |                                                                                                |     |   |
|--------------|---------------|------------------------------------------------------------------------------------------------|-----|---|
| <b>19:10</b> | Reserved      |                                                                                                | R   | 0 |
| <b>9:8</b>   | PWM2MODE[1:0] | PWM2 output mode<br>00: PWM mode 1<br>01: PWM mode 2<br>10: Forced to 0.<br>11: Forced to 1.   | R/W | 0 |
| <b>7:6</b>   | PWM1MODE[1:0] | PWM1 output mode<br>00: PWM mode 1<br>01: PWM mode 2<br>10: Forced to 0.<br>11: Forced to 1.   | R/W | 0 |
| <b>5:4</b>   | PWM0MODE[1:0] | PWM0 output mode<br>00: PWM mode 1<br>01: PWM mode 2<br>10: Forced to 0.<br>11: Forced to 1.   | R/W | 0 |
| <b>3</b>     | Reserved      |                                                                                                | R   | 0 |
| <b>2</b>     | PWM2EN        | PWM2 enable<br>0: CT16Bn_PWM2 is controlled by EM2.<br>1: PWM mode is enabled for CT16Bn_PWM2. | R/W | 0 |
| <b>1</b>     | PWM1EN        | PWM1 enable<br>0: CT16Bn_PWM1 is controlled by EM1.<br>1: PWM mode is enabled for CT16Bn_PWM1. | R/W | 0 |
| <b>0</b>     | PWM0EN        | PWM0 enable<br>0: CT16Bn_PWM0 is controlled by EM0.<br>1: PWM mode is enabled for CT16Bn_PWM0. | R/W | 0 |

### 8.7.12 CT16Bn Timer Raw Interrupt Status register (CT16Bn\_RIS) (n=0,1,2)

Address Offset: 0x38

This register indicates the raw status for Timer/PWM interrupts. A Timer/PWM interrupt is sent to the interrupt controller if the corresponding bit in the CT16Bn\_IE register is set.

| Bit         | Name     | Description                                                                                                                    | Attribute | Reset |
|-------------|----------|--------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:5</b> | Reserved |                                                                                                                                | R         | 0     |
| <b>4</b>    | CAP0IF   | Interrupt flag for capture channel 0.<br>0: No interrupt on CAP0<br>1: Interrupt requirements met on CAP0.                     | R         | 0     |
| <b>3</b>    | MR3IF    | Interrupt flag for match channel 3.<br>0: No interrupt on match channel 3<br>1: Interrupt requirements met on match channel 3. | R         | 0     |
| <b>2</b>    | MR2IF    | Interrupt flag for match channel 2.<br>0: No interrupt on match channel 2<br>1: Interrupt requirements met on match channel 2. | R         | 0     |
| <b>1</b>    | MR1IF    | Interrupt flag for match channel 1.<br>0: No interrupt on match channel 1<br>1: Interrupt requirements met on match channel 1. | R         | 0     |
| <b>0</b>    | MR0IF    | Interrupt flag for match channel 0.<br>0: No interrupt on match channel 0<br>1: Interrupt requirements met on match channel 0. | R         | 0     |

**8.7.13 CT16Bn Timer Interrupt Clear register (CT16Bn\_IC) (n=0,1,2)**

Address Offset: 0x3C

| Bit  | Name     | Description                         | Attribute | Reset |
|------|----------|-------------------------------------|-----------|-------|
| 31:5 | Reserved |                                     | R         | 0     |
| 4    | CAP0IC   | 0: No effect<br>1: Clear CAP0IF bit | W         | 0     |
| 3    | MR3IC    | 0: No effect<br>1: Clear MR3IF bit  | W         | 0     |
| 2    | MR2IC    | 0: No effect<br>1: Clear MR2IF bit  | W         | 0     |
| 1    | MR1IC    | 0: No effect<br>1: Clear MR1IF bit  | W         | 0     |
| 0    | MR0IC    | 0: No effect<br>1: Clear MR0IF bit  | W         | 0     |

# 9

## 32-BIT TIMER WITH CAPTURE FUNCTION

### 9.1 OVERVIEW

Each Counter/timer is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and can optionally generate interrupts or perform other actions at specified timer values based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

In PWM mode, up to four match registers can be used to provide a single-edge controlled PWM output on the match output pins.

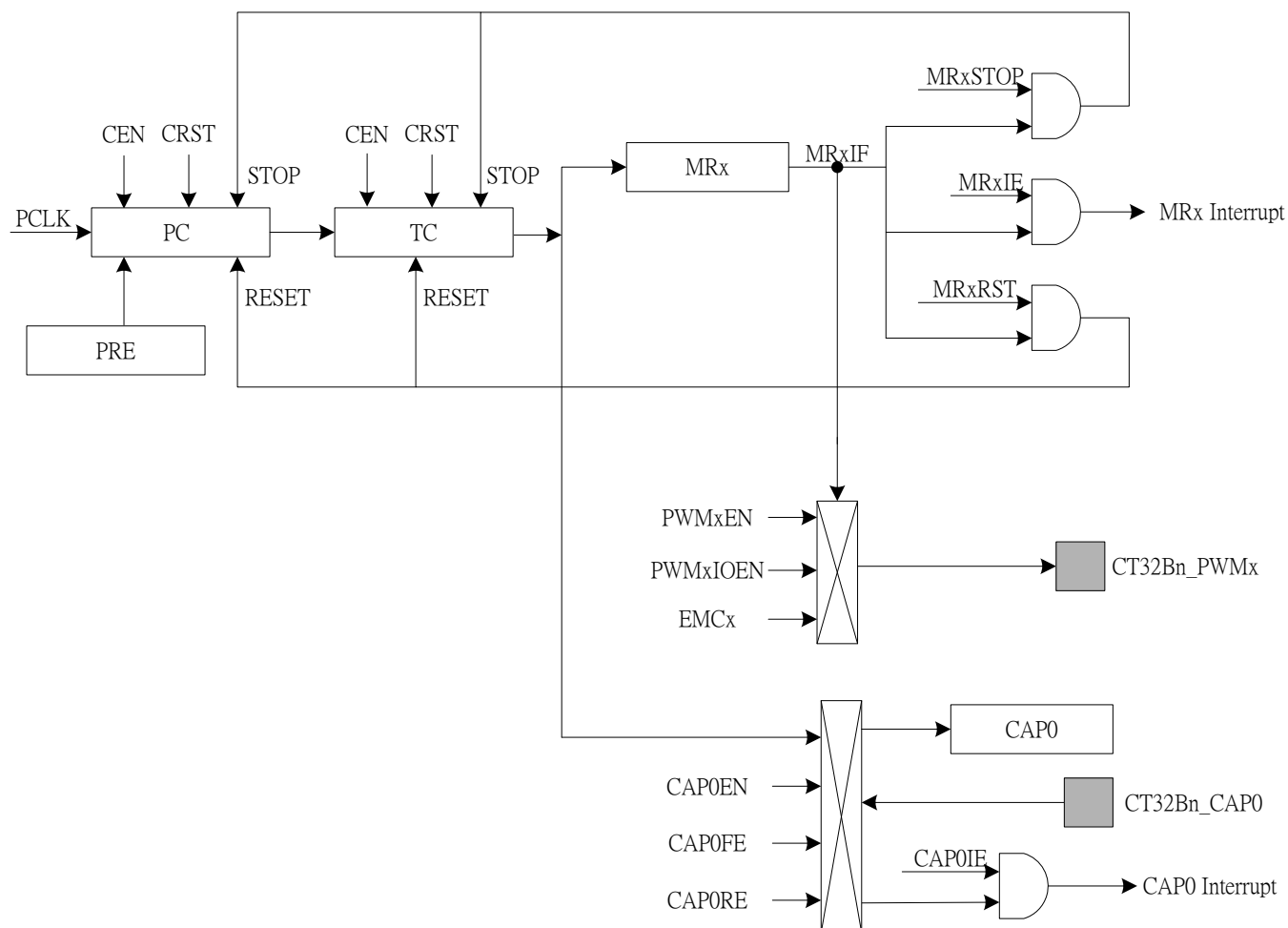
### 9.2 FEATURES

1. Three 32-bit counter/timers with a programmable 32-bit prescaler.
2. Counter or timer operation
3. Three 32-bit capture channels that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
4. The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
5. For each timer, 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
  - Configured as PWM allowing using up to four match outputs as single edge controlled PWM outputs.
6. For each timer, up to four PWM outputs corresponding to match registers with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

### 9.3 PIN DESCRIPTION

| Pin Name    | Type | Description                           | GPIO Configuration                |
|-------------|------|---------------------------------------|-----------------------------------|
| CT32Bn_CAP0 | I    | Capture channel input 0               | Depends on GPIO <sub>n</sub> _CFG |
| CT32Bn_PWMx | O    | Output channel x of Match/PWM output. |                                   |

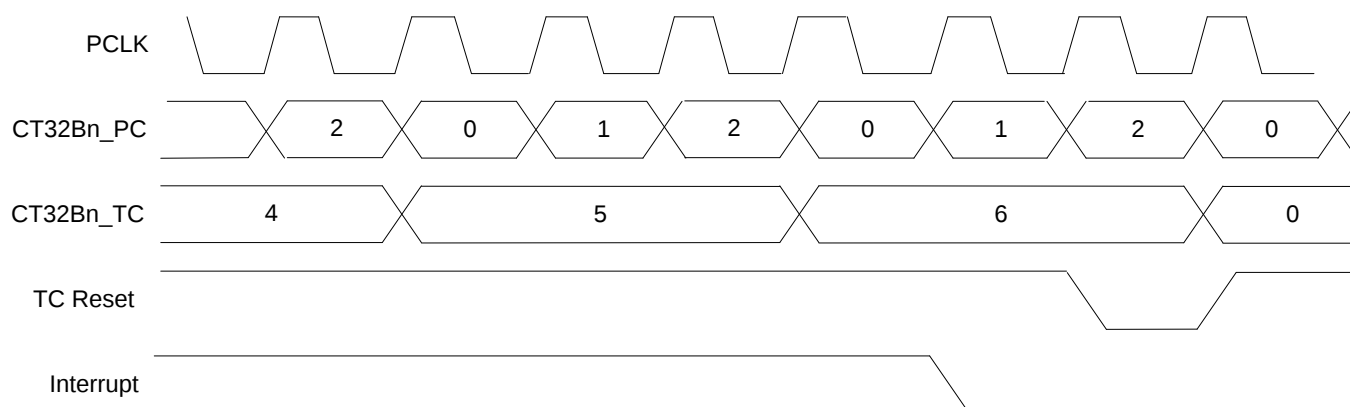
## 9.4 BLOCK DIAGRAM



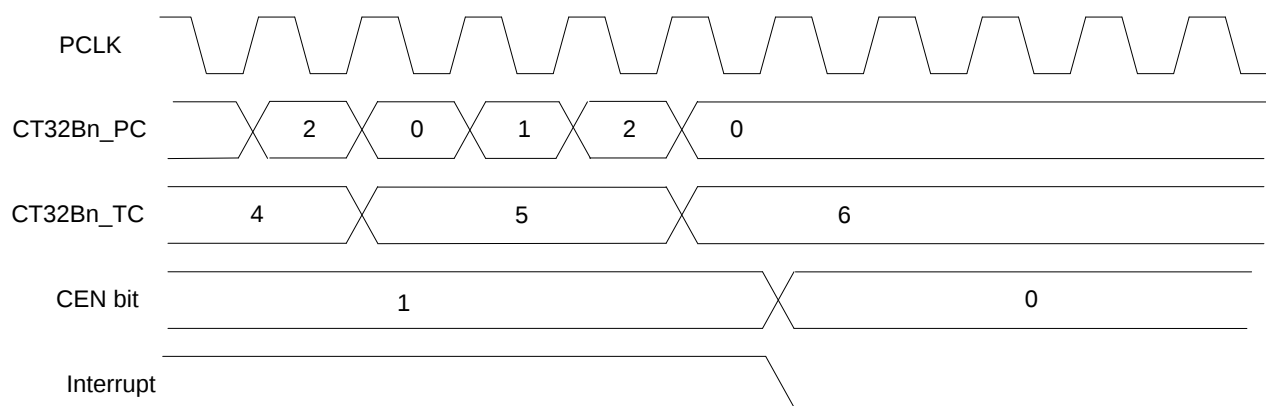
## 9.5 TIMER OPERATION

### 9.5.1 Edge-aligned Up-counting Mode

The following figure shows a timer configured to reset the count and generate an interrupt on match. The [CT32Bn\\_PRE](#) register is set to 2, and the [CT32Bn\\_MRx](#) register is set to 6. At the end of the timer cycle where the match occurs, the timer count is reset. This gives a full length cycle to the match value. The interrupt indicating that a match occurred is generated in the next clock after the timer reached the match value.



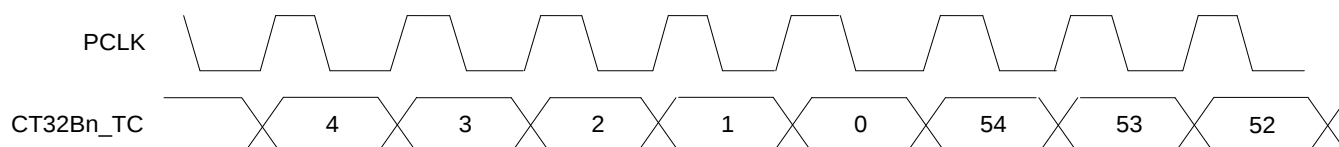
The following figure shows a timer configured to stop and generate an interrupt on match. The [CT32Bn\\_PRE](#) register is set to 2, and the [CT32Bn\\_MRx](#) register is set to 6. In the next clock after the timer reaches the match value, the CEN bit in [CT32Bn\\_TMRCTRL](#) register is cleared, and the interrupt indicating that a match occurred is generated.



## 9.5.2 Edge-aligned Down-counting Mode

The timer count TC[31:0] will be reset to the value of CT32Bn\_MR3 after resetting counter or TC reaches 0. Besides, TC is blocked while the value of CT132Bn\_MR3 is zero.

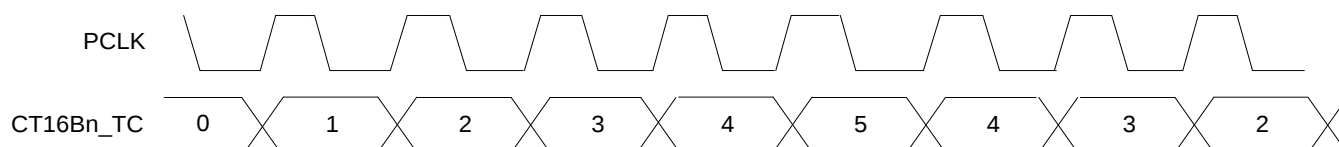
The following figure shows a timer configured to reset the count in Edge-aligned down-counting mode. The [CT32Bn\\_PRE](#) register is set to 0, and the [CT32Bn\\_MR3](#) register is set to 54. After TC reaches 0, the timer count is reset and loaded from the value of CT32Bn\_MR3.



## 9.5.3 Center-aligned Counting Mode

In Center-aligned counting mode, TC counts up from 0 to the value of CT32Bn\_MR3, and then counts down to 0 alternatively. Besides, TC is blocked while the value of CT32Bn\_MR3 is zero.

The following figure shows a timer in Center-aligned counting mode. The [CT32Bn\\_PRE](#) register is set to 0, and the [CT32Bn\\_MR3](#) register is set to 5.



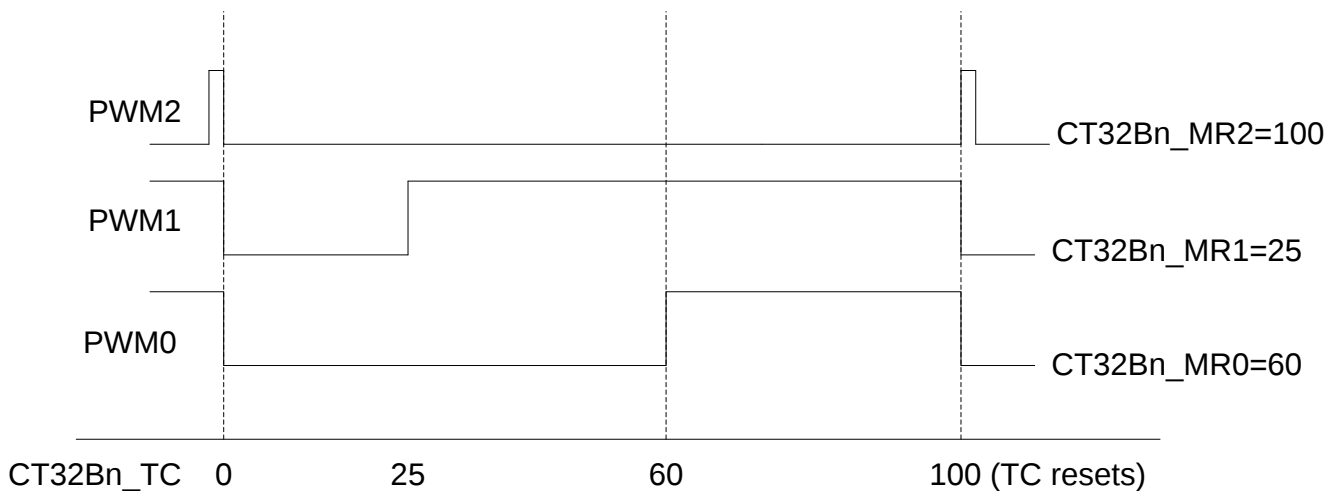
## 9.6 PWM

### 9.6.1 PWM Mode 1

- \* PWMn is 0 when  $TC < MRn$  during Up-counting period
- \* PWMn is 0 when  $TC \leq MRn$  during Down-counting period

Take Edge-aligned Up-counting Mode as example,

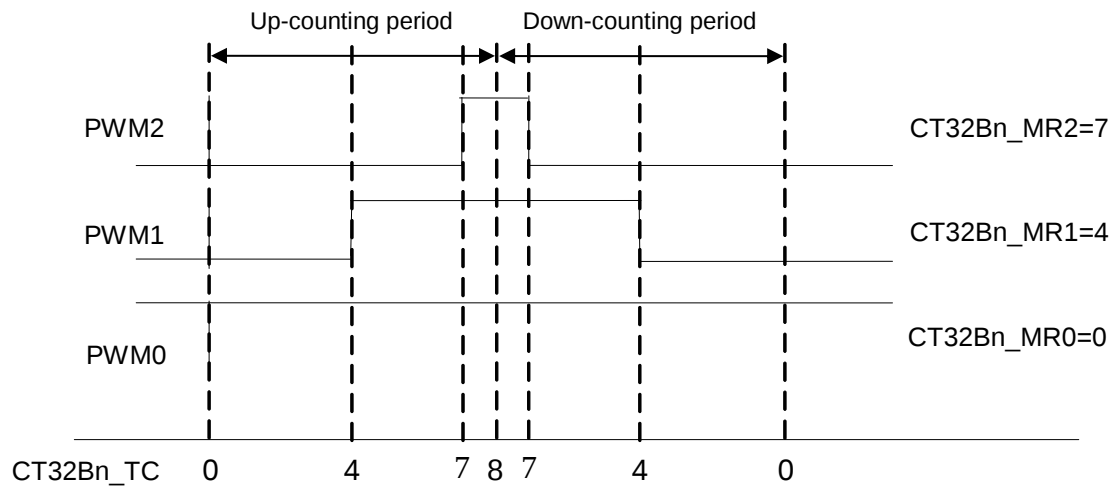
1. All single edge controlled PWM outputs go LOW at the beginning of each PWM cycle (timer is set to zero) unless their match value in CT32Bn\_MR0~3 registers is equal to zero.
2. Each PWM output will go HIGH when its match value is reached. If no match occurs, the PWM output remains continuously LOW.
3. If a match value larger than the PWM cycle length is written to the CT32Bn\_MR0~3 registers, and the PWM signal is HIGH already, then the PWM signal will be cleared on the next start of the next PWM cycle.
4. If a match register contains the same value as the timer reset value (the PWM cycle length), then the PWM output will be reset to LOW on the next clock tick. Therefore, the PWM output will always consist of a one clock tick wide positive pulse with a period determined by the PWM cycle length.
5. If a match register is set to zero, then the PWM output will go to HIGH the first time the timer goes back to zero and will stay HIGH continuously.



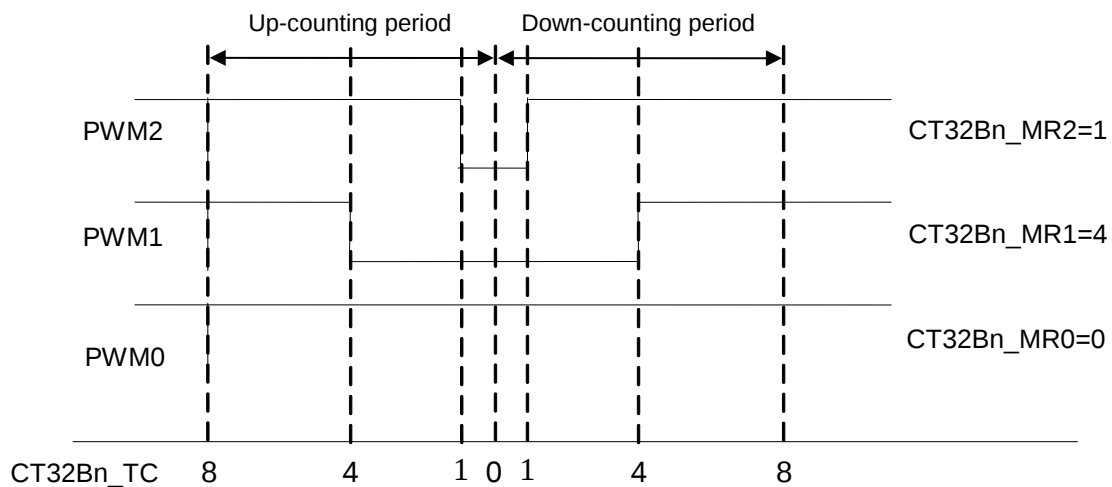
\* **Note:** When the match outputs are selected to perform as PWM outputs, the timer reset (MRnRST) and timer stop (MRnSTOP) bits in [CT32Bn\\_MCTRL](#) register must be set to zero except for the match register setting the PWM cycle length. For this register, set the MRnR bit to one to enable the timer reset when the timer value matches the value of the corresponding match register.

The following figure shows the PWM mode 1 wave form in Center-aligned counting mode.

Case 1: The [CT32Bn\\_PRE](#) register is set to 0, the [CT32Bn\\_MR3](#) register is set to 8, the [CT32Bn\\_MR2](#) register is set to 7, the [CT32Bn\\_MR1](#) register is set to 4, and the [CT32Bn\\_MR0](#) register is set to 0.



Case 2: The [CT32Bn\\_PRE](#) register is set to 0, the [CT32Bn\\_MR3](#) register is set to 8, the [CT32Bn\\_MR2](#) register is set to 1, the [CT32Bn\\_MR1](#) register is set to 4, and the [CT32Bn\\_MR0](#) register is set to 0.



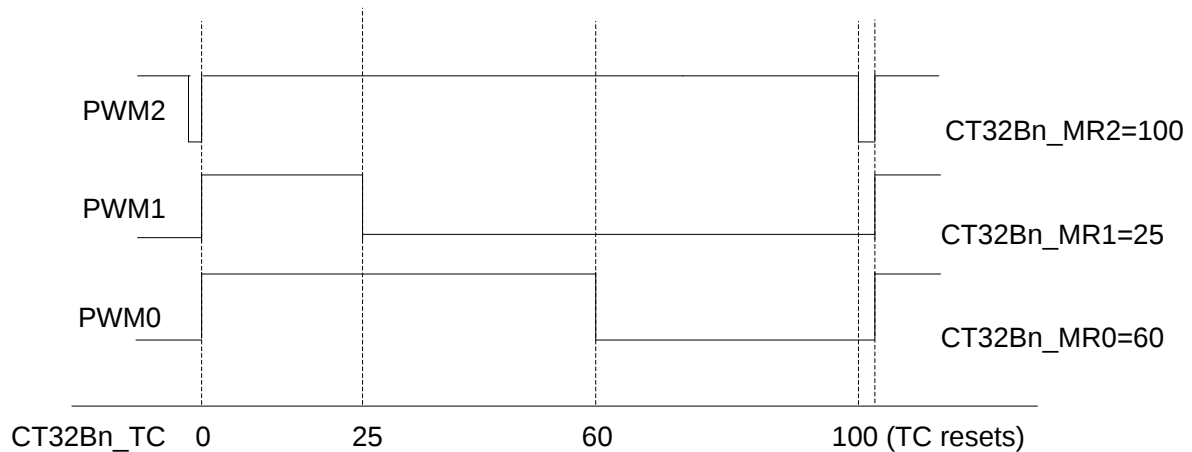
## 9.6.2 PWM Mode 2

- PWMn is 1 when  $TC < MRn$  during Up-counting period
- PWMn is 1 when  $TC \leq MRn$  during Down-counting period
- Not support in Center-aligned counting mode

Take Edge-aligned up-counting Mode as example,

1. All single edge controlled PWM outputs go HIGH at the beginning of each PWM cycle (timer is set to zero) unless their match value in CT32Bn\_MR0~3 registers is equal to zero.
2. Each PWM output will go LOW when its match value is reached. If no match occurs, the PWM output remains continuously HIGH.
3. If a match value larger than the PWM cycle length is written to the CT32Bn\_MR0~3 registers, and the PWM signal is LOW already, then the PWM signal will go HIGH on the next start of the next PWM cycle.
4. If a match register contains the same value as the timer reset value (the PWM cycle length), then the PWM output will be reset to HIGH on the next clock tick. Therefore, the PWM output will always consist of a one clock tick wide low pulse with a period determined by the PWM cycle length.

5. If a match register is set to zero, then the PWM output will go LOW the first time the timer goes back to zero and will stay LOW continuously.



\* **Note:** When the match outputs are selected to perform as PWM outputs, the timer reset (MRnRST) and timer stop (MRnSTOP) bits in [CT32Bn\\_MCTRL](#) register must be set to zero except for the match register setting the PWM cycle length. For this register, set the MRnR bit to one to enable the timer reset when the timer value matches the value of the corresponding match register.

## 9.7 CT32Bn REGISTERS

Base Address: 0x4000 6000 (CT32B0)  
0x4000 8000 (CT32B1)  
0x4000 A000 (CT32B2)

### 9.7.1 CT32Bn Timer Control register (CT32Bn\_TMRCTRL) (n=0,1,2)

Address Offset: 0x00

**\* Note:** CEN bit shall be set at last!

| Bit  | Name     | Description                                                                                                                                                                                                                                                                                                                                                                                                                          | Attribute | Reset |
|------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:7 | Reserved |                                                                                                                                                                                                                                                                                                                                                                                                                                      | R         | 0     |
| 6:4  | CM[2:0]  | Counting mode selection<br>000: Edge-aligned Up-counting mode<br>001: Edge-aligned Down-counting mode<br>010: Center-aligned mode 1. The match interrupt flag is set during the down-counting period<br>100: Center-aligned mode 2. The match interrupt flag is set during the up-counting period<br>110: Center-aligned mode 3. The match interrupt flag is set during both up-counting and down-counting period<br>Other: Reserved | R/W       | 000b  |
| 3:2  | Reserved |                                                                                                                                                                                                                                                                                                                                                                                                                                      | R         | 0     |
| 1    | CRST     | Counter Reset.<br>0: Disable counter reset.<br>1: Timer Counter is synchronously reset on the next positive edge of PCLK. This is cleared by HW when the counter reset operation finishes.                                                                                                                                                                                                                                           | R/W       | 0     |
| 0    | CEN      | Counter Enable<br>0: Disable Counter.<br>1: Enable Timer Counter for counting.                                                                                                                                                                                                                                                                                                                                                       | R/W       | 0     |

### 9.7.2 CT32Bn Timer Counter register (CT32Bn\_TC) (n=0,1,2)

Address Offset: 0x04

In Edge-aligned up-counting mode (CM[2:0]=000b), unless it is reset before reaching its upper limit, the TC will count up to the value 0xFFFFFFFF and then wrap back to the value 0x00000000. This event does not cause an interrupt, but a Match register can be used to detect an overflow if needed.

In Edge-aligned down-counting mode (CM[2:0]=001b), the TC[31:0] should be reset to the value of CT32Bn\_MR3 after resetting counter (SW set CRST to 1).

| Bit  | Name     | Description   | Attribute | Reset |
|------|----------|---------------|-----------|-------|
| 31:0 | TC[31:0] | Timer Counter | R/W       | 0     |

### 9.7.3 CT32Bn Prescale register (CT32Bn\_PRE) (n=0,1,2)

Address Offset: 0x08

| Bit  | Name      | Description        | Attribute | Reset |
|------|-----------|--------------------|-----------|-------|
| 31:0 | PRE[31:0] | Prescale max value | R/W       | 0     |

### 9.7.4 CT32Bn Prescale Counter register (CT32Bn\_PC) (n=0,1,2)

Address Offset: 0x0C

The 32-bit Prescale Counter controls division of PCLK by some constant value before it is applied to the Timer Counter. This allows control of the relationship between the resolution of the timer and the maximum time before the timer overflows. The Prescale Counter is incremented on every PCLK. When it reaches the value stored in the Prescale Register, the Timer Counter is incremented, and the Prescale Counter is reset on the next PCLK. This causes the TC to increment on every PCLK when PR = 0, every 2 PCLKs when PR = 1, etc.

| Bit  | Name     | Description      | Attribute | Reset |
|------|----------|------------------|-----------|-------|
| 31:0 | PC[31:0] | Prescale Counter | R/W       | 0     |

### 9.7.5 CT32Bn Count Control register (CT32Bn\_CNTCTRL) (n=0,1,2)

Address Offset: 0x10

This register is used to select between Timer and Counter mode, and in Counter mode to select the pin and edges for counting.

When Counter Mode is chosen as a mode of operation, the CAP input (selected by CIS bits) is sampled on every rising edge of the PCLK clock. After comparing two consecutive samples of this CAP input, one of the following four events is recognized: rising edge, falling edge, either of edges or no changes in the level of the selected CAP input. Only if the identified event occurs, and the event corresponds to the one selected by CTM bits in this register, will the Timer Counter register be incremented.

Effective processing of the externally supplied clock to the counter has some limitations. Since two successive rising edges of the PCLK clock are used to identify only one edge on the CAP selected input, the frequency of the CAP input cannot exceed one half of the PCLK clock. Consequently, the duration of the HIGH/LOW levels on the same CAP input in this case cannot be shorter than  $1/(2 \times \text{PCLK})$ .

**\* Note: If Counter mode is selected in the CNTCTRL register, Capture Control (CAPCTRL) register must be programmed as 0x0.**

| Bit  | Name     | Description                                                                                                                                                                                                                        | Attribute | Reset |
|------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:4 | Reserved |                                                                                                                                                                                                                                    | R         | 0     |
| 3:2  | CIS[1:0] | Count Input Select.<br>In counter mode (when CTM[1:0] are not 00), these bits select which CAP pin is sampled for clocking.<br>00: CT32Bn_CAP0<br>Other: Reserved.                                                                 | R/W       | 0     |
| 1:0  | CTM[1:0] | Counter/Timer Mode.<br>This field selects which rising PCLK edges can clear PC and increment Timer Counter (TC).<br>00: Timer Mode: every rising PCLK edge<br>01: Counter Mode: TC is incremented on rising edges on the CAP input | R/W       | 0     |

|  |  |                                                                                                                                                                                                                  |  |  |
|--|--|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|
|  |  | selected by CIS bits.<br>10: Counter Mode: TC is incremented on falling edges on the CAP input selected by CIS bits.<br>11: Counter Mode: TC is incremented on both edges on the CAP input selected by CIS bits. |  |  |
|--|--|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|

### 9.7.6 CT32Bn Match Control register (CT32Bn\_MCTRL) (n=0,1,2)

Address Offset: 0x14

| Bit   | Name     | Description                                                                                                      | Attribute | Reset |
|-------|----------|------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:12 | Reserved |                                                                                                                  | R         | 0     |
| 11    | MR3STOP  | Stop MR3: TC will stop and CEN bit will be cleared if MR3 matches TC.<br>0: Disable<br>1: Enable                 | R/W       | 0     |
| 10    | MR3RST   | Enable reset TC when MR3 matches TC.<br>0: Disable<br>1: Enable                                                  | R/W       | 0     |
| 9     | MR3IE    | Enable generating an interrupt based on CM[2:0] when MR3 matches the value in the TC.<br>0: Disable<br>1: Enable | R/W       | 0     |
| 8     | MR2STOP  | Stop MR2: TC will stop and CEN bit will be cleared if MR2 matches TC.<br>0: Disable<br>1: Enable                 | R/W       | 0     |
| 7     | MR2RST   | Enable reset TC when MR2 matches TC.<br>0: Disable<br>1: Enable                                                  | R/W       | 0     |
| 6     | MR2IE    | Enable generating an interrupt based on CM[2:0] when MR2 matches the value in the TC.<br>0: Disable<br>1: Enable | R/W       | 0     |
| 5     | MR1STOP  | Stop MR1: TC will stop and CEN bit will be cleared if MR1 matches TC.<br>0: Disable<br>1: Enable                 | R/W       | 0     |
| 4     | MR1RST   | Enable reset TC when MR1 matches TC.<br>0: Disable<br>1: Enable                                                  | R/W       | 0     |
| 3     | MR1IE    | Enable generating an interrupt based on CM[2:0] when MR1 matches the value in the TC.<br>0: Disable<br>1: Enable | R/W       | 0     |
| 2     | MR0STOP  | Stop MR0: TC will stop and CEN bit will be cleared if MR0 matches TC.<br>0: Disable<br>1: Enable                 | R/W       | 0     |
| 1     | MR0RST   | Enable reset TC when MR0 matches TC.<br>0: Disable<br>1: Enable                                                  | R/W       | 0     |
| 0     | MR0IE    | Enable generating an interrupt based on CM[2:0] when MR0 matches the value in the TC.<br>0: Disable<br>1: Enable | R/W       | 0     |

### 9.7.7 CT32Bn Match register 0~3 (CT32Bn\_MR0~3) (n=0,1,2)

Address Offset: 0x18, 0x1C, 0x20, 0x24

The Match register values are continuously compared to the Timer Counter (TC) value. When the two values are equal, actions can be triggered automatically. The action possibilities are to generate an interrupt, reset the Timer Counter, or stop the timer. Actions are controlled by the settings in the CT32Bn\_MCTRL register.

| Bit  | Name     | Description               | Attribute | Reset |
|------|----------|---------------------------|-----------|-------|
| 31:0 | MR[31:0] | Timer counter match value | R/W       | 0     |

### 9.7.8 CT32Bn Capture Control register (CT32Bn\_CAPCTRL) (n=0,1,2)

Address Offset: 0x28

The Capture Control register is used to control whether the Capture register is loaded with the value in the Counter/timer when the capture event occurs, and whether an interrupt is generated by the capture event. Setting both the rising and falling bits at the same time is a valid configuration, resulting in a capture event for both edges.

**\* Note: HW will switch I/O Configuration directly when CAP0EN =1.**

| Bit  | Name     | Description                                                                                                                                                 | Attribute | Reset |
|------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:4 | Reserved |                                                                                                                                                             | R         | 0     |
| 3    | CAP0EN   | Capture 0 function enable bit<br>0: Disable<br>1: Enable..                                                                                                  | R/W       | 0     |
| 2    | CAP0IE   | Interrupt on CT32Bn_CAP0 event: a CAP0 load due to a CT32Bn_CAP0 event will generate an interrupt.<br>0: Disable<br>1: Enable                               | R/W       | 0     |
| 1    | CAP0FE   | Capture on CT32Bn_CAP0 falling edge: a sequence of 1 then 0 on CT32Bn_CAP0 will cause CAP0 to be loaded with the contents of TC.<br>0: Disable<br>1: Enable | R/W       | 0     |
| 0    | CAP0RE   | Capture on CT32Bn_CAP0 rising edge: a sequence of 0 then 1 on CT32Bn_CAP0 will cause CAP0 to be loaded with the contents of TC.<br>0: Disable<br>1: Enable  | R/W       | 0     |

### 9.7.9 CT32Bn Capture 0 register (CT32Bn\_CAP0) (n=0,1,2)

Address Offset: 0x2C

Each Capture register is associated with a device pin and may be loaded with the counter/timer value when a specified event occurs on that pin. The settings in the Capture Control register determine whether the capture function is enabled, and whether a capture event happens on the rising edge of the associated pin, the falling edge, or on both edges.

| Bit  | Name       | Description                 | Attribute | Reset |
|------|------------|-----------------------------|-----------|-------|
| 31:0 | CAP0[31:0] | Timer counter capture value | R         | 0     |

### 9.7.10 CT32Bn External Match register (CT32Bn\_EM) (n=0,1,2)

Address Offset: 0x30

The External Match register provides both control and status of the external match pins CT32Bn\_PWMCTRL[3:0]. If the match outputs are configured as PWM output, the function of the external match registers is determined by the [PWM rules](#).

| Bit   | Name      | Description                                                     | Attribute | Reset |
|-------|-----------|-----------------------------------------------------------------|-----------|-------|
| 31:12 | Reserved  |                                                                 | R         | 0     |
| 11:10 | EMC3[1:0] | Determines the functionality of CT32Bn_PWM3.<br>00: Do Nothing. | R/W       | 0     |

|            |           |                                                                                                                                                             |     |   |
|------------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---|
|            |           | 01: CT32Bn_PWM3 pin is LOW<br>10: CT32Bn_PWM3 pin is HIGH<br>11: Toggle CT32Bn_PWM3 pin.                                                                    |     |   |
| <b>9:8</b> | EMC2[1:0] | Determines the functionality of CT32Bn_PWM2.<br>00: Do Nothing.<br>01: CT32Bn_PWM2 pin is LOW<br>10: CT32Bn_PWM2 pin is HIGH<br>11: Toggle CT32Bn_PWM2 pin. | R/W | 0 |
| <b>7:6</b> | EMC1[1:0] | Determines the functionality of CT32Bn_PWM1.<br>00: Do Nothing.<br>01: CT32Bn_PWM1 pin is LOW<br>10: CT32Bn_PWM1 pin is HIGH.<br>11: Toggle CT32Bn_PWM1.    | R/W | 0 |
| <b>5:4</b> | EMC0[1:0] | Determines the functionality of CT32Bn_PWM0.<br>00: Do Nothing.<br>01: CT32Bn_PWM0 pin is LOW<br>10: CT32Bn_PWM0 pin is HIGH<br>11: Toggle CT32Bn_PWM0.     | R/W | 0 |
| <b>3</b>   | EM3       | When the TC and MR3 are equal, this bit will act according to EMC3 bits, and also drive the state of CT32Bn_PWM3 output.                                    | R/W | 0 |
| <b>2</b>   | EM2       | When the TC and MR2 are equal, this bit will act according to EMC2 bits, and also drive the state of CT32Bn_PWM2 output.                                    | R/W | 0 |
| <b>1</b>   | EM1       | When the TC and MR1 are equal, this bit will act according to EMC1 bits, and also drive the state of CT32Bn_PWM1 output.                                    | R/W | 0 |
| <b>0</b>   | EM0       | When the TC and MR0 are equal, this bit will act according to EMC0 bits, and also drive the state of CT32Bn_PWM0 output.                                    | R/W | 0 |

### 9.7.11 CT32Bn PWM Control register (CT32Bn\_PWMCTRL) (n=0,1,2)

Address Offset: 0x34

The PWM Control register is used to configure the match outputs as PWM outputs. Each match output can be independently set to perform either as PWM output or as match output whose function is controlled by [CT32Bn\\_EM](#) register.

For each timer, a maximum of three single edge controlled PWM outputs can be selected on the CT32Bn\_PWMCTRL[3:0] outputs. One additional match register determines the PWM cycle length. When a match occurs in any of the other match registers, the PWM output is set to HIGH. The timer is reset by the match register that is configured to set the PWM cycle length. When the timer is reset to zero, all currently HIGH match outputs configured as PWM outputs are cleared.

| Bit          | Name          | Description                                                                                                                                          | Attribute | Reset |
|--------------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:24</b> | Reserved      |                                                                                                                                                      | R         | 0     |
| <b>23</b>    | PWM3IOEN      | CT32Bn_PWM3/GPIO selection bit<br>0: CT32Bn_PWM3 pin act as GPIO<br>1: CT32Bn_PWM3 pin act as match output, and output signal depends on PWM3EN bit. | R/W       | 0     |
| <b>22</b>    | PWM2IOEN      | CT32Bn_PWM2/GPIO selection bit<br>0: CT32Bn_PWM2 pin act as GPIO<br>1: CT32Bn_PWM2 pin act as match output, and output signal depends on PWM2EN bit. | R/W       | 0     |
| <b>21</b>    | PWM1IOEN      | CT32Bn_PWM1/GPIO selection bit<br>0: CT32Bn_PWM1 pin act as GPIO<br>1: CT32Bn_PWM1 pin act as match output, and output signal depends on PWM1EN bit. | R/W       | 0     |
| <b>20</b>    | PWM0IOEN      | CT32Bn_PWM0/GPIO selection bit<br>0: CT32Bn_PWM0 pin act as GPIO<br>1: CT32Bn_PWM0 pin act as match output, and output signal depends on PWM0EN bit. | R/W       | 0     |
| <b>19:12</b> | Reserved      |                                                                                                                                                      | R         | 0     |
| <b>11:10</b> | PWM3MODE[1:0] | PWM3 output mode<br>00: PWM mode 1                                                                                                                   | R/W       | 0     |

|            |               |                                                                                                |     |   |
|------------|---------------|------------------------------------------------------------------------------------------------|-----|---|
|            |               | 01: PWM mode 2<br>10: Forced to 0.<br>11: Forced to 1.                                         |     |   |
| <b>9:8</b> | PWM2MODE[1:0] | PWM2 output mode<br>00: PWM mode 1<br>01: PWM mode 2<br>10: Forced to 0.<br>11: Forced to 1.   | R/W | 0 |
| <b>7:6</b> | PWM1MODE[1:0] | PWM1 output mode<br>00: PWM mode 1<br>01: PWM mode 2<br>10: Forced to 0.<br>11: Forced to 1.   | R/W | 0 |
| <b>5:4</b> | PWM0MODE[1:0] | PWM0 output mode<br>00: PWM mode 1<br>01: PWM mode 2<br>10: Forced to 0.<br>11: Forced to 1.   | R/W | 0 |
| <b>3</b>   | PWM3EN        | PWM3 enable<br>0: CT32Bn_PWM3 is controlled by EM3.<br>1: PWM mode is enabled for CT32Bn_PWM3. | R/W | 0 |
| <b>2</b>   | PWM2EN        | PWM2 enable<br>0: CT32Bn_PWM2 is controlled by EM2.<br>1: PWM mode is enabled for CT32Bn_PWM2. | R/W | 0 |
| <b>1</b>   | PWM1EN        | PWM1 enable<br>0: CT32Bn_PWM1 is controlled by EM1.<br>1: PWM mode is enabled for CT32Bn_PWM1. | R/W | 0 |
| <b>0</b>   | PWM0EN        | PWM0 enable<br>0: CT32Bn_PWM0 is controlled by EM0.<br>1: PWM mode is enabled for CT32Bn_PWM0. | R/W | 0 |

### 9.7.12 CT32Bn Timer Raw Interrupt Status register (CT32Bn\_RIS) (n=0,1,2)

Address Offset: 0x38

This register indicates the raw status for Timer/PWM interrupts. A Timer/PWM interrupt is sent to the interrupt controller if the corresponding bit in the CT16Bn\_IE register is set.

| Bit         | Name     | Description                                                                                                                    | Attribute | Reset |
|-------------|----------|--------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:5</b> | Reserved |                                                                                                                                | R         | 0     |
| <b>4</b>    | CAP0IF   | Interrupt flag for capture channel 0.<br>0: No interrupt on CAP0<br>1: Interrupt requirements met on CAP0.                     | R         | 0     |
| <b>3</b>    | MR3IF    | Interrupt flag for match channel 3.<br>0: No interrupt on match channel 3<br>1: Interrupt requirements met on match channel 3. | R         | 0     |
| <b>2</b>    | MR2IF    | Interrupt flag for match channel 2.<br>0: No interrupt on match channel 2<br>1: Interrupt requirements met on match channel 2. | R         | 0     |
| <b>1</b>    | MR1IF    | Interrupt flag for match channel 1.<br>0: No interrupt on match channel 1<br>1: Interrupt requirements met on match channel 1. | R         | 0     |
| <b>0</b>    | MR0IF    | Interrupt flag for match channel 0.<br>0: No interrupt on match channel 0<br>1: Interrupt requirements met on match channel 0. | R         | 0     |

**9.7.13 CT32Bn Timer Interrupt Clear register (CT32Bn\_IC) (n=0,1,2)**

Address Offset: 0x3C

| Bit         | Name     | Description                         | Attribute | Reset |
|-------------|----------|-------------------------------------|-----------|-------|
| <b>31:5</b> | Reserved |                                     | R         | 0     |
| <b>4</b>    | CAP0IC   | 0: No effect<br>1: Clear CAP0IF bit | W         | 0     |
| <b>3</b>    | MR3IC    | 0: No effect<br>1: Clear MR3IF bit  | W         | 0     |
| <b>2</b>    | MR2IC    | 0: No effect<br>1: Clear MR2IF bit  | W         | 0     |
| <b>1</b>    | MR1IC    | 0: No effect<br>1: Clear MR1IF bit  | W         | 0     |
| <b>0</b>    | MR0IC    | 0: No effect<br>1: Clear MR0IF bit  | W         | 0     |

# 10 WATCHDOG TIMER (WDT)

## 10.1 OVERVIEW

The purpose of the Watchdog is to reset the MCU within a reasonable amount of time if it enters an erroneous state. When enabled, the Watchdog will generate a system reset or interrupt if the user program fails to "feed" (or reload) the Watchdog within a predetermined amount of time.

The Watchdog consists of a divide by 128 fixed pre-scaler and an 8-bit counter. The clock is fed to the timer via a pre-scaler. The timer decrements when clocked. The minimum value from which the counter decrements is 0x01. Hence the minimum Watchdog interval is  $(T_{WDT\_PCLK} \times 128 \times 1)$  and the maximum Watchdog interval is  $(T_{WDT\_PCLK} \times 128 \times 256)$ .

The Watchdog should be used in the following manner:

1. Select the clock source for the watchdog timer with WDTCLKSEL register.
2. Set the prescale value for the watchdog clock with WDTPRE bits in [APB Clock Prescale register 1 \(SYS1\\_APBPCP1\)](#) register.
3. Set the Watchdog timer constant reload value in [WDT\\_TC](#) register.
4. Enable the Watchdog and setup the Watchdog timer operating mode in [WDT\\_CFG](#) register.
5. The Watchdog should be fed again by writing 0x55AA to [WDT\\_FEED](#) register before the Watchdog counter underflows to prevent reset or interrupt.

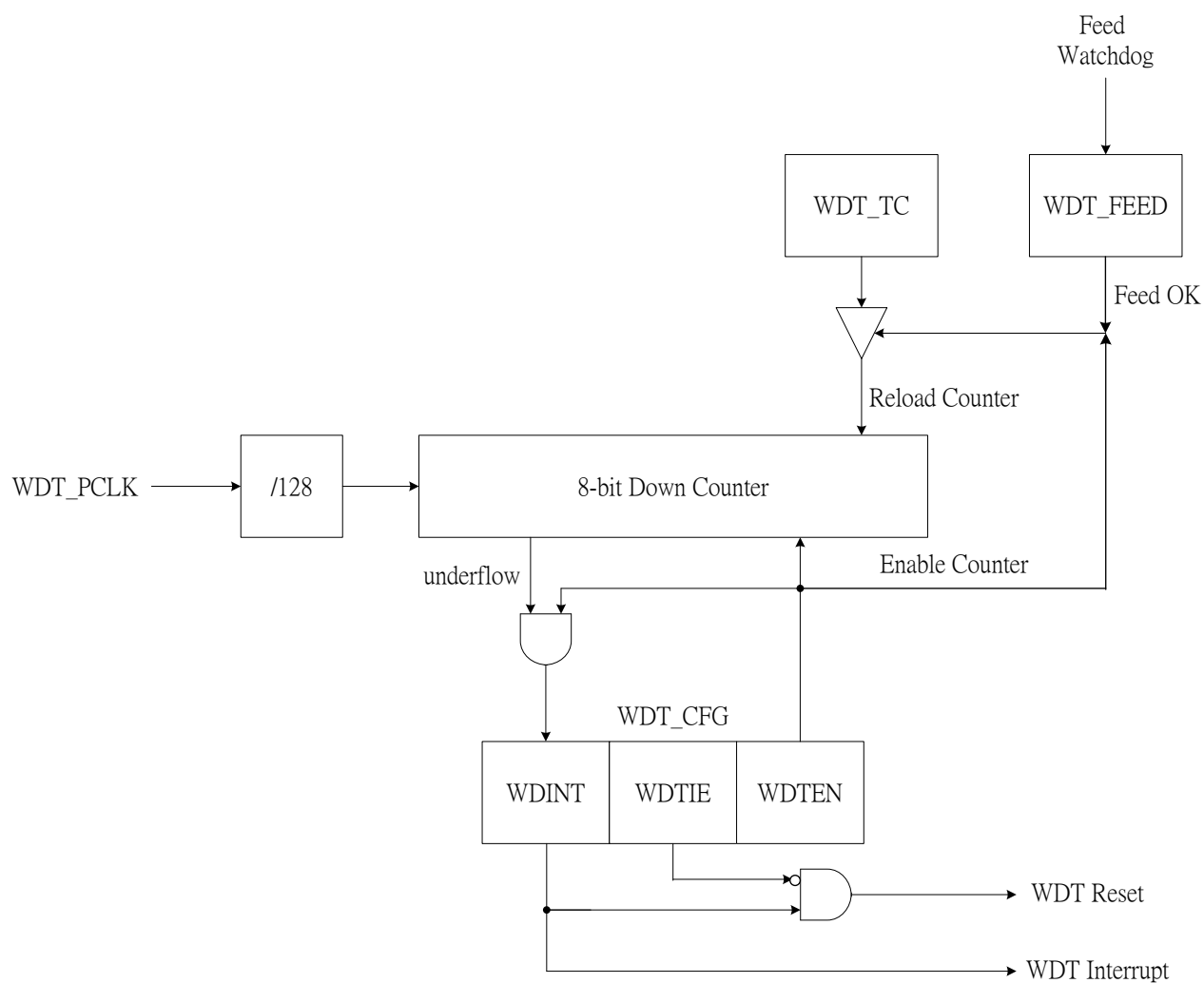
When the watchdog is started by setting the WDTEN in [WDT\\_CFG](#) register, the time constant value is loaded in the watchdog counter and the counter starts counting down. When the Watchdog is in the reset mode and the counter underflows, the CPU will be reset, loading the stack pointer and program counter from the vector table as in the case of external reset. Whenever the value 0x55AA is written in [WDT\\_FEED](#) register, the WDT\_TC value is reloaded in the watchdog counter and the watchdog reset or interrupt is prevented.

The watchdog timer block uses two clocks: HCLK and WDT\_PCLK. HCLK is used for the AHB accesses to the watchdog registers and is derived from the system clock. The WDT\_PCLK is used for the watchdog timer counting. Several clocks can be used as a clock source for WDT\_PCLK clock: IHRC, ILRC, ELS X'tal, and HCLK.

The clock to the watchdog register block can be disabled in [AHB Clock Enable register \(SYS1\\_AHBCLKEN\)](#) register for power savings.

Watchdog reset or interrupt will occur any time the watchdog is running and has an operating clock source.

## 10.2 BLOCK DIAGRAM



## 10.3 WDT REGISTERS

Base Address: 0x4001 0000

### 10.3.1 Watchdog Configuration register (WDT\_CFG)

Address Offset: 0x00

The WDT\_CFG register controls the operation of the Watchdog through the combination of WDTEN and WDTIE bits. This register indicates the raw status for Watchdog Timer interrupts. A WDT interrupt is sent to the interrupt controller if both the WDINT bit and the WDTIE bit are set.

| Bit   | Name     | Description                                                                                                                                                                                                                                                | Attribute | Reset |
|-------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:16 | WDKEY    | Watchdog register key.<br>Read as 0. When writing to the register you must write 0x5AFA to WDKEY, otherwise behavior of writing to the register is ignored.                                                                                                | W         | 0     |
| 15:3  | Reserved |                                                                                                                                                                                                                                                            | R         | 0     |
| 2     | WDINT    | Watchdog interrupt flag<br>0: Read→Watchdog does not cause an interrupt.<br>Writ→ Clear this flag. SW shall feed Watchdog before clearing.<br>1: Watchdog timeout and causes an interrupt (Only when WDTIE =1).                                            | R/W       | 0     |
| 1     | WDTIE    | Watchdog interrupt enable<br>0: Watchdog timeout will cause a chip reset. (Watchdog reset mode)<br>Watchdog counter underflow will reset the MCU, and will clear the WDINT flag.<br>1: Watchdog timeout will cause an interrupt. (Watchdog interrupt mode) | R/W       | 0     |
| 0     | WDTEN    | Watchdog enable<br>0: Disable<br>1: Enable. When enable the watchdog, the WDT_TC value is loaded in the watchdog counter.                                                                                                                                  | R/W       | 0     |

### 10.3.2 Watchdog Clock Source register (WDT\_CLKSOURCE)

Address Offset: 0x04

| Bit   | Name        | Description                                                                                                                                                 | Attribute | Reset |
|-------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:16 | WDKEY       | Watchdog register key.<br>Read as 0. When writing to the register you must write 0x5AFA to WDKEY, otherwise behavior of writing to the register is ignored. | W         | 0     |
| 15:2  | Reserved    |                                                                                                                                                             | R         | 0     |
| 1:0   | CLKSEL[1:0] | Selected Watchdog clock source.<br>00: IHRC oscillator<br>01: HCLK<br>10: ILRC oscillator<br>11: ELS X'TAL                                                  | R/W       | 0     |

### 10.3.3 Watchdog Timer Constant register (WDT\_TC)

Address Offset: 0x08

The WDT\_TC register determines the time-out value. Every time a feed sequence occurs the WDT\_TC content is reloaded in to the Watchdog timer. It's an 8-bit counter. Thus the time-out interval is  $T_{WDT\_PCLK} \times 128 \times 1 \sim T_{WDT\_PCLK} \times 128 \times 256$ .

Watchdog overflow time =  $(0.02\mu s \times 1) \times 128 \times 1 \sim (0.0625ms \times 32) \times 128 \times 256$   
= 2.56 $\mu s$  ~ 65536ms

| Bit | Name | Description | Attribute | Reset |
|-----|------|-------------|-----------|-------|
|-----|------|-------------|-----------|-------|

|              |          |                                                                                                                                                                                                                |     |      |
|--------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|
| <b>31:16</b> | WDKEY    | Watchdog register key.<br>Read as 0. When writing to the register you must write 0x5AFA to WDKEY, otherwise behavior of writing to the register is ignored.                                                    | W   | 0    |
| <b>15:8</b>  | Reserved |                                                                                                                                                                                                                | R   | 0    |
| <b>7:0</b>   | TC[7:0]  | Watchdog timer constant reload value = TC[7:0]+1<br>0000 0000 : Timer constant = 1<br>0000 0001 : Timer constant = 2<br>.....<br>.....<br>1111 1110 : Timer constant = 255<br>1111 1111 : Timer constant = 256 | R/W | 0xFF |

### 10.3.4 Watchdog Feed register (WDT\_FEED)

Address Offset: 0x0C

| Bit          | Name     | Description                                                                                                                                                 | Attribute | Reset |
|--------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:16</b> | WDKEY    | Watchdog register key.<br>Read as 0. When writing to the register you must write 0x5AFA to WDKEY, otherwise behavior of writing to the register is ignored. | W         | 0     |
| <b>15:0</b>  | FV[15:0] | Feed value (Read as 0x0)<br>0x55AA: The watchdog is fed, and the WDT_TC value is reloaded in the watchdog counter.                                          | W         | 0     |

# 11 REAL-TIME CLOCK (RTC)

## 11.1 OVERVIEW

The RTC is an independent timer. The RTC provides a set of continuously running counters which can be used to provide a clock-calendar function with suitable software.  
The counter values can be written to set the current time/date of the system.

## 11.2 FEATURES

- Programmable prescale value: division factor up to  $2^{20}$
- 32-bit programmable counter for long-term measurement
- The RTC clock source could be any of the following:
  - EHS XTAL clock divided by 128
  - ELS X'TA
  - ILRC
- Reset sources of the RTC Core (Prescale value, Alarm, Counter and Divider):
  - “Cold” boot
  - DPD\_WAKEUP
- Three dedicated enabled interrupt lines:
  - Alarm interrupt: generating a software programmable alarm interrupt.
  - Seconds interrupt: generating a periodic interrupt signal with a programmable period length (up to 1 second).
  - Overflow interrupt: to detect when the internal programmable counter rolls over to zero.

## 11.3 FUNCTIONAL DESCRIPTION

### 11.3.1 INTRODUCTION

RTC core includes a 20-bit preload value (RTC\_SECCNTV). Every TR\_CLK period, the RTC generates an interrupt (Second Interrupt) if it is enabled in [RTC\\_IE](#) register. The second block is a 32-bit programmable counter that can be initialized to the current system time. The system time is incremented at the TR\_CLK rate and compared with a programmable date (stored in the RTC\_ALR register) in order to generate an alarm interrupt, if enabled in [RTC\\_IE](#) register.

### 11.3.2 RTC FLAG ASSERTION

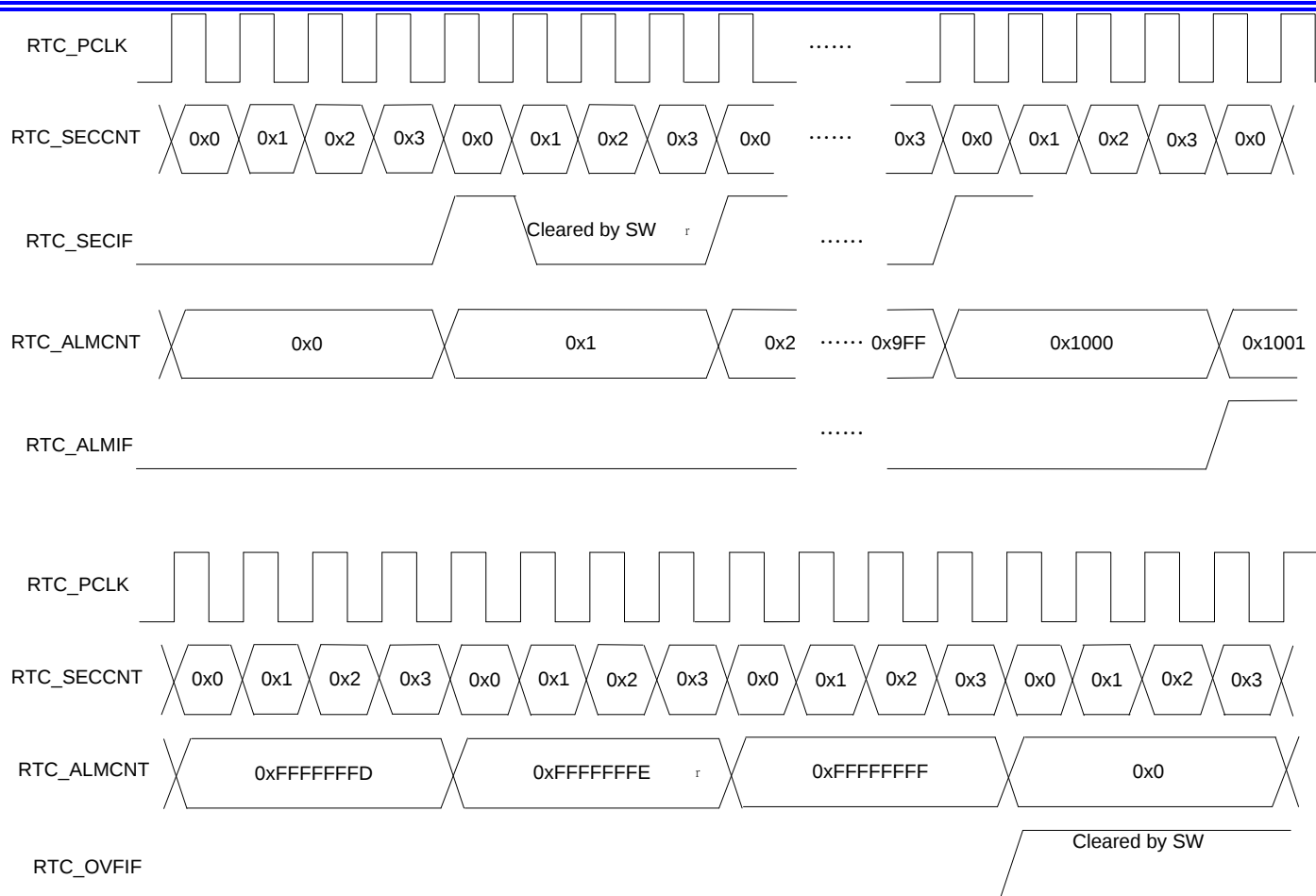
The RTC Second interrupt flag (SECIF) is asserted on each RTC Core clock cycle before the update of the RTC Counter.

The RTC Overflow interrupt flag (OVFIF) is asserted on the last RTC Core clock cycle before the counter reaches 0x0.

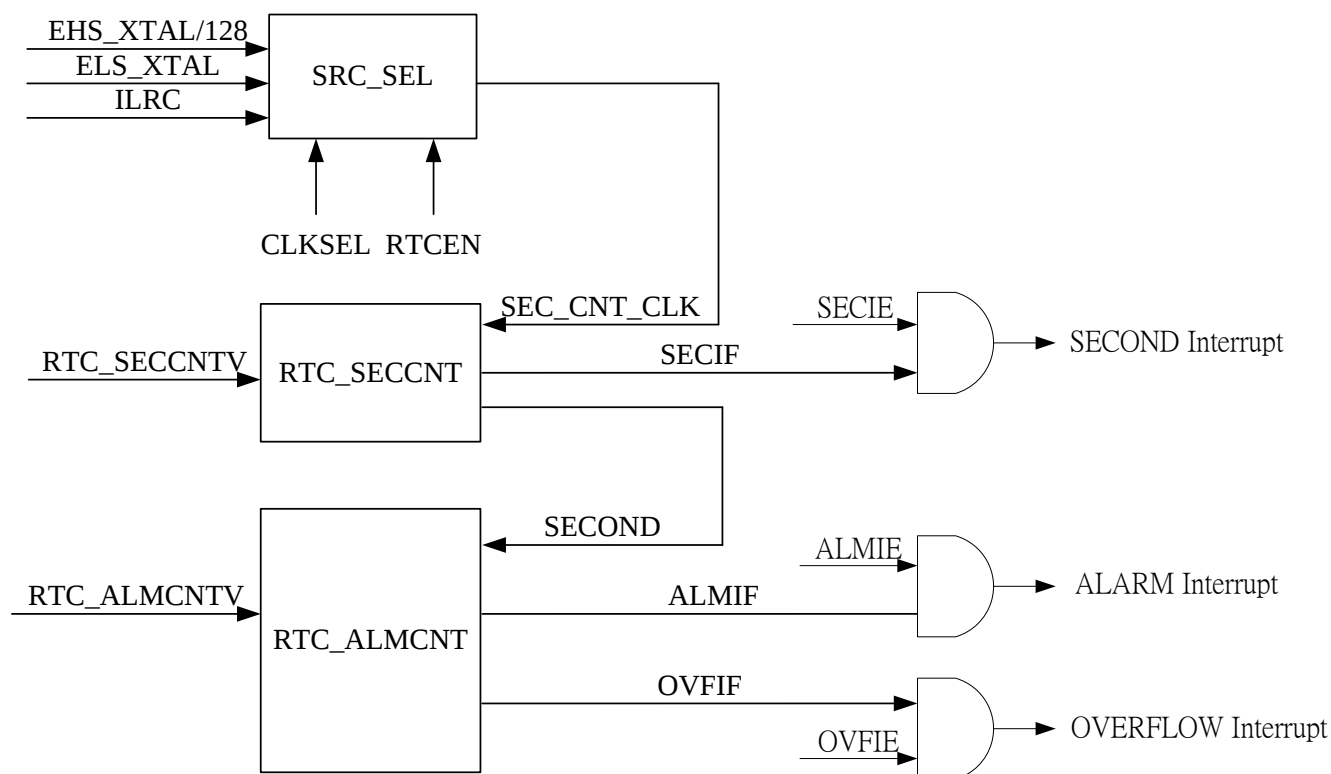
The RTC Alarm interrupt flag (ALMIF) are asserted on the last RTC Core clock cycle before the counter reaches the RTC Alarm counter reload value stored in the Alarm register.

### 11.3.3 RTC OPERATION

The following figure shows the RTC waveform when it is configured with RTC\_SECCNTV=3, RTC\_ALMCNTV=0x1000.



## 11.4 BLOCK DIAGRAM



## 11.5 RTC REGISTERS

Base Address: 0x4001 2000

### 11.5.1 RTC Control register (RTC\_CTRL)

Address offset: 0x00

\* **Note: RTCEN bit shall be set at last!**

| Bit  | Name     | Description                                                           | Attribute | Reset |
|------|----------|-----------------------------------------------------------------------|-----------|-------|
| 31:1 | Reserved |                                                                       | R         | 0     |
| 0    | RTCEN    | RTC enable bit<br>0: Disable<br>1: Enable. Reset SEC_CNT and ALM_CNT. | R/W       | 0     |

### 11.5.2 RTC Clock Source Select register (RTC\_CLKS)

Address offset: 0x04

\* **Note: SW shall disable RTC (RTCEN=0) when changing the value of this register.**

| Bit  | Name        | Description                                                                                                                                                         | Attribute | Reset |
|------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:2 | Reserved    |                                                                                                                                                                     | R         | 0     |
| 1:0  | CLKSEL[1:0] | RTC clock source selection.<br>HW will reset SEC_CNT and ALM_CNT when changing the value.<br>00: ILRC<br>01: ELS X'TAL<br>10: Reserved<br>11: EHS X'TAL clock / 128 | R/W       | 0     |

### 11.5.3 RTC Interrupt Enable register (RTC\_IE)

Address offset: 0x08

| Bit  | Name     | Description                                          | Attribute | Reset |
|------|----------|------------------------------------------------------|-----------|-------|
| 31:3 | Reserved |                                                      | R         | 0     |
| 2    | OVFIE    | Overflow interrupt enable<br>0: Disable<br>1: Enable | R/W       | 0     |
| 1    | ALMIE    | Alarm interrupt enable<br>0: Disable<br>1: Enable    | R/W       | 0     |
| 0    | SECIE    | Second interrupt enable<br>0: Disable<br>1: Enable   | R/W       | 0     |

### 11.5.4 RTC Raw Interrupt Status register (RTC\_RIS)

Address offset: 0x0C

| Bit  | Name     | Description                                                                                                                                                                                                                             | Attribute | Reset |
|------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:3 | Reserved |                                                                                                                                                                                                                                         | R         | 0     |
| 2    | OVFIF    | Overflow interrupt flag<br>This bit is set by HW when ALM_CNT overflows (ALM_CNT counts from 0xFFFFFFFF to 0x0). An interrupt is generated if OVFIE=1.<br>0: Overflow not detected<br>1: 32-bit programmable counter overflow occurred. | R         | 0     |
| 1    | ALMIF    | Alarm interrupt flag<br>This bit is set by HW when ALM_CNT=ALM_CNTV. An interrupt is generated if ALRIE=1.<br>0: Alarm not detected<br>1: Alarm detected.                                                                               | R         | 0     |
| 0    | SECIF    | Second interrupt flag<br>This bit is set by HW when SEC_CNT=SEC_CNTV. An interrupt is generated if SECIE=1.<br>0: Second flag condition not met.<br>1: Second flag condition met.                                                       | R         | 0     |

### 11.5.5 RTC Interrupt Clear register (RTC\_IC)

Address offset: 0x10

| Bit  | Name     | Description                        | Attribute | Reset |
|------|----------|------------------------------------|-----------|-------|
| 31:3 | Reserved |                                    | R         | 0     |
| 2    | OVFIC    | 0: No effect<br>1: Clear OVFIF bit | W         | 0     |
| 1    | ALMIC    | 0: No effect<br>1: Clear ALMIF bit | W         | 0     |
| 0    | SECIC    | 0: No effect<br>1: Clear SECIF bit | W         | 0     |

### 11.5.6 RTC Second Counter Reload Value register (RTC\_SECCNTV)

Address offset: 0x14

Reset value: 0x8000

| Bit   | Name          | Description                                                                                                                                                                                            | Attribute | Reset  |
|-------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|--------|
| 31:20 | Reserved      |                                                                                                                                                                                                        | R         | 0      |
| 19:0  | SECCNTV[19:0] | RTC second counter reload value.<br>Update this register will reset RTC_SECCNT and RTC_ALMCNT registers.<br>The zero value is not recommended, and will be replaced with default value (0x8000) by HW. | R/W       | 0x8000 |

### 11.5.7 RTC Second Count register (RTC\_SECCNT)

Address offset: 0x18

The RTC core has one 32-bit programmable counter, and this register keeps the current counting value of this counter.

| Bit  | Name         | Description                                                 | Attribute | Reset |
|------|--------------|-------------------------------------------------------------|-----------|-------|
| 31:0 | SECCNT[31:0] | RTC second counter<br>The current value of the RTC counter. | R         | 0     |

### 11.5.8 RTC Alarm Counter Reload Value register (RTC\_ALMCNTV)

Address offset: 0x1C

Reset value: 0xFFFFFFFF

| Bit  | Name          | Description                                                                                                                                                                  | Attribute | Reset      |
|------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|------------|
| 31:0 | ALMCNTV[31:0] | RTC alarm counter reload value.<br>Update this register will reset ALMCNT.<br>The zero value is not recommended, and will be replaced with default value (0xFFFFFFFF) by HW. | R/W       | 0xFFFFFFFF |

### 11.5.9 RTC Alarm Count register (RTC\_ALMCNT)

Address offset: 0x20

| Bit  | Name         | Description                                                      | Attribute | Reset |
|------|--------------|------------------------------------------------------------------|-----------|-------|
| 31:0 | ALMCNT[31:0] | RTC alarm counter<br>The current value of the RTC alarm counter. | R         | 0     |

# 12 SPI/SSP

## 12.1 OVERVIEW

The SSP is a Synchronous Serial Port controller capable of operation on a SPI, and 4-wire SSI bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of 4 to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice it is often the case that only one of these data flows carries meaningful data.

## 12.2 FEATURES

- Compatible with Motorola SPI, and 4-wire TI SSI bus.
- Synchronous Serial Communication.
- Supports master or slave operation.
- 8-frame FIFO for both transmitter and receiver.
- 4-bit to 16-bit frame.
- Maximum SPI speed of 25 Mbps (master) or 6 Mbps (slave) in SSP mode.
- Data transfer format is from MSB or LSB controlled by register.
- The start phase of data sampling location selection is 1<sup>st</sup>-phase or 2<sup>nd</sup>-phase controlled register.

## 12.3 PIN DESCRIPTION

| Pin Name          | Type | Description                              | GPIO Configuration                |
|-------------------|------|------------------------------------------|-----------------------------------|
| SCKn              | O    | SSP Serial clock (Master)                |                                   |
|                   | I    | SSP Serial clock (Slave)                 | Depends on GPIO <sub>n</sub> _CFG |
| SELn              | O    | SPI Slave Select/SSI Frame Sync (Master) |                                   |
|                   | I    | SSP Slave Select (Slave)                 | Depends on GPIO <sub>n</sub> _CFG |
| MISO <sub>n</sub> | I    | Master In Slave Out (Master)             | Depends on GPIO <sub>n</sub> _CFG |
|                   | O    | Master In Slave Out (Slave)              |                                   |
| MOSI <sub>n</sub> | O    | Master Out Slave In (Master)             |                                   |
|                   | I    | Master Out Slave In (Slave)              | Depends on GPIO <sub>n</sub> _CFG |

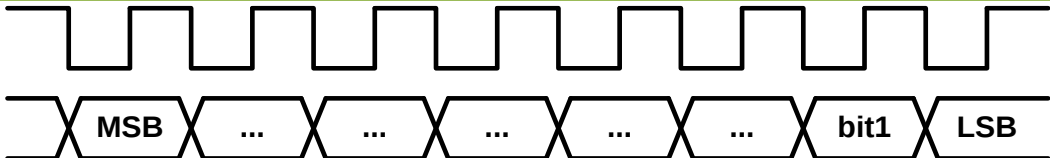
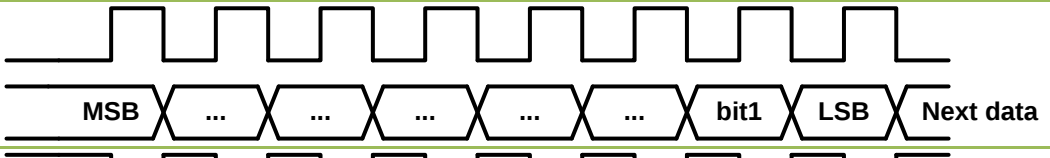
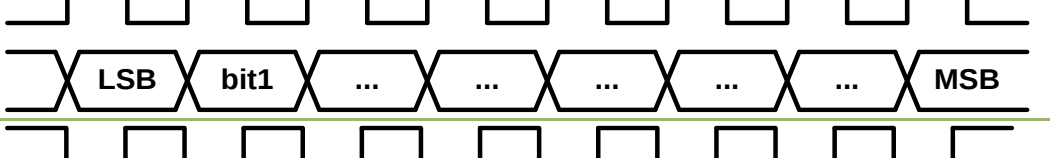
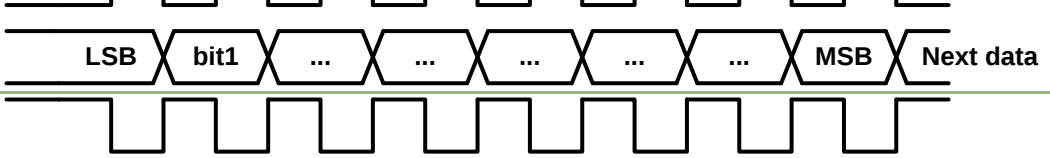
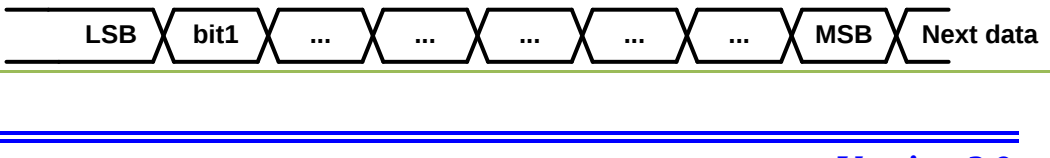
## 12.4 INTERFACE DESCRIPTION

### 12.4.1 SPI

The SPI interface is a 4-wire interface where the SEL signal behaves as a slave select. The main feature of the SPI format is that the inactive state and phase of the SCK signal are programmable through the CPOL and CPHA bits in [SSPn\\_CTRL1](#) register.

When the “CPOL” clock polarity control bit is LOW, it produces a steady state low value on the SCK pin. If the CPOL clock polarity control bit is HIGH, a steady state high value is placed on the CLK pin when data is not being transferred. The “CPHA” clock phase bit controls the phase of the clock on which data is sampled. When CPHA=1, the SCK first edge is for data transition, and receive and transmit data is at SCK 2<sup>nd</sup> edge. When CPHA=0, the 1<sup>st</sup> bit is fixed already, and the SCK first edge is to receive and transmit data.

The SPI data transfer timing as following figure:

| MLSB | CPOL | CPHA | SCK Idle Status | Diagrams                                                                             |
|------|------|------|-----------------|--------------------------------------------------------------------------------------|
| 0    | 0    | 1    | Low             |    |
| 0    | 1    | 1    | High            |   |
| 0    | 0    | 0    | Low             |  |
| 0    | 1    | 0    | High            |  |
| 1    | 0    | 1    | Low             |  |
| 1    | 1    | 1    | High            |  |
| 1    | 0    | 0    | Low             |  |
| 1    | 1    | 0    | High            |  |

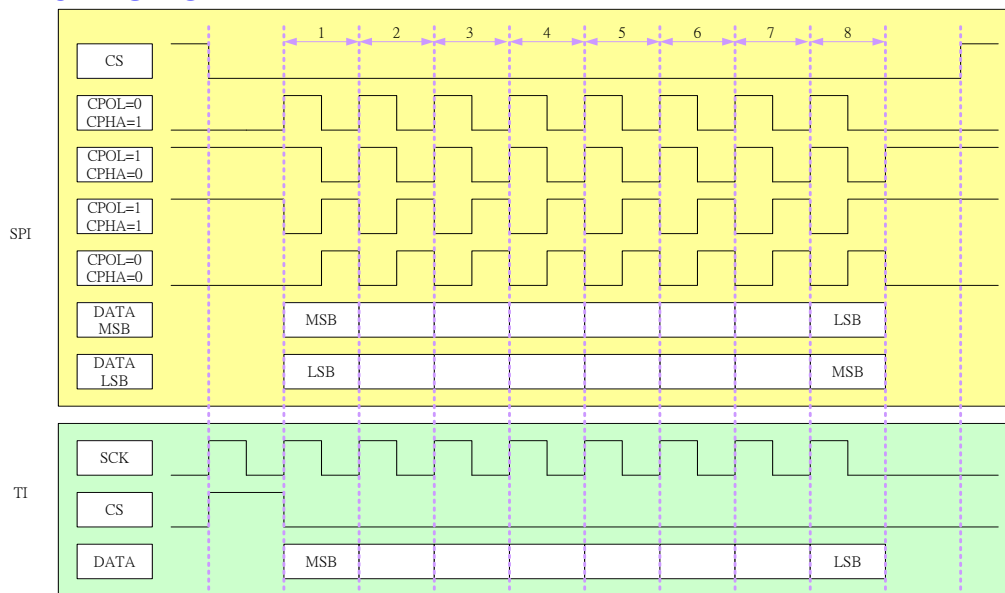
## 12.4.2 SSI

For device configured as a master in this mode, SCK and CS are forced LOW, and the transmit data line DX is in 3-state mode whenever the SSP hardware is idle.

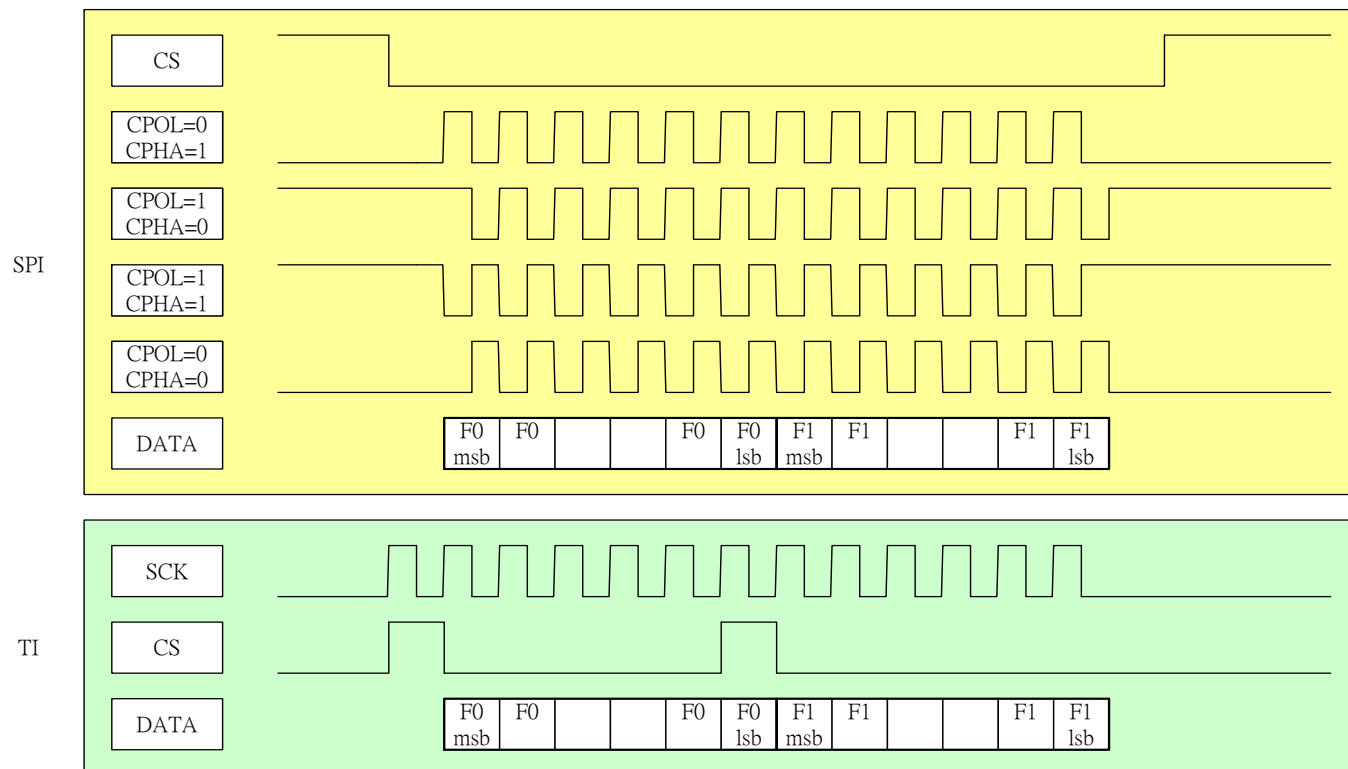
Once the bottom entry of the transmit FIFO contains data, CS is pulsed HIGH for one SCK period. The value to be transmitted is also transferred from the transmit FIFO to the serial shift register of the shifted out on the DX pin. Likewise, the MSB of the received data is shifted onto the DR pin by the off-chip serial slave device. Both the SSP hardware and the off-chip serial slave device then clock each data bit into their serial shifter on the falling edge of each SCK. The received data is transferred from the serial shifter to the receive FIFO on the first rising edge of SCK after the LSB has been latched.

## 12.4.3 COMMUNICATION FLOW

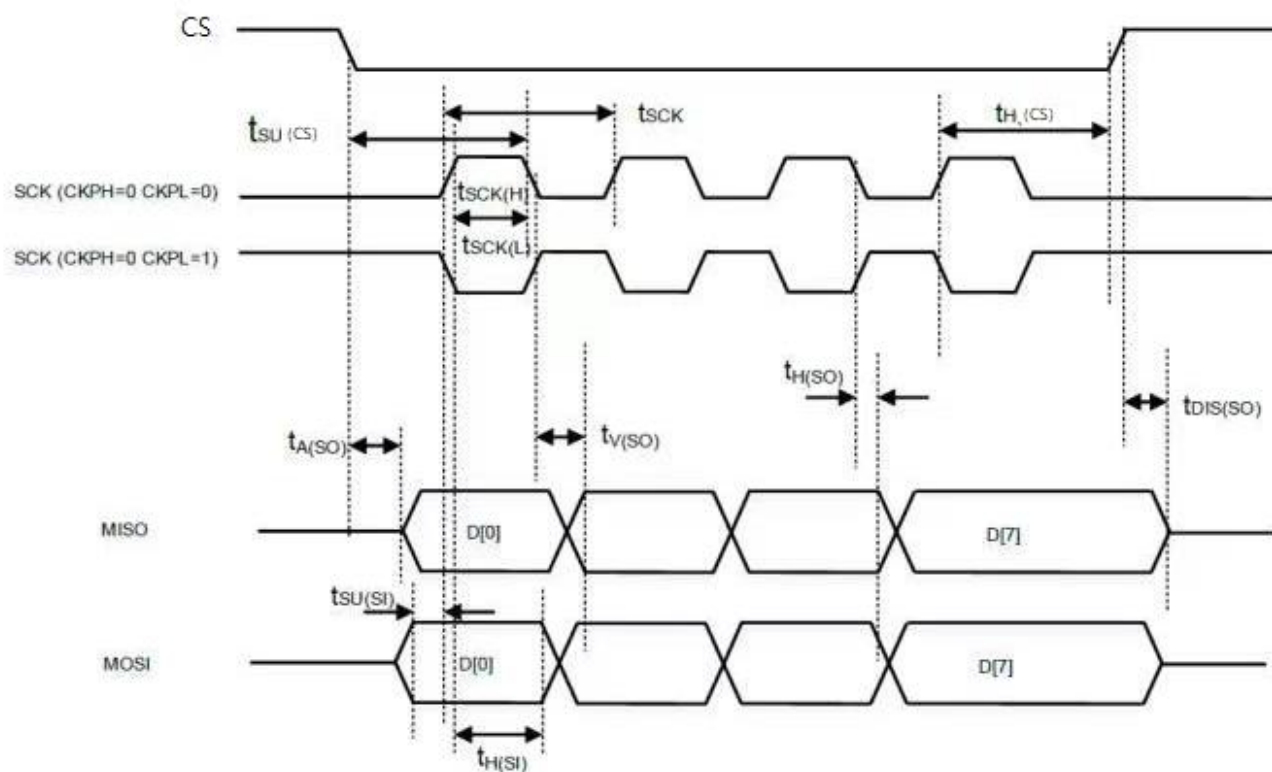
### 12.4.3.1 SINGLE-FRAME



### 12.4.3.2 MULTI-FRAME



## 12.5 TIMING CHARACTERISTICS



**Master Mode:**

| Symbol         | Parameter           | Min                 | Typ | Max | Unit |
|----------------|---------------------|---------------------|-----|-----|------|
| $t_{sck}$      | SCK out period      | 33                  |     |     | ns   |
| $t_{sck}(H)$   | SCK out high pulse  | $t_{sck} \cdot 0.4$ |     |     | ns   |
| $t_{sck}(L)$   | SCK out low pulse   | $t_{sck} \cdot 0.4$ |     |     | ns   |
| $t_{su}(CS)$   | CS out setup time   | $t_{sck} \cdot 2$   |     |     | ns   |
| $t_h(CS)$      | CS out hold time    | $t_{sck} \cdot 1.5$ |     |     | ns   |
| $t_{su}(MISO)$ | Data in setup time  | $t_{sck} \cdot 0.4$ |     |     | ns   |
| $t_h(MISO)$    | Data in hold time   | $t_{sck} \cdot 0.4$ |     |     | ns   |
| $t_{su}(MOSI)$ | Data out setup time | $t_{sck} \cdot 0.4$ |     |     | ns   |
| $t_h(MOSI)$    | Data out hold time  | $t_{sck} \cdot 0.4$ |     |     | ns   |

**Slave Mode:**

| Symbol         | Parameter           | Min                 | Typ | Max | Unit |
|----------------|---------------------|---------------------|-----|-----|------|
| $t_{sck}$      | SCK in period       | 33                  |     |     | ns   |
| $t_{sck}(H)$   | SCK in high pulse   | $t_{sck} \cdot 0.4$ |     |     | ns   |
| $t_{sck}(L)$   | SCK in low pulse    | $t_{sck} \cdot 0.4$ |     |     | ns   |
| $t_{su}(CS)$   | CS in setup time    | $t_{sck} \cdot 1.5$ |     |     | ns   |
| $t_h(CS)$      | CS in hold time     | $t_{sck}$           |     |     | ns   |
| $t_{su}(MISO)$ | Data out setup time | $t_{sck} \cdot 0.4$ |     |     | ns   |
| $t_h(MISO)$    | Data out hold time  | $t_{sck} \cdot 0.4$ |     |     | ns   |
| $t_{su}(MOSI)$ | Data in setup time  | $t_{sck} \cdot 0.4$ |     |     | ns   |
| $t_h(MOSI)$    | Data in hold time   | $t_{sck} \cdot 0.4$ |     |     | ns   |

## 12.6 AUTO-SEL

The Auto-SEL function is disabled (SELDIS = 1) by default, HW does NOT control SELn pin at all, and SELn pin is GPIO. If Auto-SEL function is enabled (SELDIS = 0), SPI HW controls the SELn activity, and SELn is assigned by [PFPA SSP](#) register.

## 12.7 SSP REGISTERS

Base Address: 0x4001 C000 (SSP0)  
0x4005 8000 (SSP1)

### 12.7.1 SSP n Control register 0 (SSPn\_CTRL0) (n=0,1)

Address Offset: 0x00

- \* Note:**
1. Must reset SSP FSM with FRESET[1:0] after changing any configuration of SSP when SSPEN = 1.
  2. HW will switch I/O configurations refer to FORMAT bit directly when SSPEN = 1.

| Bit   | Name          | Description                                                                                                                                                                                                                                                                                            | Attribute | Reset |
|-------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:19 | Reserved      |                                                                                                                                                                                                                                                                                                        | R         | 0     |
| 18    | SELDIS        | Auto-SEL disable bit. For SPI mode only.<br>0: Enable Auto-SEL flow control.<br>1: Disable Auto-SEL flow control.                                                                                                                                                                                      | R/W       | 1     |
| 17:15 | RXFIFOTH[2:0] | RX FIFO Threshold level<br>000: RX FIFO threshold level = 0<br>001: RX FIFO threshold level = 1<br>...<br>...<br>111: RX FIFO threshold level = 7                                                                                                                                                      | R/W       | 000b  |
| 14:12 | TXFIFOTH[2:0] | TX FIFO Threshold level<br>000: TX FIFO threshold level = 0<br>001: TX FIFO threshold level = 1<br>...<br>...<br>111: TX FIFO threshold level = 7                                                                                                                                                      | R/W       | 000b  |
| 11:8  | DL[3:0]       | Data length = DL[3:0] + 1<br>0000~0001: Reversed<br>0010: data length = 3<br>...<br>...<br>1110: data length = 15<br>1111: data length = 16                                                                                                                                                            | R/W       | 1111b |
| 7:6   | FRESET[1:0]   | SSP FSM and FIFO Reset bit<br>00: No effect<br>01: Reserved<br>10: Reserved<br>11: Reset finite state machine and FIFO. (BUF_BUSY = 0, data in shift BUF is cleared, TX_EMPTY = 1, TX_FULL = 0, RX_EMPTY = 1, RX_FULL = 0, and data in FIFO is cleared). This bit will be cleared by HW automatically. | W         | 0     |
| 5     | Reserved      |                                                                                                                                                                                                                                                                                                        | R         | 0     |
| 4     | FORMAT        | Interface format.<br>0: SPI<br>1: SSI                                                                                                                                                                                                                                                                  | R/W       | 0     |
| 3     | MS            | Master/Slave selection bit<br>0: Act as Master.<br>1: Act as Slave.                                                                                                                                                                                                                                    | R/W       | 0     |
| 2     | SDODIS        | Slave data output disable bit (ONLY used in slave mode)<br>0: Enable slave data output.<br>1: Disable slave data output. (MISO=0)                                                                                                                                                                      | R/W       | 0     |
| 1     | LOOPBACK      | Loop back mode enable<br>0: Disable<br>1: Data input from data output                                                                                                                                                                                                                                  | R/W       | 0     |
| 0     | SSPEN         | SSP enable bit                                                                                                                                                                                                                                                                                         | R/W       | 0     |

|  |  |                          |  |  |
|--|--|--------------------------|--|--|
|  |  | 0: Disable<br>1: Enable. |  |  |
|--|--|--------------------------|--|--|

### 12.7.2 SSP n Control register 1 (SSPn\_CTRL1) (n=0,1)

Address Offset: 0x04

| Bit         | Name     | Description                                                                                                                                                                                                                                                                                                                                                                | Attribute | Reset |
|-------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:3</b> | Reserved |                                                                                                                                                                                                                                                                                                                                                                            | R         | 0     |
| <b>2</b>    | CPHA     | Clock phase for edge sampling.<br>0: Data changes at clock falling edge, latches at clock rising edge when CPOL = 0; Data changes at clock rising edge, latches at clock falling edge when CPOL = 1.<br>1: Data changes at clock rising edge, latches at clock falling edge when CPOL = 0; Data changes at clock falling edge, latches at clock rising edge when CPOL = 1. | R/W       | 0     |
| <b>1</b>    | CPOL     | Clock polarity selection bit<br>0: SCK idles at Low level.<br>1: SCK idles at High level.                                                                                                                                                                                                                                                                                  | R/W       | 0     |
| <b>0</b>    | MLSB     | MSB/LSB selection bit<br>0: MSB transmit first.<br>1: LSB transmit first.                                                                                                                                                                                                                                                                                                  | R/W       | 0     |

### 12.7.3 SSP n Clock Divider register (SSPn\_CLKDIV) (n=0,1)

Address Offset: 0x08

| Bit         | Name     | Description                                                                                                                     | Attribute | Reset |
|-------------|----------|---------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:8</b> | Reserved |                                                                                                                                 | R         | 0     |
| <b>7:0</b>  | DIV[7:0] | SSPn clock divider<br>0: SCK = SSPn_PCLK / 2<br>1: SCK = SSPn_PCLK / 4<br>2: SCK = SSPn_PCLK / 6<br>X: SCK = SSPn_PCLK / (2X+2) | R/W       | 0     |

### 12.7.4 SSP n Status register (SSPn\_STAT) (n=0,1)

Address Offset: 0x0C

| Bit         | Name      | Description                                                                              | Attribute | Reset |
|-------------|-----------|------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:7</b> | Reserved  |                                                                                          | R         | 0     |
| <b>6</b>    | RXFIFOTHF | RX FIFO threshold flag<br>0: Data in RX FIFO ≤ RXFIFOTH<br>1: Data in RX FIFO > RXFIFOTH | R         | 0     |
| <b>5</b>    | TXFIFOTHF | TX FIFO threshold flag<br>0: Data in TX FIFO > TXFIFOTH<br>1: Data in TX FIFO ≤ TXFIFOTH | R         | 1     |
| <b>4</b>    | BUSY      | Busy flag.<br>0: SSP controller is idle.<br>1: SSP controller is transferring.           | R         | 0     |
| <b>3</b>    | RX_FULL   | RX FIFO full flag.<br>0: RX FIFO is NOT full.<br>1: RX FIFO is full.                     | R         | 0     |
| <b>2</b>    | RX_EMPTY  | RX FIFO empty flag<br>0: RX FIFO is NOT empty.<br>1: RX FIFO is empty.                   | R         | 1     |
| <b>1</b>    | TX_FULL   | TX FIFO full flag.<br>0: TX FIFO is NOT full.<br>1: TX FIFO is full.                     | R         | 0     |

|          |                 |                                                                                                                                              |          |          |
|----------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------|----------|----------|
| <b>0</b> | <b>TX_EMPTY</b> | TX FIFO empty flag<br>0: TX FIFO is NOT empty. In Master mode, the transmitter will begin to transmit automatically.<br>1: TX FIFO is empty. | <b>R</b> | <b>1</b> |
|----------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------|----------|----------|

### 12.7.5 SSP n Interrupt Enable register (SSPn\_IE) (n=0,1)

Address Offset: 0x10

This register controls whether each of the four possible interrupt conditions in the SSP controller is enabled.

| Bit         | Name       | Description                                                   | Attribute | Reset |
|-------------|------------|---------------------------------------------------------------|-----------|-------|
| <b>31:4</b> | Reserved   |                                                               | R         | 0     |
| <b>3</b>    | TXFIFOTHIE | TX FIFO threshold interrupt enable<br>0: Disable<br>1: Enable | R/W       | 0     |
| <b>2</b>    | RXFIFOTHIE | RX FIFO threshold interrupt enable<br>0: Disable<br>1: Enable | R/W       | 0     |
| <b>1</b>    | RXTOIE     | RX time-out interrupt enable<br>0: Disable<br>1: Enable       | R/W       | 0     |
| <b>0</b>    | RXOVFIE    | RX Overflow interrupt enable<br>0: Disable<br>1: Enable       | R/W       | 0     |

### 12.7.6 SSP n Raw Interrupt Status register (SSPn\_RIS) (n=0,1)

Address Offset: 0x14

This register contains the status for each interrupt condition, regardless of whether or not the interrupt is enabled in SSPn\_IE register.

This register indicates the status for SSP control raw interrupts. An SSP interrupt is sent to the interrupt controller if the corresponding bit in the SSPn\_IE register is set.

| Bit         | Name       | Description                                                                                                                                                                                                                                                            | Attribute | Reset |
|-------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:4</b> | Reserved   |                                                                                                                                                                                                                                                                        | R         | 0     |
| <b>3</b>    | TXFIFOTHIF | TX FIFO threshold interrupt flag<br>0: No TX FIFO threshold interrupt<br>1: TX FIFO threshold triggered.                                                                                                                                                               | R         | 0     |
| <b>2</b>    | RXFIFOTHIF | RX FIFO threshold interrupt flag<br>0: No RX FIFO threshold interrupt<br>1: RX FIFO threshold triggered.                                                                                                                                                               | R         | 0     |
| <b>1</b>    | RXTOIF     | RX time-out interrupt flag<br>RXTO occurs when the RX FIFO is not empty, and has not been read for a time-out period (32*SSPn_PCLK). The time-out period is the same for master and slave modes.<br>0: RXTO doesn't occur.<br>1: RXTO occurs.                          | R         | 0     |
| <b>0</b>    | RXOVFIF    | RX Overflow interrupt flag<br>RXOVF occurs when the RX FIFO is full and another frame is completely received. The ARM spec implies that the preceding frame data is overwritten by the new frame data when this occurs.<br>0: RXOVF doesn't occur.<br>1: RXOVF occurs. | R         | 0     |

### 12.7.7 SSP n Interrupt Clear register (SSPn\_IC) (n=0,1)

Address Offset: 0x18

| Bit  | Name       | Description                             | Attribute | Reset |
|------|------------|-----------------------------------------|-----------|-------|
| 31:4 | Reserved   |                                         | R         | 0     |
| 3    | TXFIFOTHIC | 0: No effect<br>1: Clear TXFIFOTHIF bit | W         | 0     |
| 2    | RXFIFOTHIC | 0: No effect<br>1: Clear RXFIFOTHIF bit | W         | 0     |
| 1    | RXTOIC     | 0: No effect<br>1: Clear RXTOIF bit.    | W         | 0     |
| 0    | RXOVFIC    | 0: No effect<br>1: Clear RXOVFIF bit.   | W         | 0     |

### 12.7.8 SSP n Data register (SSPn\_DATA) (n=0,1)

Address Offset: 0x1C

| Bit   | Name       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Attribute | Reset |
|-------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:16 | Reserved   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | R         | 0     |
| 15:0  | DATA[15:0] | <p><u>Write</u></p> <p>SW can write data to be sent in a future frame to this register when TX_FULL = 0 in <a href="#">SSPn_STAT</a> register (TX FIFO is not full). If the TX FIFO was previously empty and the SSP controller is not busy on the bus, transmission of the data will begin immediately. Otherwise the data written to this register will be sent as soon as all previous data has been sent (and received).</p> <p><u>Read</u></p> <p>SW can read data from this register when RX_EMPTY=0 in <a href="#">SSPn_STAT</a> register (Rx FIFO is not empty). When SW reads this register, the SSP controller returns data from the least recent frame in the RX FIFO. If the data length is less than 16 bit, the data is right-justified in this field with higher order bits filled with 0s.</p> | R/W       | 0     |

### 12.7.9 SSP n Data Fetch register (SSPn\_DF) (n=0,1)

Address Offset: 0x20

| Bit  | Name     | Description                                                                      | Attribute | Reset |
|------|----------|----------------------------------------------------------------------------------|-----------|-------|
| 31:1 | Reserved |                                                                                  | R         | 0     |
| 0    | DF       | SSP data fetch control bit<br>0: Disable<br>1: Enable when SCKn frequency > 6MHz | R/W       | 0     |

# 13 I2C

## 13.1 OVERVIEW

The I2C bus is bidirectional for inter-IC control using only two wires: Serial Clock Line (SCL) and Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I2C is a multi-master bus and can be controlled by more than one bus master connected to it. It is also SMBus 2.0 compatible.

The I2C interface is byte oriented and has four operating modes:

- Master transmitter mode
- Master receiver mode
- Slave transmitter mode
- Slave receiver mode

## 13.2 FEATURES

The I2C interface complies with the entire I2C specification, supporting the ability to turn power off to the ARM Cortex-M0 without interfering with other devices on the same I2C-bus.

- Standard I2C-compliant bus interfaces may be configured as Master or Slave.
- I2C Master features:
  - Clock generation
  - Start and Stop generation
- I2C Slave features:
  - Programmable I2C Address detection
  - Optional recognition of up to four distinct slave addresses
  - Stop bit detection
- Supports different communication speeds:
  - Standard Speed (up to 100KHz)
  - Fast Speed (up to 400 KHz)
- Arbitration is handled between simultaneously transmitting masters without corruption of serial data on the bus.
- Programmable clock allows adjustment of I2C transfer rates.
- Data transfer is bidirectional between masters and slaves.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization is used as a handshake mechanism to suspend and resume serial transfer.
- Monitor mode allows observing all I2C-bus traffic, regardless of slave address.
- I2C-bus can be used for test and diagnostic purposes.
- Generation and detection of 7-bit/10-bit addressing and General Call.

## 13.3 PIN DESCRIPTION

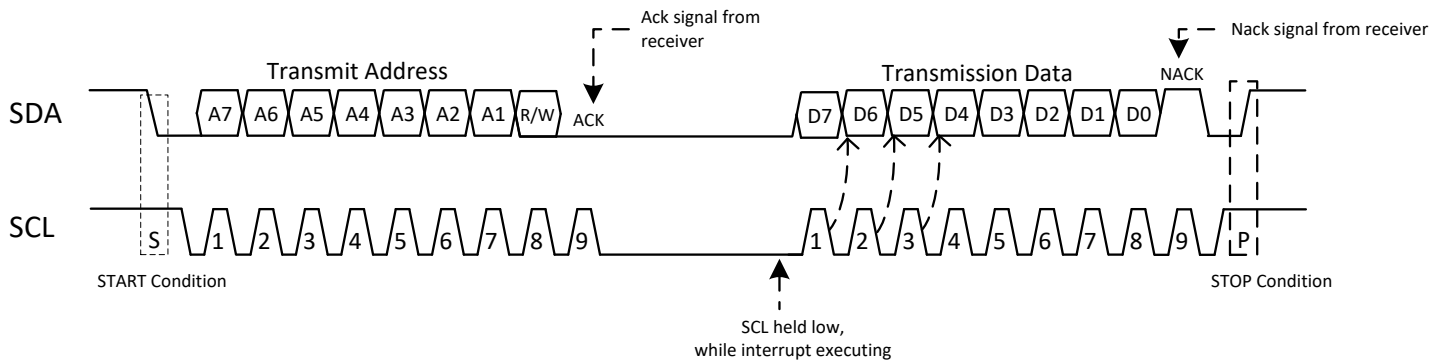
| Pin Name | Type | Description      | GPIO Configuration                                                |
|----------|------|------------------|-------------------------------------------------------------------|
| SCLn     | I/O  | I2C Serial clock | Output with Open-drain<br>Input depends on GPIO <sub>n</sub> _CFG |
| SDAn     | I/O  | I2C Serial data  | Output with Open-drain<br>Input depends on GPIO <sub>n</sub> _CFG |

## 13.4 I2C PROTOCOL

I2C transmission structure includes a START(S) condition, 8-bit address byte, one or more data byte and a STOP (P) condition. START condition is generated by master to initial any transmission.

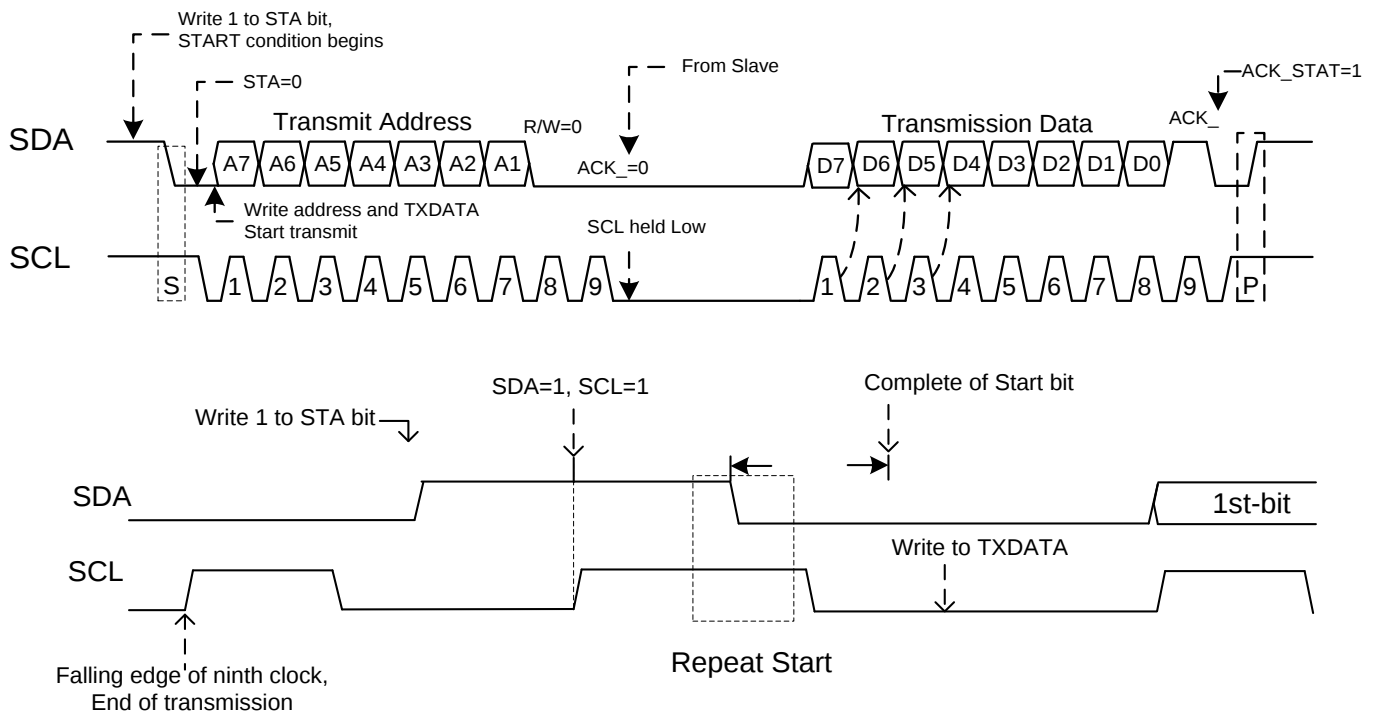
Data is transmitted with the Most Significant Bit (MSB) first. In address byte, the higher 7-bit is address bit and the lowest bit is data direction (R/W) bit. When R/W=0, it assigns a “WRITE” operation. When R/W=1, it assigns a “READ” operation.

After each byte is received, the receiver (a master or a slave) must send an acknowledge (ACK) bit. If transmitter can't receive an ACK, it will recognize a not acknowledge (NACK). In WRITE operation, the master will transmit data to the slave and then waits for ACK from slave. In READ operation, the slave will transmit data to the master and then waits for ACK from master. In the end, the master will generate a STOP condition to finish transmission.

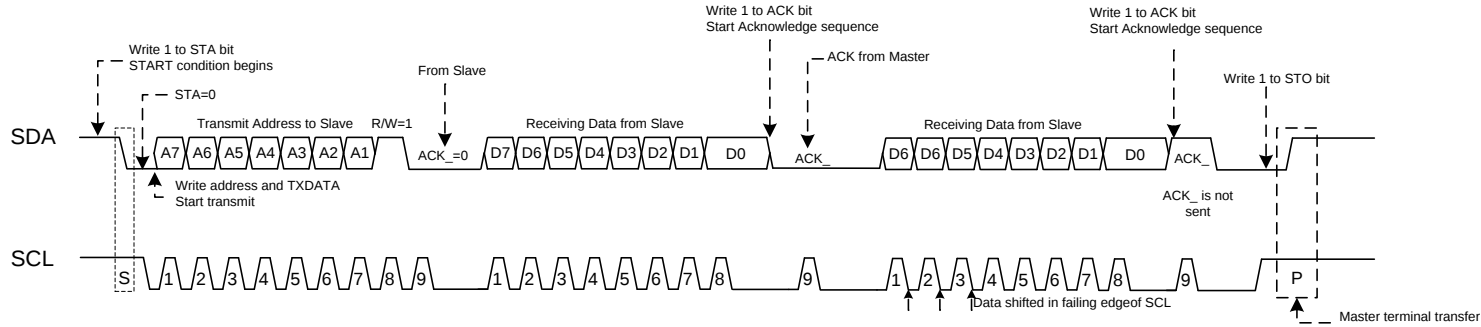


### 13.4.1 7-BIT ADDRESSING MODES

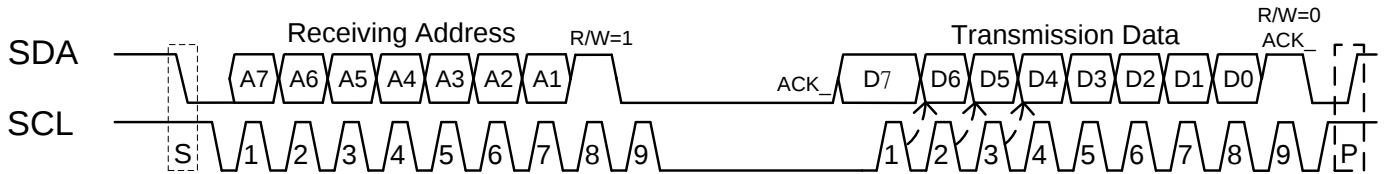
#### 13.4.1.1 MASTER TRANSMITTER MODE



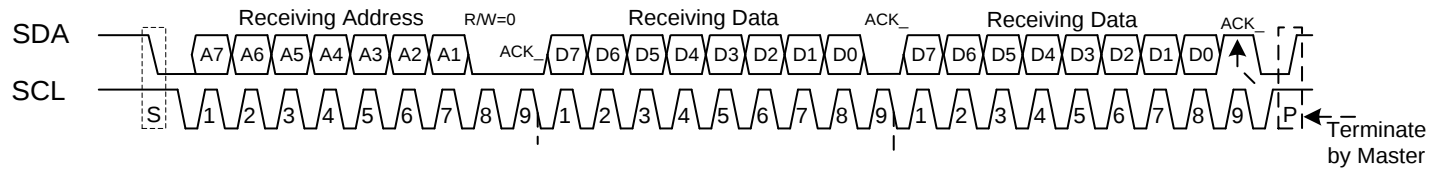
### 13.4.1.2 MASTER RECEIVER MODE



### 13.4.1.3 SLAVE TRANSMITTER MODE

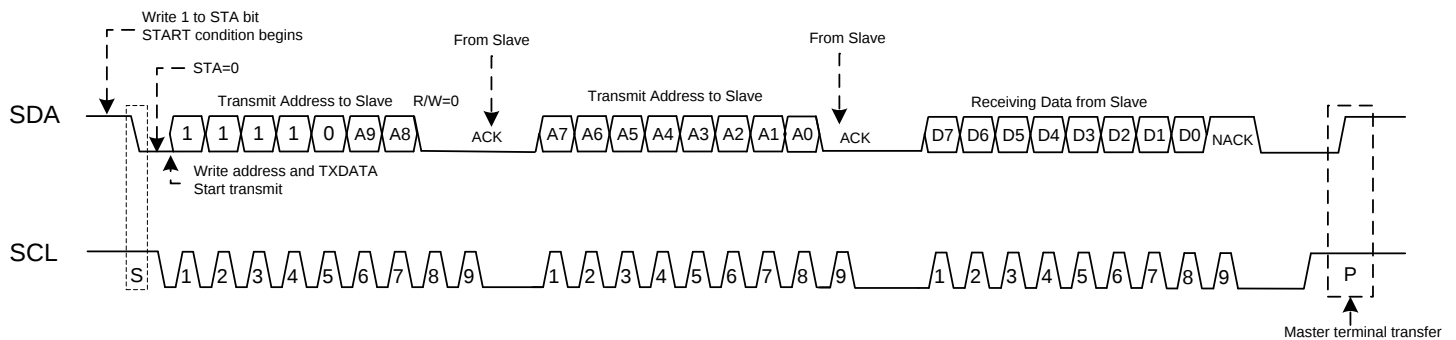


### 13.4.1.4 SLAVE RECEIVER MODE

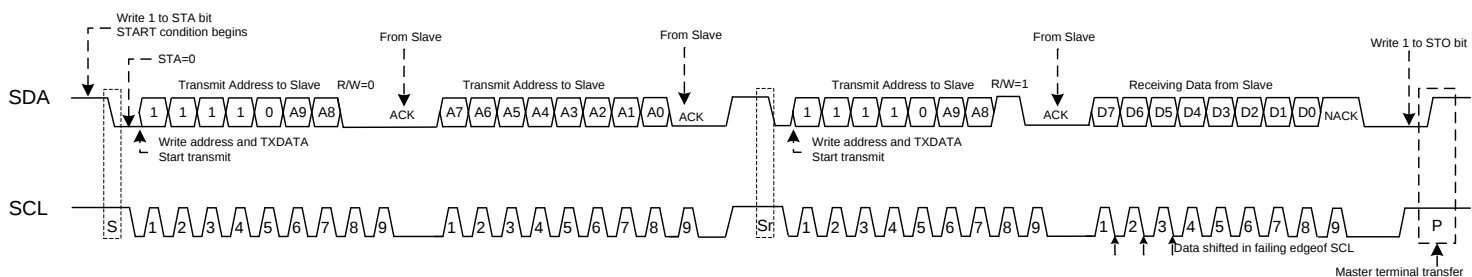


## 13.4.2 10-BIT ADDRESSING MODES

### 13.4.2.1 MASTER TRANSMITTER MODE



### 13.4.2.2 MASTER RECEIVER MODE



## 13.5 ARBITRATION

In multi-master condition, more than one master may transmit on bus in the same time. It must be decided which master has the control of bus and complete its transmission. Clock synchronization and arbitration are used to configure multi-master transmission.

Clock synchronization is executed by synchronizing the SCL signal with another devices. When two masters want to transmit data in the same time, the clock synchronization will start by the High to Low transition on the SCL. If master 1 pulls the SCL line LOW first, it holds the SCL in LOW status until the SCL line is released to HIGH status. However, if another master still pulls the SCL line LOW, the SCL Low to High transition of master 1 may not change SCL status (SCL line is still LOW). The SCL will transit from LOW to HIGH when the all masters release the SCL line. In the duration, the master1 will wait for SCL transition from LOW to HIGH, and then continue its transmission.

After clock synchronization, the clock of all devices is synchronized with the SCL clock. Arbitration is used to decide which master can complete its transmission by SDA signal. Two masters may send out a START condition and transmit data on bus in the same time, and may be influenced by each other. Arbitration will force one master to lose the control on bus. Data transmission will keep until two masters output different data signal. If one master transmits HIGH status and another master transmits LOW status, the SDA will be pulled low. The master which pulls the SDA line High will detect the different with SDA and loses the control on bus. The master which pulls the SDA line LOW status wins the bus control and continues its transmission. There is no data miss during arbitration.

Arbitration may also be lost in the master receiver mode. Loss of arbitration in this mode can only occur while the I2C block is returning a “not acknowledge” to the bus. Arbitration is lost when another device on the bus pulls this signal low. Since this can occur only at the end of a serial byte, the I2C block generates no further clock pulses.

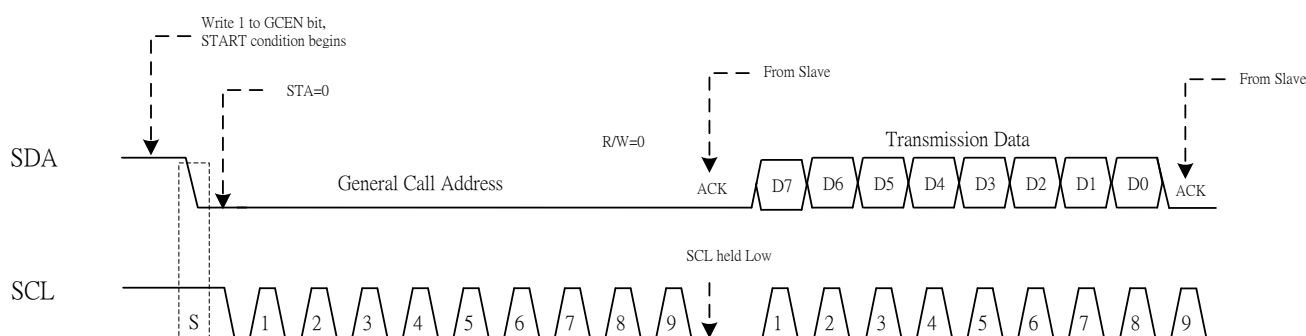
## 13.6 CLOCK STRETCHING

Clock stretching pauses a transaction by pulling the SCL line LOW. The transaction cannot continue until the line is released HIGH again. Clock stretching is optional.

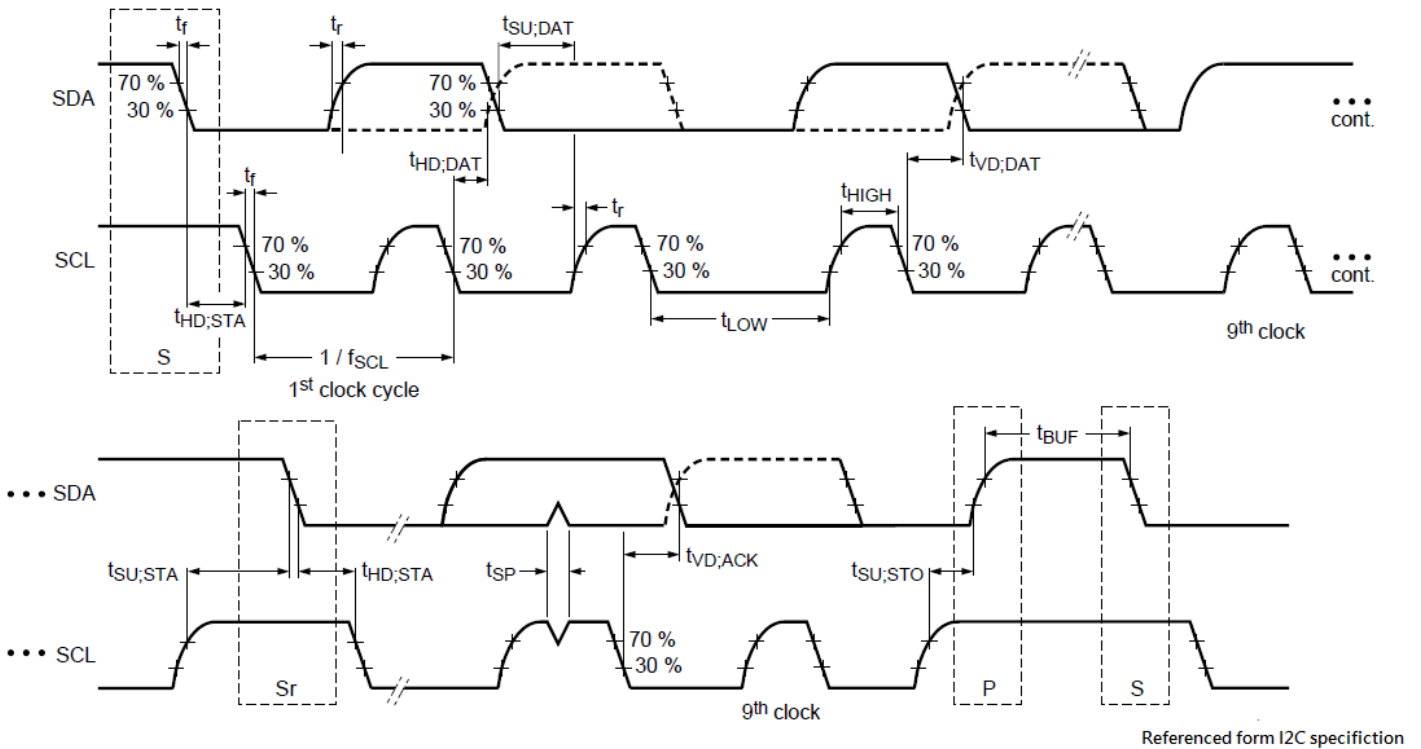
On the byte level, a device may be able to receive bytes of data at a fast rate, but needs more time to store a received byte or prepare another byte to be transmitted. Slaves can then pull the SCL line LOW after reception and acknowledgment of a byte to force the master into a wait state until the slave is ready for the next byte transfer in a type of handshake procedure.

## 13.7 GENERAL CALL ADDRESS

The general call address is a special address which is reserved as all “0” of 7-bit address and is for addressing every device connected to the I2C-bus at the same time. However, if a device does not need any of the data supplied within the general call structure, it can ignore this address by not issuing an acknowledgment (ACK). If a device does require data from a general call address, it acknowledges this address and behaves as a slave-receiver. The master does not actually know how many devices acknowledged if one or more devices respond. The second and following bytes are acknowledged by every slave-receiver capable of handling this data. A slave who cannot process one of these bytes must ignore it by not-acknowledging. If one or more slaves acknowledge, the not-acknowledge will not be seen by the master. The meaning of the general call address is specified in the second byte.



## 13.8 TIMING CHARACTERISTICS



### 13.8.1 MASTER TRANSMITTER MODE

- $t_{HIGH}$ :  $(SCLHT + 1) * I2C\_PCLK$  cycle
- $t_{LOW}$ :  $(SCLLT + 1) * I2C\_PCLK$  cycle
- $t_{HD;STA}$ :  $(SCLLT + 4) * I2C\_PCLK$  cycle
- $t_{HD;DAT}$ :  $2 * I2C\_PCLK$  cycle ~  $3 * I2C\_PCLK$  cycle
- $t_{SU;STA}$ :  $(SCLL + 3) * I2C\_PCLK$  cycle
- $t_{SU;STO}$ :  $(SCLLT + 2) * I2C\_PCLK$  cycle ~  $(SCLLT + 3) * I2C\_PCLK$  cycle

### 13.8.2 SLAVE TRANSMITTER MODE

- $t_{HIGH}$ : controlled by Master
- $t_{LOW}$ : controlled by Master
- $t_{HD;DAT}$ :  $2 * I2C\_PCLK$  cycle ~  $3 * I2C\_PCLK$  cycle
- $t_{SU;DAT}$ :  $t_{LOW} - 2 * I2C\_PCLK$  cycle ~  $t_{LOW} - 3 * I2C\_PCLK$  cycle

## **13.9 MONITOR MODE**

### **13.9.1 INTERRUPT**

All interrupts will occur as normal when the module is in monitor mode. This means that the first interrupt will occur when an address-match is detected (any address received if the MATCH\_ALL bit is set, otherwise an address matching one of the four address registers).

Subsequent to an address-match detection, interrupts will be generated after each data byte is received for a slave-write transfer, or after each byte that the module “thinks” it has transmitted for a slave-read transfer. In this second case, the data register will actually contain data transmitted by some other slave on the bus which was actually addressed by the master.

Following all of these interrupts, the processor may read the data register to see what was actually transmitted on the bus.

### **13.9.2 LOSS of ARBITRATION**

In monitor mode, the I2C module will not be able to respond to a request for information by the bus master or issue an ACK). Some other slave on the bus will respond instead. This will most probably result in a lost-arbitration state as far as our module is concerned. Software should be aware of the fact that the module is in monitor mode and should not respond to any loss of arbitration state that is detected. In addition, hardware may be designed into the module to block some/all loss of arbitration states from occurring if those state would either prevent a desired interrupt from occurring or cause an unwanted interrupt to occur. Whether any such hardware will be added is still to be determined.

## 13.10 I2C REGISTERS

Base Address: 0x4001 8000 (I2C0)  
0x4005 A000 (I2C1)

### 13.10.1 I2C n Control register (I2Cn\_CTRL) (n=0,1)

Address Offset: 0x00

Setting of the bits in this register controls operation of the I2C interface.

When STA =1 and the I2C interface is not already in master mode, it enters master mode, checks the bus and generates a START condition if the bus is free. If the bus is not free, it waits for a STOP condition (which will free the bus) and generates a START condition after a delay of a half clock period of the internal clock generator. If the I2C interface is already in master mode and data has been transmitted or received, it transmits a Repeated START condition. STA may be set at any time, including when the I2C interface is in an addressed slave mode.

When STO = 1 in master mode, a STOP condition is transmitted on the I2C bus. When the bus detects the STOP condition, STO is cleared automatically. In slave mode, setting STO bit can recover from an error condition. In this case, no STOP condition is transmitted to the bus. The HW behaves as if a STOP condition has been received and it switches to “not addressed” slave receiver mode.

If STA and STO are both set, then a STOP condition is transmitted on the I2C bus if the interface is in master mode, and transmits a START condition thereafter. If the I2C interface is in slave mode, an internal STOP condition is generated, but is not transmitted on the bus.

**\* Note:**

1. **I2CEN shall be set at last.**
2. **HW will assign SCL0/SCL1 and SDA0/SDA1 pins as output pins with open-drain function instead of GPIO automatically.**
3. **ACK and NACK bits can't both be “1” when receiving data.**
4. **User has to write 1 to ACK or NACK bit in Master mode to continue next RX process.**

| Bit  | Name     | Description                                                                                                                                                                                                                                                                                                                                                                              | Attribute | Reset |
|------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:9 | Reserved |                                                                                                                                                                                                                                                                                                                                                                                          | R         | 0     |
| 8    | I2CEN    | I2C Interface enable bit<br>0: Disable. The STO bit is forced to “0”.<br>1: Enable.<br>I2CEN shall not be used to temporarily release the I2C bus since the bus status is lost when I2CEN resets. The ACK flag should be used instead.                                                                                                                                                   | R/W       | 0     |
| 7:6  | Reserved |                                                                                                                                                                                                                                                                                                                                                                                          | R         | 0     |
| 5    | STA      | START bit.<br>0: No START condition or Repeated START condition will be generated.<br>1: Cause the I2C interface to enter master mode and transmit a START or a Repeated START condition. Automatically cleared by HW.                                                                                                                                                                   | R/W       | 0     |
| 4    | STO      | STOP flag<br>0: Stop condition idle.<br>1: Cause the I2C interface to transmit a STOP condition in master mode, or recover from an error condition in slave mode.<br>Automatically cleared by HW.                                                                                                                                                                                        | R/W       | 0     |
| 3    | Reserved |                                                                                                                                                                                                                                                                                                                                                                                          | R         | 0     |
| 2    | ACK      | Assert ACK flag.<br>0: Master mode→ No function<br>Slave mode→Return a NACK after receiving address or data.<br>1: An ACK will be returned during the acknowledge clock pulse on SCLn when <ul style="list-style-type: none"> <li>➤ The address in the Slave Address register has been received.</li> <li>➤ The General Call address has been received while the General Call</li> </ul> | R/W       | 0     |

|          |          |                                                                                                                                                                                                                                                                             |     |   |
|----------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---|
|          |          | enable bit (GCEN) in SLVADDR0 register is set.<br>➤ A data byte has been received while the I2C is in the master receiver mode.<br>➤ A data byte has been received while the I2C is in the addressed slave receiver mode.<br>HW will clear after issuing ACK automatically. |     |   |
| <b>1</b> | NACK     | Assert NACK flag.<br>0: No function<br>1: An NACK will be returned during the acknowledge clock pulse on SCLn when<br>➤ A data byte has been received while the I2C is in the master receiver mode.<br>HW will clear after issuing NACK automatically.                      | R/W | 0 |
| <b>0</b> | Reserved |                                                                                                                                                                                                                                                                             | R   | 0 |

### 13.10.2 I2C n Status register (I2Cn\_STAT) (n=0,1)

Address Offset: 0x04

Check this register when I2C interrupt occurs, and all status will be cleared automatically by writing I2Cn\_CTRL or I2Cn\_TXDATA register.

Following events will trigger I2C interrupt if I2C interrupt is enabled in NVIC interrupt controller.

- **START/Repeat START condition**
- **STOP condition**
- **Timeout**
- **Data byte transmitted or received**
- **ACK Transmit or received**
- **NACK Transmit or received**

| Bit          | Name       | Description                                                                                                                       | Attribute | Reset |
|--------------|------------|-----------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:16</b> | Reserved   |                                                                                                                                   | R         | 0     |
| <b>15</b>    | I2CIF      | I2C Interrupt flag.<br>0: I2C status doesn't change.<br>1: Read→I2C status changes.<br>Write→Clear this flag.                     | R/W       | 0     |
| <b>14:10</b> | Reserved   |                                                                                                                                   | R         | 0     |
| <b>9</b>     | TIMEOUT    | Time-out status<br>0: No Timeout<br>1: Timeout                                                                                    | R         | 0     |
| <b>8</b>     | LOST_ARB   | Lost arbitration<br>0: Not lost arbitration<br>1: Lost arbitration                                                                | R         | 0     |
| <b>7</b>     | SLV_TX_HIT | 0: No matched slave address.<br>1: Slave address hit, and is called for TX in slave mode.                                         | R         | 0     |
| <b>6</b>     | SLV_RX_HIT | 0: No matched slave address.<br>1: Slave address hit, and is called for RX in slave mode.                                         | R         | 0     |
| <b>5</b>     | MST        | Master/Slave status<br>0: I2C is in Slave state.<br>1: I2C is in Master state.                                                    | R         | 0     |
| <b>4</b>     | START_DN   | Start done status<br>0: No START bit.<br>1: MASTER mode→ a START bit was issued.<br>SLAVE mode→ a START bit was received.         | R         | 0     |
| <b>3</b>     | STOP_DN    | Stop done status<br>0: No STOP bit.<br>1: MASTER mode→ a STOP condition was issued.<br>SLAVE mode→ a STOP condition was received. | R         | 0     |
| <b>2</b>     | NACK_STAT  | NACK done status<br>0 : Not received a NACK<br>1 : Received a NACK                                                                | R         | 0     |
| <b>1</b>     | ACK_STAT   | ACK done status<br>0 : Not received an ACK<br>1 : Received an ACK                                                                 | R         | 0     |

|   |       |                                                                                                   |   |   |
|---|-------|---------------------------------------------------------------------------------------------------|---|---|
| 0 | RX_DN | RX done status<br>0: No RX with ACK/NACK transfer.<br>1: 8-bit RX with ACK/NACK transfer is done. | R | 0 |
|---|-------|---------------------------------------------------------------------------------------------------|---|---|

### 13.10.3 I2C n TX Data register (I2Cn\_TXDATA) (n=0,1)

Address Offset: 0x08

This register contains the data to be transmitted.

In Master TX mode, CPU writes this register will trigger a TX function. In Slave TX mode, CPU has to write this register before next TX procedure.

| Bit  | Name      | Description             | Attribute | Reset |
|------|-----------|-------------------------|-----------|-------|
| 31:8 | Reserved  |                         | R         | 0     |
| 7:0  | DATA[7:0] | Data to be transmitted. | R/W       | 0x00  |

### 13.10.4 I2C n RX Data register (I2Cn\_RXDATA) (n=0,1)

Address Offset: 0x0C

| Bit  | Name      | Description                                                    | Attribute | Reset |
|------|-----------|----------------------------------------------------------------|-----------|-------|
| 31:8 | Reserved  |                                                                | R         | 0     |
| 7:0  | DATA[7:0] | Contains the data received. Read this register when RX_DN = 1. | R         | 0x00  |

### 13.10.5 I2C n Slave Address 0 register (I2Cn\_SLVADDR0) (n=0,1)

Address Offset: 0x10

Only used in slave mode. In master mode, this register has no effect.

If this register contains 0x00, the I2C will not acknowledge any address on the bus. Register ADR0 to ADR3 will be cleared to this disabled state on reset.

| Bit   | Name      | Description                                                                                          | Attribute | Reset |
|-------|-----------|------------------------------------------------------------------------------------------------------|-----------|-------|
| 31    | ADD_MODE  | Slave address mode.<br>0 : 7-bit address mode<br>1: 10-bit address mode                              | RW        | 0     |
| 30    | GCEN      | General call address enable bit.<br>0: Disable<br>1: Enable general call address (0x0)               | RW        | 0     |
| 29:10 | Reserved  |                                                                                                      | R         | 0     |
| 9:0   | ADDR[9:0] | The I2C slave address.<br>ADD[9:0] is valid when ADD_MODE = 1<br>ADD[7:1] is valid when ADD_MODE = 0 | R/W       | 0     |

### 13.10.6 I2C n Slave Address 1~3 register (I2Cn\_SLVADDR1~3) (n=0,1)

Address Offset: 0x14, 0x18, 0x1C

| Bit   | Name      | Description                                                                                          | Attribute | Reset |
|-------|-----------|------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:10 | Reserved  |                                                                                                      | R         | 0     |
| 9:0   | ADDR[9:0] | The I2C slave address.<br>ADD[9:0] is valid when ADD_MODE = 1<br>ADD[7:1] is valid when ADD_MODE = 0 | R/W       | 0     |

**13.10.7 I2C n SCL High Time register (I2Cn\_SCLHT) (n=0,1)**

Address Offset: 0x20

\* **Note:**  $I2C \text{ Bit Frequency} = I2Cn\_PCLK / (I2Cn\_SCLHT + I2Cn\_SCLLT)$

| Bit  | Name      | Description                                                                         | Attribute | Reset |
|------|-----------|-------------------------------------------------------------------------------------|-----------|-------|
| 31:8 | Reserved  |                                                                                     | R         | 0     |
| 7:0  | SCLH[7:0] | Count for SCL High Period time<br>SCL High Period Time = (SCLH+1) * I2C0_PCLK cycle | R/W       | 0x04  |

**13.10.8 I2C n SCL Low Time register (I2Cn\_SCLLT) (n=0,1)**

Address Offset: 0x24

| Bit  | Name      | Description                                                                       | Attribute | Reset |
|------|-----------|-----------------------------------------------------------------------------------|-----------|-------|
| 31:8 | Reserved  |                                                                                   | R         | 0     |
| 7:0  | SCLL[7:0] | Count for SCL Low Period time<br>SCL Low Period Time = (SCLL+1) * I2C0_PCLK cycle | R/W       | 0x04  |

**13.10.9 I2C n Timeout Control register (I2Cn\_TOCTRL) (n=0,1)**

Address Offset: 0x2C

Timeout happens when Master/Slave SCL remained LOW for:  
TO \* 32 \* I2C0\_PCLK cycle.

When I2C timeout occurs, the I2C transfer will return to "IDLE" state, and issue a TO interrupt to inform user. That means SCL/SDA will be released by HW after timeout. User can issue a STOP after timeout interrupt occurred in Master mode.

Time-out status will be cleared automatically by writing I2Cn\_CTRL or I2Cn\_TXDATA register.

| Bit   | Name     | Description                                                                                                 | Attribute | Reset |
|-------|----------|-------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:16 | Reserved |                                                                                                             | R         | 0     |
| 15:0  | TO[15:0] | Count for checking Timeout.<br>0: Disable Timeout checking<br>N: Timeout period time = N*32*I2Cn_PCLK cycle | R/W       | 0x0   |

**13.10.10 I2C n Monitor Mode Control register (I2Cn\_MMCTRL) (n=0,1)**

Address Offset: 0x30

This register controls the Monitor mode which allows the I2C module to monitor traffic on the I2C bus without actually participating in traffic or interfering with the I2C bus.

In Monitor mode, SDA output will be forced high to prevent the I2C module from outputting data of any kind (including ACK) onto the I2C data bus. Depending on the state of the SCLOEN bit, the SCL output may be also forced high to prevent the module from having control over the I2C clock line.

\* **Note:** The SCLOEN and MATCH\_ALL bits have no effect if MMEN bit is '0' (i.e. if the module is NOT in monitor mode).

| Bit         | Name      | Description                                                                                                                                                                                                                                                                                  | Attribute | Reset |
|-------------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:8</b> | Reserved  |                                                                                                                                                                                                                                                                                              | R         | 0     |
| <b>2</b>    | MATCH_ALL | Match address selection<br>0: Interrupt will only be generated when the address matches one of the values in I2Cn_SLVADDR0~3 register.<br>1: If I2C is in monitor mode, an interrupt will be generated on ANY address received. This will enable the part to monitor all traffic on the bus. | R/W       | 0     |
| <b>1</b>    | SCLOEN    | SCL output enable bit.<br>0: SCL output will be forced high.<br>1: I2C module may act as a slave peripheral just like in normal operation, the I2C holds the clock line low until it has had time to respond to an I2C interrupt.                                                            | R/W       | 0     |
| <b>0</b>    | MMEN      | Monitor mode enable bit.<br>0: Disable<br>1: Enable.                                                                                                                                                                                                                                         | R/W       | 0     |

# 14 UNIVERSAL SYNCHRONOUS AND ASYNCHRONOUS RECEIVER AND TRANSMITTER (USART)

## 14.1 OVERVIEW

The USART offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. The serial interface is applied to low speed data transfer and communicate with low speed peripheral devices.

The USART offers a very wide range of baud rates using a fractional baud rate generator. It supports both synchronous one-way communication and single wire communication. It also supports the LIN (local interconnection network), Smart card Protocol, and modem operations (CTS/RTS).

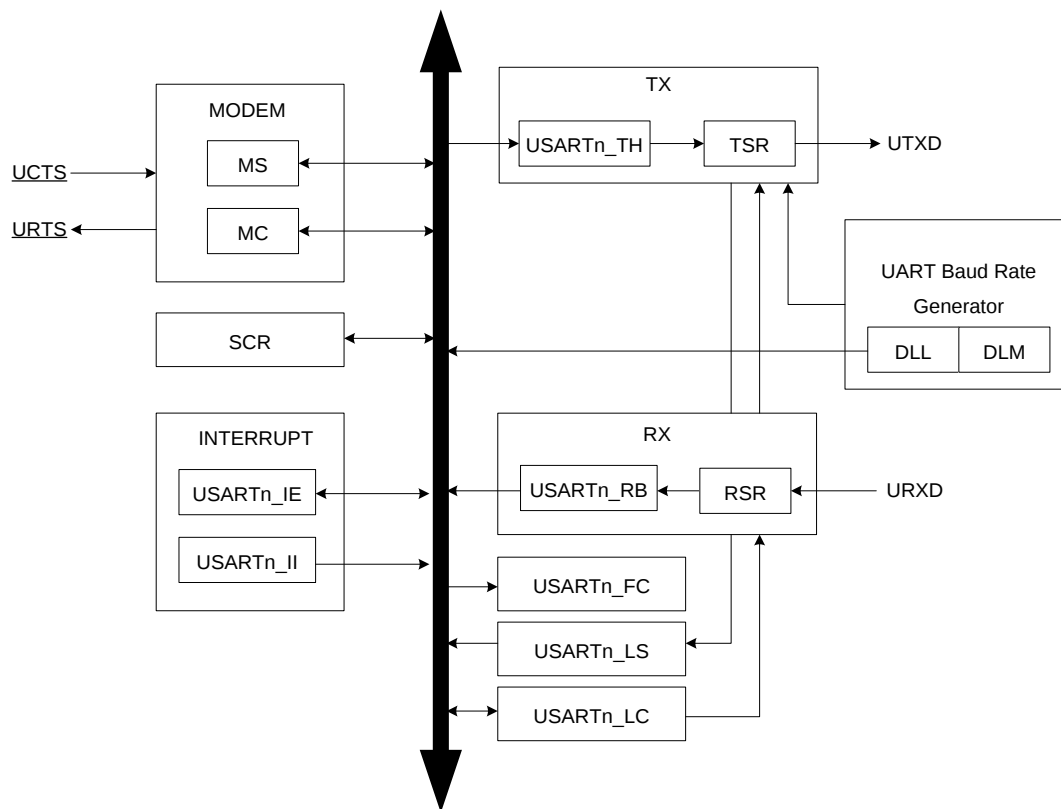
## 14.2 FEATURES

- Full-duplex, 2-wire asynchronous data transfer.
- Single-wire half-duplex communication
- Transmitter clock output for synchronous transmission
- 16-byte receive and transmit FIFOs
- Register locations conform to 16550 industry standard.
- Receiver FIFO trigger points at 1, 4, 8, and 14 bytes.
- Built-in baud rate generator.
- Software or hardware flow control.
- EIA-485 9-bit mode support with output enable.
- Modem control signals (CTS/RTS).
- ISO 7816-3 compliant Smart card interface.

## 14.3 PIN DESCRIPTION

| Pin Name     | Type | Description                                                                                                                                                                                                                                                                                                                  | GPIO Configuration                |
|--------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|
| UTXDn        | O    | Serial Transmit data.                                                                                                                                                                                                                                                                                                        |                                   |
| URXDn        | I    | Serial Receive data.                                                                                                                                                                                                                                                                                                         | Depends on GPIO <sub>n</sub> _CFG |
| USCKn        | O    | Serial clock of Synchronous mode (Master)                                                                                                                                                                                                                                                                                    |                                   |
| <u>UCTSn</u> | I    | Clear to Send.<br>When low, this indicates that the MODEM or data set is ready to exchange data. The <u>CTS</u> signal is a MODEM status input whose conditions can be tested by reading bit 4 (CTS) of USART <sub>n</sub> _MS register.                                                                                     | Depends on GPIO <sub>n</sub> _CFG |
| <u>URTSn</u> | O    | Request to Send. RS-485 direction control pin.<br>When low, this informs the MODEM or data set that the UART is ready to exchange data. The <u>RTS</u> output signal can be set to an active low by programming bit 1 (RTS) of USART <sub>n</sub> _MC register. Loop mode operation holds this signal in its inactive state. |                                   |

## 14.4 BLOCK DIAGRAM



## 14.5 EIA-485/RS-485 MODES

The RS-485/EIA-485 feature allows the USART to be configured as an addressable slave receiver. The addressable slave receiver is one of multiple slaves receivers controlled by a single master.

The USART master transmitter will identify an address character by setting the parity (9th) bit to '1'. For data characters, the parity bit is set to '0'.

Each USART slave receiver can be assigned a unique address. The slave can be programmed to either manually or automatically reject data following an address which is not theirs.

In RS-485 mode, PS bits in [USARTn\\_LC](#) register shall be selected as forced 1 stick parity (Address), or forced stick 0 parity (Data) by SW. In addition, the word length shall be 8 bits by setting WLS bits in [USARTn\\_LC](#) register to 11b by SW.

### 14.5.1 RS-485/EIA-485 NORMAL MULTIDROP MODE (NMM)

Setting the NMMEN bit in [USARTn\\_RS485CTRL](#) register enables this mode. In this mode, an address is detected when a received byte causes the USART to set the parity error and generate an interrupt.

If the receiver is disabled (RXEN = 0 in [USARTn\\_RS485CTRL](#) register), any received data bytes will be ignored and will not be stored in the RXFIFO. When an address byte is detected (parity bit = '1') it will be placed into the RXFIFO and a parity error (PE) Interrupt will be generated. The processor can then read the address byte and decide whether or not to enable the receiver to accept the following data.

While the receiver is enabled (RXEN = 1 in [USARTn\\_RS485CTRL](#) register), all received bytes will be accepted and stored in the RXFIFO regardless of whether they are data or address. When an address character is received a parity error interrupt will be generated and the processor can decide whether or not to disable the receiver.

### 14.5.2 RS-485/EIA-485 AUTO ADDRESS DETECTION (AAD) MODE

When both NMMEN (9-bit mode enable) bit and AADEN (AAD mode enable) bit in [USARTn\\_RS485CTRL](#) register are set, the USART is in auto address detect mode.

In this mode, the receiver will compare any address byte received (parity = '1') to the 8-bit value programmed into the [USARTn\\_RS485ADRMATCH](#) register.

If the receiver is disabled (RXEN = 0 in [USARTn\\_RS485CTRL](#) register), any received byte will be discarded if it is either a data byte or an address byte which is different from the value in [USARTn\\_RS485ADRMATCH](#) register.

When a matching address character is detected it will be pushed onto the RXFIFO along with the parity bit, and the receiver will be automatically enabled (RXEN bit will be set by HW). The receiver will also generate an RX Data Available (RDA) Interrupt.

While the receiver is enabled (RXEN = 1 in [USARTn\\_RS485CTRL](#) register), all bytes received will be accepted and stored in the RXFIFO until an address byte which is different from the MATCH value is received. When this occurs, the receiver will be automatically disabled by HW (RXEN bit will be cleared by HW), the received non-matching address character will not be stored in the RXFIFO.

### 14.5.3 RS-485/EIA-485 AUTO DIRECTION CONTROL (ADC)

RS485/EIA-485 mode includes the option of allowing the transmitter to automatically control the state of the DIR pin as a direction control output signal. Set ADCEN bit in [USARTn\\_RS485CTRL](#) register to enable this feature.

The ADCEN bit takes precedence over all other mechanisms controlling the direction control pin with the exception of loopback mode.

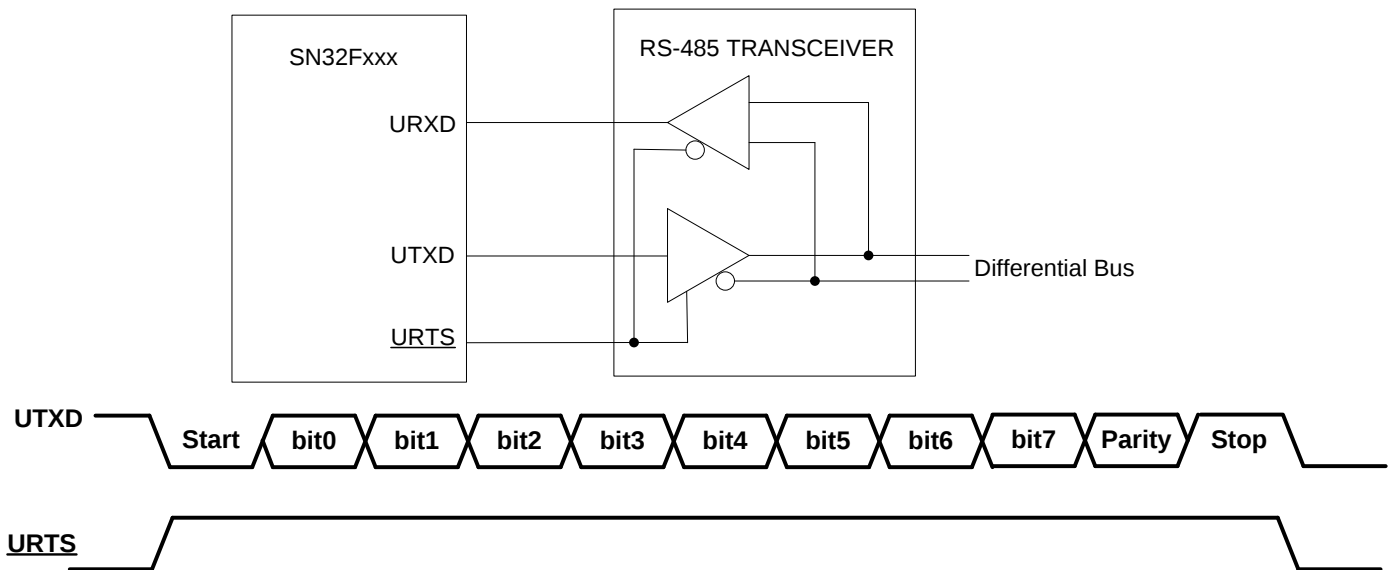
### 14.5.4 RS485/EIA-485 DRIVER DELAY TIME

The driver delay time is the delay between the last stop bit leaving the TXFIFO and the de-assertion of URTS. This delay time can be programmed in the 8-bit USARTn\_RS485DLYV register. The delay time is in periods of the baud clock. Any delay time from 0 to 255 bit times may be used.

### 14.5.5 RS485/EIA-485 OUTPUT INVERSION

The polarity of the direction control signal on the URTS pin can be reversed by programming OINV bit in USARTn\_RS485CTRL register. When OINV bit is set, the direction control pin will be driven to logic 1 (driven LOW) when the transmitter has data waiting to be sent. The direction control pin will be driven to logic 0 (driven High) once the last bit of data has been transmitted.

### 14.5.6 RS485/EIA-485 FRAME STRUCTURE



## 14.6 BAUD RATE CALCULATION

The USART baud rate is calculated as:

$$\text{UART}_{\text{BAUDRATE}} = \frac{\text{USARTn\_PCLK}}{\text{Oversampling} \times (256 \times \text{DLM} + \text{DLL}) \times (1 + \text{DIVADDVAL} / \text{MUL})}$$

Where USARTn\_PCLK is the peripheral clock, USARTn\_DLM and USARTn\_DLL are the standard UART baud rate divider registers, and DIVADDVAL and MUL are USART fractional baud rate generator specific parameters in USARTn\_FD register.

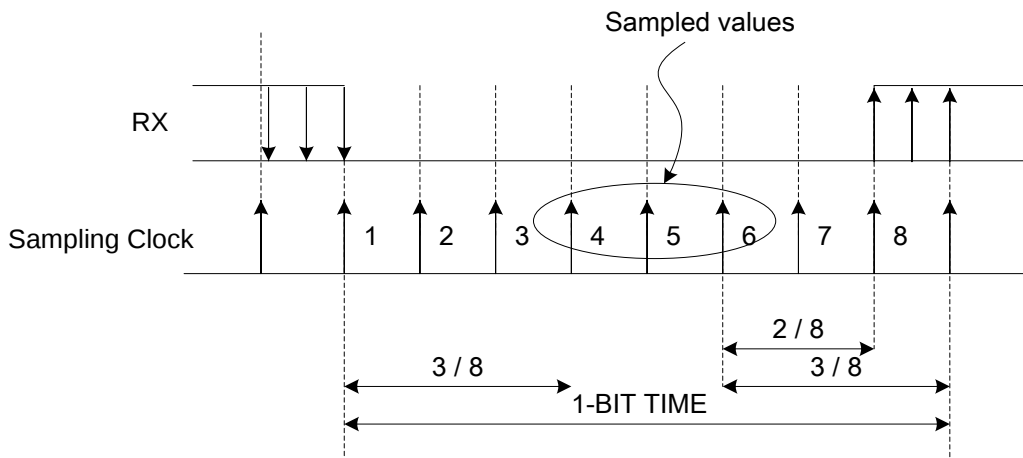
The value of MUL and DIVADDVAL should comply with the following conditions:

1.  $1 \leq \text{MUL} \leq 15$
2.  $0 \leq \text{DIVADDVAL} \leq 14$
3.  $\text{DIVADDVAL} < \text{MUL}$
4.  $\text{MUL} - \text{DIVADDVAL} \neq 2$
5. Oversampling is 8 or 16

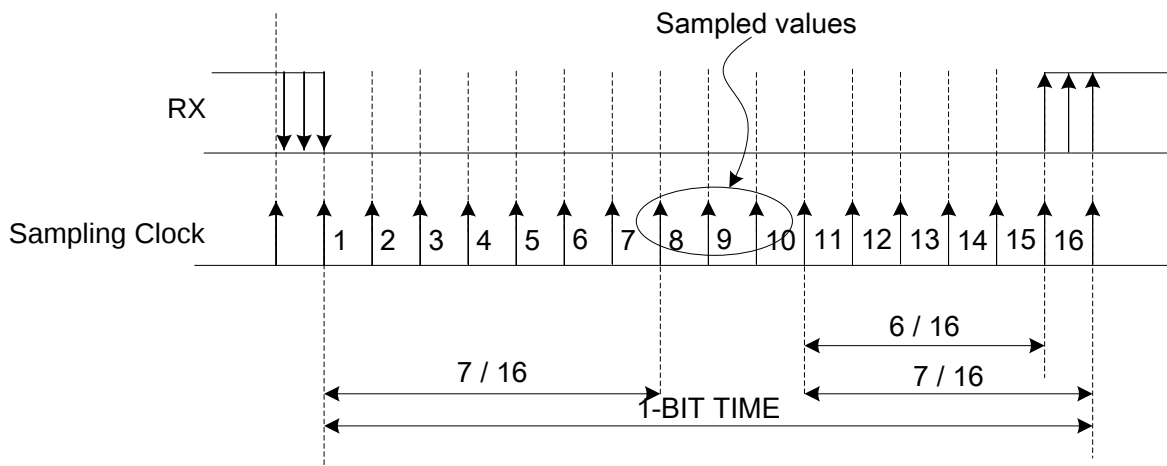
The value of the [USARTn\\_FD](#) register should not be modified while transmitting/receiving data or data may be lost or corrupted.

The oversampling method can be selected by programming the OVER8 bit in [USARTn\\_FD](#) register and can be either 16 or 8 times the baud rate clock.

- OVER8=1: Oversampling by 8 to achieve higher speed (up to USARTn\_PCLK/8). In this case the maximum receiver tolerance to clock deviation is reduced.



- OVER8=0: Oversampling by 16 to increase the tolerance of the receiver to clock deviations. In this case, the maximum speed is limited to maximum USARTn\_PCLK/16



If the [USARTn\\_FD](#) register value does not comply with these two requests, then the fractional divider output is undefined. If DIVADDVAL is zero then the fractional divider is disabled, and the clock will not be divided.

USART can operate with or without using the Fractional Divider. The desired baud rate can be achieved using several different Fractional Divider settings. The following algorithm illustrates one way of finding a set of DLM, DLL, MUL, and DIVADDVAL values. Such set of parameters yields a baud rate with a relative error of less than 1.1% from the desired one.

The following example illustrates selecting the DIVADDVAL, MUL, DLM, and DLL to generate BR = 115200 when USARTn\_PCLK = 12 MHz, and Oversampling = 16.

$$\text{UART}_{\text{BAUDRATE}} = \frac{\text{USARTn\_PCLK}}{\text{Oversampling} \times (256 \times \text{DLM} + \text{DLL}) \times (1 + \text{DIVADDVAL} / \text{MUL})}$$

$$115200 = \frac{12000000}{\dots}$$

$$16 \times (256 \times \text{DLM} + \text{DLL}) \times (1 + \text{DIVADDVAL} / \text{MUL})$$

$$(256 \times \text{DLM} + \text{DLL}) \times (1 + \text{DIVADDVAL} / \text{MUL}) = 6.51$$

Since the value of MUL and DIVADDVAL should comply with the following conditions:

1.  $1 \leq \text{MUL} \leq 15$
2.  $0 \leq \text{DIVADDVAL} \leq 14$
3.  $\text{DIVADDVAL} < \text{MUL}$
4.  $\text{MUL} - \text{DIVADDVAL} \neq 2$

Thus, the suggested UART settings would be: DLM = 0, DLL = 4, DIVADDVAL = 5, and MUL = 8 (fill in 7 in the MULVAL bits). The baud rate generated is 115384, and has a relative error of 0.16% from the originally specified 115200.

## 14.7 MODEM CONTROL (MC)

If Auto-RTS mode is enabled, the USART's receiver FIFO hardware controls the URTS output of the USART. If the auto-CTS mode is enabled, the USART's transmitter will only start sending if the UCTS pin is low.

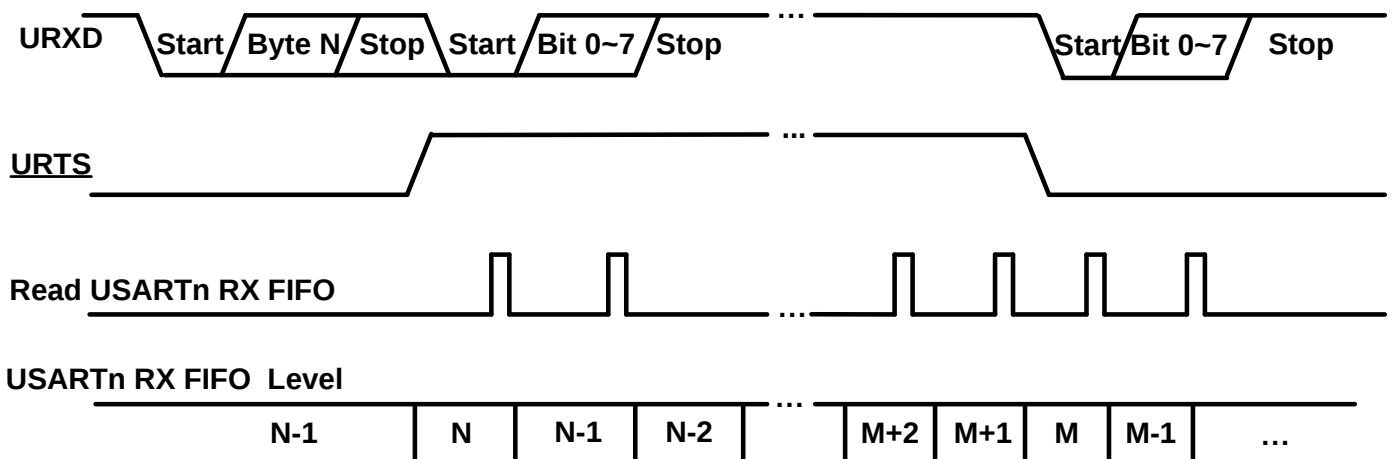
### 14.7.1 AUTO-RTS

The Auto-RTS function is enabled by setting the RTSEN bit. Auto-RTS data flow control originates in the USARTn\_RB module and is linked to the programmed receiver FIFO trigger level. If auto-RTS is enabled, the data-flow is controlled as follows:

When the receiver FIFO level reaches the programmed trigger level, URTS is deasserted (to a high value). It is possible that the sending USART sends an additional byte after the trigger level is reached (assuming the sending USART has another byte to send) because it might not recognize the deassertion of URTS until after it has begun sending the additional byte. URTS is automatically reasserted (to a low value) once the receiver FIFO has reached the previous trigger level. The reassertion of URTS signals the sending USART to continue transmitting data.

If Auto-RTS mode is disabled, the RTSEN bit controls the URTS output of the USART. If Auto-RTS mode is enabled, hardware controls the RTS output, and the actual value of URTS will be copied in the URTS Control bit of the USART. As long as Auto-RTS is enabled, the value of the RTS Control bit is read-only for software.

Example: Suppose the USART operating in type 16550 mode has the trigger level in USARTn\_FIFOCtrl register set to 0x2, then, if Auto-RTS is enabled, the USART will deassert the URTS output as soon as the receive FIFO contains 8 bytes. The URTS output will be reasserted as soon as the receive FIFO hits the previous trigger level: 4 bytes.

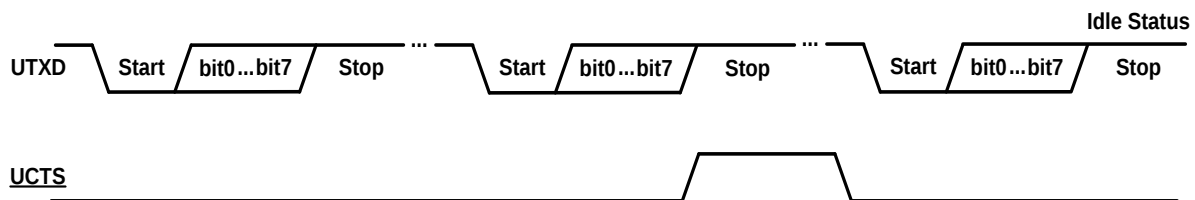


## 14.7.2 AUTO-CTS

The Auto-CTS function is enabled when CTSEN=1. If Auto-CTS is enabled, the transmitter circuitry checks the UCTS input before sending the next data byte. When UCTS is active (low), the transmitter sends the next byte. To stop the transmitter from sending the following byte, UCTS must be released before the middle of the last stop bit that is currently being sent. In Auto-CTS mode, a change of the UCTS signal does not trigger a modem status interrupt unless the CTS Interrupt Enable bit is set, but the DCTS bit in the USARTn\_MS register will be set.

| MSIE | CTSEN | Delta CTS (DCTS) | MODEM status interrupt |
|------|-------|------------------|------------------------|
| 0    | X     | X                | X                      |
| 1    | 0     | 1                | O                      |
| 1    | 1     | 0                | X                      |
| 1    | 1     | 1                | O                      |

The Auto-CTS function typically eliminates the need for CTS interrupts. When flow control is enabled, a UCTS state change does not trigger host interrupts because the device automatically controls its own transmitter. Without Auto-CTS, the transmitter sends any data present in the transmit FIFO and a receiver overrun error can result.



During transmission of the second character the UCTS signal is negated. The third character is not sent thereafter. The USART maintains 1 on UTXD as long as UCTS is negated (high). As soon as UCTS is asserted, transmission resumes and a start bit is sent followed by the data bits of the next character.

## 14.8 AUTO-BAUD FLOW

### 14.8.1 AUTO-BAUD

The USART auto-baud function can be used to measure the incoming baud rate based on the “AT” protocol (Hayes command). If enabled the auto-baud feature will measure the bit time of the receive data stream and set the divisor latch registers USARTn\_DLM and USARTn\_DLL accordingly.

Auto-baud function is started by setting the START bit in USARTn\_ABCTRL register, and can be stopped by clearing the START bit. The START bit will clear once auto-baud has finished and reading the bit will return the status of auto-baud (pending/finished). When auto-baud function is started, FIFO will be cleared, not available to write the TX FIFO, and the transmitter will stop transmitting until auto-baud function finishes or be stopped.

Two auto-baud measuring modes are available which can be selected by the MODE bit in USARTn\_ABCTRL register. In Mode 0 the baud rate is measured on two subsequent falling edges of the USART RX pin (the falling edge of the start bit and the falling edge of the least significant bit). In Mode 1 the baud rate is measured between the falling edge and the subsequent rising edge of the USART RX pin (the length of the start bit).

The AUTORESTART bit in USARTn\_ABCTRL register can be used to automatically restart baud rate measurement if a timeout occurs (the rate measurement counter overflows). If this bit is set, the rate measurement will restart at the next falling edge of the URXD pin.

The auto-baud function can generate two interrupts.

- The ABTOINT interrupt in USARTn\_I register will get set if the interrupt is enabled (ABTOIE bit in USARTn\_IE register is set and the auto-baud rate measurement counter overflows).

- The ABEOINT interrupt in [USARTn\\_I2](#) register will get set if the interrupt is enabled (ABTOIE bit in [USARTn\\_IE](#) register is set and the auto-baud has completed successfully).

The auto-baud interrupts have to be cleared by setting the corresponding ABTOINTCLR and ABEOIE bits in [USARTn\\_IE](#) register.

The fractional baud rate generator must be disabled (DIVADDVAL = 0) during auto-baud. Also, when auto-baud is used, any write to [USARTn\\_DLM](#) and [USARTn\\_DLL](#) registers should be done before [USARTn\\_ABCCTRL](#) register write. The minimum and the maximum baud rates supported by USART are a function of USARTn\_PCLK and the number of data bits, stop bits and parity bits.

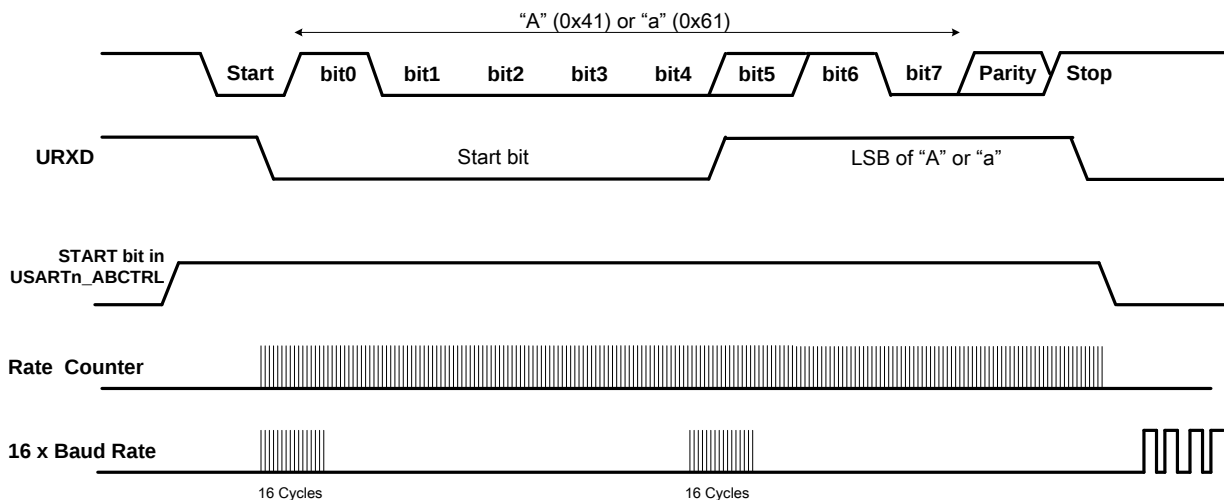
$$ratemin = \frac{2 \times PCLK}{16 \times 2^{15}} \leq \text{USART}_{baudrate} \leq \frac{PCLK}{16 \times (2 + databits + paritybits + stopbits)} = ratemax$$

## 14.8.2 AUTO-BAUD MODES

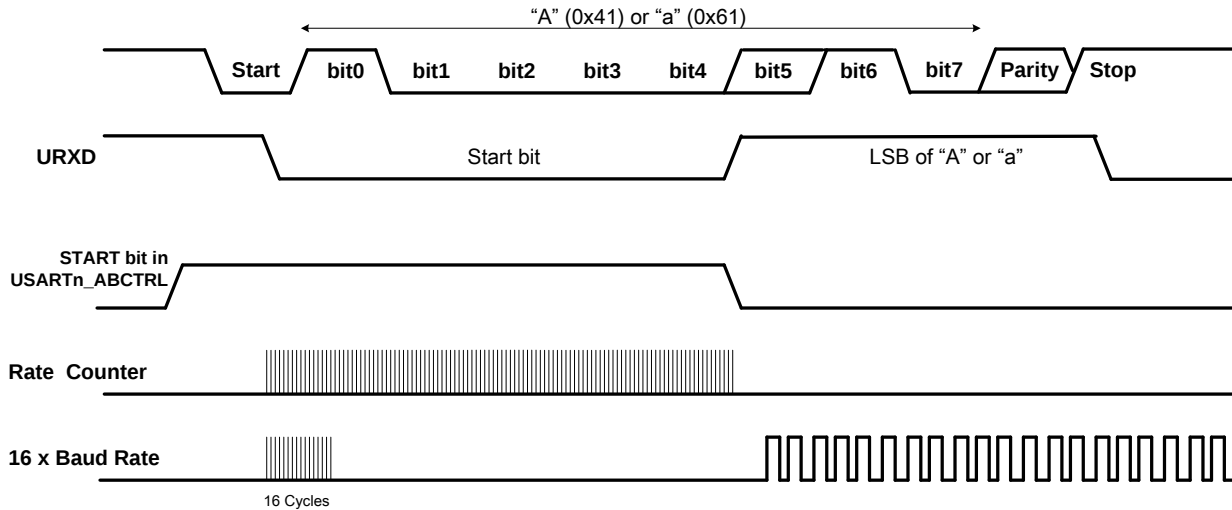
When the SW is expecting an "AT" command, it configures the USART with the expected character format and sets the ACR Start bit. The initial values in the divisor latches DLM and DLL don't care. Because of the "A" or "a" ASCII coding ("A" = 0x41, "a" = 0x61), the USART Rx pin sensed start bit and the LSB of the expected character are delimited by two falling edges. When the ACR Start bit is set, the auto-baud protocol will execute the following phases:

1. On START bit setting, the baud rate measurement counter is reset and the RSR is reset. The RSR baud rate is switched to the highest rate.
2. A falling edge on URXD pin triggers the beginning of the start bit. The rate measuring counter will start counting USARTn\_PCLK cycles.
3. During the receipt of the start bit, 16 pulses are generated on the RSR baud input with the frequency of the USART input clock, guaranteeing the start bit is stored in the RSR.
4. During the receipt of the start bit (and the character LSB for MODE = 0 in [USARTn\\_ABCTRL](#) register), the rate counter will continue incrementing with the pre-scaled USART input clock (USARTn\_PCLK).
5. If MODE = 0, the rate counter will stop on next falling edge of the USART RX pin. If MODE = 1, the rate counter will stop on the next rising edge of the URXD pin.
6. The rate counter is loaded into [USARTn\\_DLM/USARTn\\_DLL](#) and the baud rate will be switched to normal operation. After setting the DLM/DLL, the end of auto-baud interrupt ABEOINT in [USARTn\\_I2](#) register will be set, if enabled. The RSR will now continue receiving the remaining bits of the character.

### ➤ AUTO-BAUD RATE MODE 0 Waveform



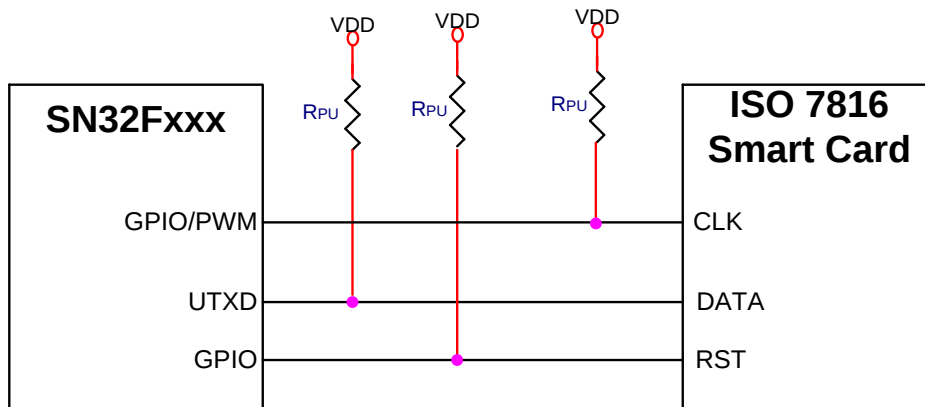
### ➤ AUTO-BAUD RATE MODE 1 Waveform



## 14.9 SMART CARD MODE

The Smart card mode is enabled by setting the USARTEN bit to 1 and MODE[2:0] = 011b in [USARTn\\_CTRL](#) register, the USART provides bidirectional serial data on the open-drain UTXD pin. No URXD pin is used in this mode. If a clock source is needed as an oscillator source into the Smart card, a timer match or PWM output can be used in cases when a higher frequency clock is needed that is not synchronous with the data bit rate.

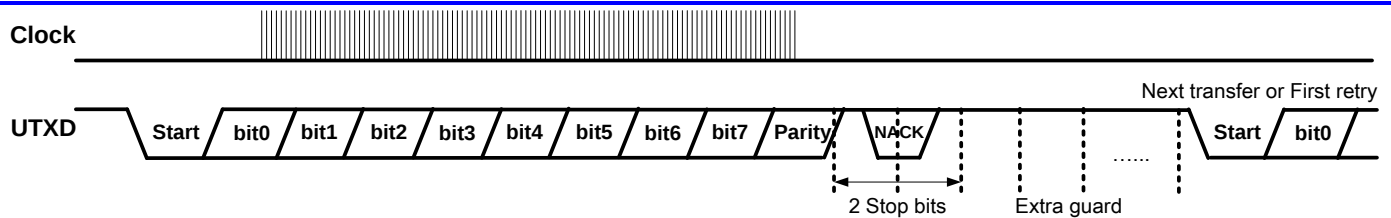
The USCLK pin may not be adequate for most asynchronous cards since it will output synchronously with the data and the data bit rate. SW must use timers to implement character and block waiting times instead.



### 14.9.1 SMART CARD SETUP PROCEDURE

A T = 0 protocol transfer consists of 8-bits of data, an even parity bit, and two stop bits that allow for the receiver of the particular transfer to flag parity errors through the NACK response. Extra guard bits may be added according to card requirements.

If no NACK is sent, the next byte may be transmitted immediately after the last guard bit. If the NACK is sent, the transmitter will retry sending the byte until successfully received or until the SCICTRL retry limit has been met.



The smart card must be set up with the following considerations:

1. Program [SYS1\\_PRST](#) register so that the USART is not continuously reset.
2. Program USARTnPRE bits in [SYS1\\_APBPC1](#) register for an initial USART frequency of 3.58 MHz.
3. If necessary, program the USARTn\_DLM and USARTn\_DLL to 00 and 01 respectively, to pass the USART clock through without division.
4. Program the [USARTn\\_LC](#) register for 8-bit characters, parity enabled, even parity.
5. Program [USARTn\\_SCICTRL](#) register to enable the smart card feature with the desired options, and HW enables a USART TXD function automatically.
6. Set up one or more timer(s) to provide timing as needed for ISO-7816 startup.
7. Program USARTnCLKEN bit in [SYS1\\_AHBCLKEN](#) register to enable the USART clock.

Thereafter, SW should monitor card insertion, handle activation, wait for answer to reset as described in ISO7816-3.

## 14.10 SYNCHRONOUS MODE

The synchronous mode is selected by writing the MODE bits to 100b in [USARTn\\_CTRL](#) register.

The USART allows the user to control a bidirectional synchronous serial communications in master mode. The SCLK pin is the output of the USART transmitter clock. No clock pulses are sent to the SCLK pin during start bit and stop bit.

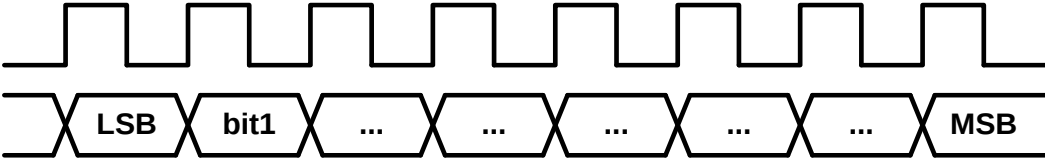
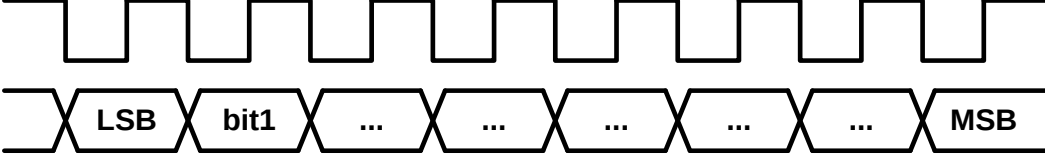
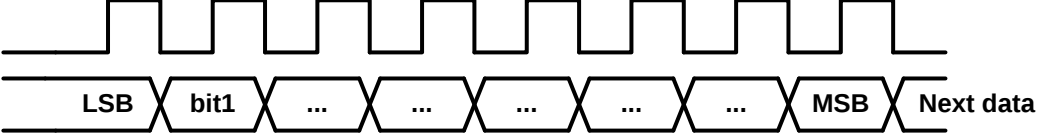
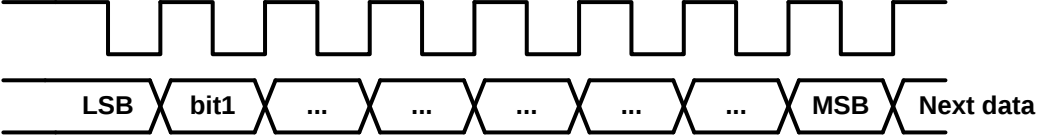
The CPOL bit in [USARTn\\_CTRL](#) register allows the user to select the clock polarity, and the CPHA bit allows the user to select the phase of the clock.

During the Idle state, preamble and send break, the external SCLK clock is not activated. In synchronous mode the USART transmitter works exactly like in asynchronous mode. But as SCLK is synchronized with TX (according to CPOL and CPHA), the data on TX is synchronous.

In synchronous mode, the USART receiver works in a different manner compared to the asynchronous mode. If Receiver is enabled (RXEN=1), the data is sampled on SCLK (depending on CPOL and CPHA) without any oversampling. A setup and a hold time must be respected (which depends on the baud rate: 1/16 bit time).

**\* Note:**

- \* *The SCLK pin works in conjunction with the UTXD pin, so the clock is provided only if TXEN=1 in [USARTn\\_CTRL](#) register, and a data is being transmitted (the data register USART\_DR has been written). This means that it is not possible to receive a synchronous data without transmitting data.*
- \* *The CPOL and CPHA bits in [USARTn\\_SYNCCTRL](#) register have to be selected when both the transmitter and the receiver are disabled (TXEN=0 and RXEN=0) to ensure that the clock pulses function correctly. These bits should not be changed while the transmitter or the receiver is enabled (TXEN=1 and RXEN=1).*
- \* *The Synchronous mode supports master mode only, it can NOT receive or send data related to an input clock (SCLK is always an output).*

| CPOL | CPHA | SCLK Idle Status | Diagrams                                                                           |
|------|------|------------------|------------------------------------------------------------------------------------|
| 0    | 1    | Low              |  |
| 1    | 1    | High             |  |
| 0    | 0    | Low              |  |
| 1    | 0    | High             |  |

## 14.11 USART REGISTERS

Base Address: 0x4001 6000 (USART0)  
0x4005 6000 (USART1)

### 14.11.1 USART n Receiver Buffer register (USARTn\_RB) (n=0,1)

Address Offset: 0x00

This register is the top byte of the USART RX FIFO, and contains the oldest character received and can be read via the bus interface. The LSB (bit 0) contains the first-received data bit. If the character received is less than 8 bits, the unused MSBs are padded with zeros.

The Divisor Latch Access Bit (DLAB) in the [USARTn\\_LC](#) register must be zero in order to access this register.

Since PE, FE and BI bits correspond to the byte on the top of the USART RX FIFO (i.e. the one that will be read in the next read from this register), the right approach for fetching the valid pair of received byte and its status bits is first to read the content of the [USARTn\\_LS](#) register, and then to read a byte from this register.

| Bit  | Name     | Description                                             | Attribute | Reset |
|------|----------|---------------------------------------------------------|-----------|-------|
| 31:8 | Reserved |                                                         | R         | 0     |
| 7:0  | RB[7:0]  | Contains the oldest received byte in the USART RX FIFO. | R         | 0     |

### 14.11.2 USART n Transmitter Holding register (USARTn\_TH) (n=0,1)

Address Offset: 0x00

This register is the top byte of the USART TX FIFO. The top byte is the newest character in the TX FIFO and can be written via the bus interface. The LSB represents the first bit to transmit.

The Divisor Latch Access Bit (DLAB) in [USARTn\\_LC](#) register must be zero in order to access this register.

| Bit  | Name     | Description                                                                                   | Attribute | Reset |
|------|----------|-----------------------------------------------------------------------------------------------|-----------|-------|
| 31:8 | Reserved |                                                                                               | R         | 0     |
| 7:0  | TH[7:0]  | The byte will be sent when it is the oldest byte in TX FIFO and the transmitter is available. | W         | 0     |

### 14.11.3 USART n Divisor Latch LSB registers (USARTn\_DLL) (n =0,1)

Address Offset: 0x00

The USART Divisor Latch is part of the USART Baud Rate Generator and holds the value used (optionally with the Fractional Divider) to divide the USARTn\_PCLK clock in order to produce the baud rate clock, which must be the multiple of the desired baud rate that is specified by the Oversampling Register (typically 16X).

The USARTn\_DLL and USARTn\_DLM registers together form a 16-bit divisor, and DLAB bit in [USARTn\\_LC](#) register must be one in order to access these registers.

DLL contains the lower 8 bits of the divisor and DLM contains the higher 8 bits. A zero value is treated like 0x0001.

| Bit  | Name     | Description                                                                                               | Attribute | Reset |
|------|----------|-----------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:8 | Reserved |                                                                                                           | R         | 0     |
| 7:0  | DLL[7:0] | The USART Divisor Latch LSB Register, along with the DLM register, determines the baud rate of the USART. | R/W       | 0     |

### 14.11.4 USART n Divisor Latch MSB register (USARTn\_DLM) (n=0,1)

Address Offset: 0x04

| Bit         | Name     | Description                                                                                               | Attribute | Reset |
|-------------|----------|-----------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:8</b> | Reserved |                                                                                                           | R         | 0     |
| <b>7:0</b>  | DLM[7:0] | The USART Divisor Latch MSB Register, along with the DLL register, determines the baud rate of the USART. | R/W       | 0     |

### 14.11.5 USART n Interrupt Enable register (USARTn\_IE) (n=0,1)

Address Offset: 0x04

The DLAB bit in the [USARTn\\_LC](#) register must be zero in order to access this register.

| Bit          | Name     | Description                                                                                                                                                      | Attribute | Reset |
|--------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:11</b> | Reserved |                                                                                                                                                                  | R         | 0     |
| <b>10</b>    | TXERRIE  | TXERR interrupt enable bit<br>The status of this interrupt can be read from TXERR bit in USARTn_LS register.<br>0: Disable<br>1: Enable                          | R/W       | 0     |
| <b>9</b>     | ABTOIE   | Enables the auto-baud time-out interrupt enable bit.<br>0: Disable<br>1: Enable                                                                                  | R/W       | 0     |
| <b>8</b>     | ABEOIE   | End of auto-baud interrupt enable bit.<br>0: Disable<br>1: Enable                                                                                                | R/W       | 0     |
| <b>7:5</b>   | Reserved |                                                                                                                                                                  | R         | 0     |
| <b>4</b>     | TEMTIE   | TEMT interrupt enable bit.<br>The status of this interrupt can be read from TEMT bit in USARTn_LS register.<br>0: Disable<br>1: Enable                           | R/W       | 0     |
| <b>3</b>     | MSIE     | Modem Status interrupt enable bit. The components of this interrupt can be read from USARTn_MS register.<br>0: Disable<br>1: Enable                              | R/W       | 0     |
| <b>2</b>     | RLSIE    | Receive Line Status (RLS) interrupt enable bit.<br>The status of this interrupt can be read from <a href="#">USARTn_LS</a> [4:1].<br>0: Disable<br>1: Enable     | R/W       | 0     |
| <b>1</b>     | THREIE   | THRE interrupt enable bit.<br>The status of this interrupt can be read from THRE bit in <a href="#">USARTn_LS</a> register.<br>0: Disable<br>1: Enable           | R/W       | 0     |
| <b>0</b>     | RDAIE    | RDA interrupt enable bit.<br>Enables the Receive Data Available interrupt. It also controls the Character Receive Time-out interrupt.<br>0: Disable<br>1: Enable | R/W       | 0     |

### 14.11.6 USART n Interrupt Identification register (USARTn\_II) (n=0,1)

Address Offset: 0x08

This register provides a status code that denotes the priority and source of a pending interrupt. The interrupts are frozen during a USARTn\_II register access. If an interrupt occurs during a USARTn\_II register access, the interrupt is recorded for the next USARTn\_II register access.

| Bit | Name | Description | Attribute | Reset |
|-----|------|-------------|-----------|-------|
|-----|------|-------------|-----------|-------|

|              |            |                                                                                                                                                                                                                                                                                                                                     |   |   |
|--------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|---|
| <b>31:11</b> | Reserved   |                                                                                                                                                                                                                                                                                                                                     | R | 0 |
| <b>10</b>    | TXERRIF    | TXERR interrupt flag<br>0: TXERR has not occurred.<br>1: TXERR has occurred and interrupt is enabled.                                                                                                                                                                                                                               | R | 0 |
| <b>9</b>     | ABTOIF     | Auto-baud time-out interrupt flag.<br>0: Auto-baud has not timed-out<br>1: Auto-baud has timed out and interrupt is enabled.                                                                                                                                                                                                        | R | 0 |
| <b>8</b>     | ABEOIF     | End of auto-baud interrupt flag<br>0: Auto-baud has not finished.<br>1: Auto-baud has finished successfully and interrupt is enabled.                                                                                                                                                                                               | R | 0 |
| <b>7:6</b>   | FIFOEN     | Equivalent to FIFOEN bit in <a href="#">USARTn_FIFOCtrl</a> register.                                                                                                                                                                                                                                                               | R | 1 |
| <b>5:4</b>   | Reserved   |                                                                                                                                                                                                                                                                                                                                     | R | 0 |
| <b>3:1</b>   | INTID[2:0] | Interrupt identification which identifies an interrupt corresponding to the USARTn RX FIFO.<br>0x3: 1 - Receive Line Status (RLS).<br>0x2: 2a - Receive Data Available (RDA).<br>0x6: 2b - Character Time-out Indicator (CTI).<br>0x1: 3a - THRE Interrupt.<br>0x0: 4 - Modem status<br>0x7: 3b – TEMT Interrupt<br>Other: Reserved | R | 0 |
| <b>0</b>     | INTSTATUS  | Interrupt status. The pending interrupt can be determined by evaluating USARTn_I[3:1].<br>0: At least one interrupt is pending.<br>1: No interrupt is pending.                                                                                                                                                                      | R | 1 |

Bits USARTn\_I[9:8] are set by the auto-baud function and signal a time-out or end of auto-baud condition. The auto-baud interrupt conditions are cleared by setting the corresponding Clear bits in the Auto-baud Control Register.

Given the status of USARTn\_I[3:0], an interrupt handler routine can determine the cause of the interrupt and how to clear the active interrupt. The USARTn\_I register must be read in order to clear the interrupt prior to exiting the Interrupt service routine.

| Interrupt | USARTn_I [3:0] | Priority        | Interrupt Source                                                                                                                                                                                             | Interrupt Reset                                                       |
|-----------|----------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------|
| RLS       | 0110           | Highest         | Overrun error (OE), Parity error (PE), Framing error (FE) or Break interrupt (BI)                                                                                                                            | Read USARTn_LS register                                               |
| RDA       | 0100           | 2 <sup>nd</sup> | RX data in FIFO reached trigger level (FCR0=1)                                                                                                                                                               | Read USARTn_RB register or USART FIFO drops below trigger level       |
| CTI       | 1100           | 2 <sup>nd</sup> | Minimum of one character in the RX FIFO and no character input or removed during a time period depending on how many characters are in FIFO and what the trigger level is set at 3.5 to 4.5 character times. | Read USARTn_RB register                                               |
| THRE      | 0010           | 3 <sup>rd</sup> | THRE                                                                                                                                                                                                         | Read USARTn_I register (if source of interrupt) or Write THR register |
| MS        | 0000           | Lowest          | CTS, DSR, RI, or DCD.                                                                                                                                                                                        | MSR Read                                                              |
| TEMT      | 1110           | 3 <sup>rd</sup> | TEMT                                                                                                                                                                                                         | Read USARTn_I register (if source of interrupt) or Write THR register |

### 14.11.7 USART n Line Status register (USARTn\_LS) (n=0,1)

Address Offset: 0x14

- \* Note:**
- \* *The break interrupt (BI) is associated with the character at the top of the USARTn\_RB FIFO.*
  - \* *The framing error (FE) is associated with the character at the top of the USARTn\_RB FIFO.*
  - \* *The parity error (PE) is associated with the character at the top of the USARTn\_RB FIFO.*

| Bit  | Name     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Attribute | Reset |
|------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:9 | Reserved |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | R         | 0     |
| 8    | TXERR    | TX Error flag. (Only available in smart card T=0 operation)<br>0: No TX Error.<br>1: Smart card has NACKed a transmitted character, one more than the number of times indicated by the TXRETRY field.                                                                                                                                                                                                                                                                                                                                                                                               | R         | 0     |
| 7    | RXFE     | Error in RX FIFO flag.<br>RXFE =1 when a character with a RX error such as framing error, parity error, or break interrupt, is loaded into the USARTn_RB register. This bit is cleared when the USARTn_LS register is read and there are no subsequent errors in the USART FIFO.<br>0: USARTn_RB register contains no USART RX errors or FIFOEN=0<br>1: USARTn_RB register contains at least one USART RX error.                                                                                                                                                                                    | R         | 0     |
| 6    | TEMT     | Transmitter Empty flag<br>TEMT=1 when both THR and TSR are empty; TEMT is cleared when either the TSR or the THR contain valid data.<br>0: THR and/or TSR contains valid data.<br>1: THR and TSR are empty.                                                                                                                                                                                                                                                                                                                                                                                         | R         | 1     |
| 5    | THRE     | Transmitter Holding Register Empty flag<br>THRE indicates that the USART is ready to accept a new character for transmission. In addition, this bit causes the USART to issue THRE interrupt to if THREIE=1. THRE=1 when a character is transferred from the THR into the TSR. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.<br>0: THR contains valid data.<br>1: THR (TX FIFO) is empty.                                                                                                                                               | R         | 1     |
| 4    | BI       | Break Interrupt flag.<br>When RXD1 is held in the spacing state (all zeros) for one full character transmission (start, data, parity, stop), a break interrupt occurs. Once the break condition has been detected, the receiver goes idle until RXD1 goes to marking state (all ones). A USARTn_LS register read clears BI bit. The time of break detection is dependent on FIFOEN bit in USARTn_FIFOCtrl register.<br>0: Break interrupt status is inactive.<br>1: Break interrupt status is active.                                                                                               | R         | 0     |
| 3    | FE       | Framing Error flag.<br>When the stop bit of a received character is a logic 0, a framing error occurs. A USARTn_LS register read clears FE bit. The time of the framing error detection is dependent on FIFOEN bit in USARTn_FIFOCtrl register.<br>Upon detection of a framing error, the RX will attempt to re-synchronize to the data and assume that the bad stop bit is actually an early start bit. However, it cannot be assumed that the next received byte will be correct even if there is no Framing Error.<br>0: Framing error status is inactive.<br>1: Framing error status is active. | R         | 0     |
| 2    | PE       | Parity Error flag.<br>When the parity bit of a received character is in the wrong state, a parity error occurs. A USARTn_LS register read clears PE bit. Time of parity error detection is dependent on FIFOEN bit in USARTn_FIFOCtrl register.<br>0: Parity error status is inactive.<br>1: Parity error status is active.                                                                                                                                                                                                                                                                         | R         | 0     |

|          |            |                                                                                                                                                                                                                                                                                                                                                                                                                                |          |          |
|----------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|----------|
| <b>1</b> | <b>OE</b>  | <p>Overrun Error flag.</p> <p>The overrun error condition is set as soon as it occurs. A USARTn_LS register read clears OE bit. OE=1 when USART RSR has a new character assembled and the USARTn_RB FIFO is full. In this case, the USARTn_RB FIFO will not be overwritten and the character in the USARTn_RS register will be lost.</p> <p>0: Overrun error status is inactive.</p> <p>1: Overrun error status is active.</p> | <b>R</b> | <b>0</b> |
| <b>0</b> | <b>RDR</b> | <p>Receiver Data Ready flag</p> <p>RDR=1 when the USARTn_RB FIFO holds an unread character and is cleared when the USARTn_RB FIFO is empty.</p> <p>0: USARTn_RB FIFO is empty.</p> <p>1: USARTn_RB FIFO contains valid data.</p>                                                                                                                                                                                               | <b>R</b> | <b>0</b> |

### 14.11.8 USART n FIFO Control register (USARTn\_FIFOCtrl) (n=0,1)

Address Offset: 0x08

This register controls the operation of the USART RX and TX FIFOs.

| Bit         | Name      | Description                                                                                                                                                                                                                                                                                                         | Attribute | Reset    |
|-------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|----------|
| <b>31:8</b> | Reserved  |                                                                                                                                                                                                                                                                                                                     | <b>R</b>  | <b>0</b> |
| <b>7:6</b>  | RXTL[1:0] | <p>RX Trigger Level. These two bits determine how many receiver USART FIFO characters must be written before an interrupt is activated.</p> <p>00: Trigger level 0 (1 character)</p> <p>01: Trigger level 1 (4 characters)</p> <p>10: Trigger level 2 (8 characters)</p> <p>11: Trigger level 3 (14 characters)</p> | <b>W</b>  | <b>0</b> |
| <b>5:3</b>  | Reserved  |                                                                                                                                                                                                                                                                                                                     | <b>R</b>  | <b>0</b> |
| <b>2</b>    | TXFIFORST | <p>TX FIFO Reset bit.</p> <p>0: No impact on either of USART FIFOs.</p> <p>1: Writing a logic 1 to reset the pointer logic in USART TX FIFO. HW shall clear this bit automatically.</p>                                                                                                                             | <b>W</b>  | <b>0</b> |
| <b>1</b>    | RXFIFORST | <p>RX FIFO Reset bit.</p> <p>0: No impact on either of USART FIFOs.</p> <p>1: Writing a logic 1 to reset the pointer logic in USART RX FIFO. HW shall clear this bit automatically.</p>                                                                                                                             | <b>W</b>  | <b>0</b> |
| <b>0</b>    | FIFOEN    | <p>FIFO enable</p> <p>0: No effect</p> <p>1: Enable for both USART Rx and TX FIFOs and USARTn_FIFOCtrl [7:1] access. This bit must be set for proper USART operation.</p>                                                                                                                                           | <b>W</b>  | <b>1</b> |

### 14.11.9 USART n Line Control register (USARTn\_LC) (n=0,1)

Address Offset: 0x0C

This register determines the format of the data character that is to be transmitted or received.

| Bit         | Name     | Description                                                                                                                                    | Attribute  | Reset    |
|-------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------|------------|----------|
| <b>31:8</b> | Reserved |                                                                                                                                                | <b>R</b>   | <b>0</b> |
| <b>7</b>    | DLAB     | <p>Divisor Latch Access bit</p> <p>0: Disable access to Divisor Latches.</p> <p>1: Enable access to Divisor Latches.</p>                       | <b>R/W</b> | <b>0</b> |
| <b>6</b>    | BC       | <p>Break Control bit</p> <p>0: Disable break transmission.</p> <p>1: Enable break transmission. Output pin USART TXD is forced to logic 0.</p> | <b>R/W</b> | <b>0</b> |

|            |                 |                                                                                                                                                                                                                                                                                              |     |   |
|------------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---|
| <b>5:4</b> | <b>PS[1:0]</b>  | Parity Select bits<br>00: Odd parity. Number of 1s in the transmitted character and the attached parity bit will be odd.<br>01: Even Parity. Number of 1s in the transmitted character and the attached parity bit will be even.<br>10: Forced 1 stick parity.<br>11: Forced 0 stick parity. | R/W | 0 |
| <b>3</b>   | <b>PE</b>       | Parity Enable bit<br>0: Disable parity generation and checking.<br>1: Enable parity generation and checking.                                                                                                                                                                                 | R/W | 0 |
| <b>2</b>   | <b>SBS</b>      | Stop Bit Select bit<br>0: 1 stop bit.<br>1: 2 stop bits (1.5 if WLS bits=00). Must be 1 in Smart card mode.                                                                                                                                                                                  | R/W | 0 |
| <b>1:0</b> | <b>WLS[1:0]</b> | Word Length Select bits<br>00: 5-bit character length.<br>01: 6-bit character length.<br>10: 7-bit character length.<br>11: 8-bit character length.                                                                                                                                          | R/W | 0 |

#### 14.11.10 USART n Modem Control register (USARTn\_MC) (n=0,1)

Address Offset: 0x10

This register enables the modem loopback mode and controls the modem output signals.

| Bit         | Name           | Description                                                                             | Attribute | Reset |
|-------------|----------------|-----------------------------------------------------------------------------------------|-----------|-------|
| <b>31:8</b> | Reserved       |                                                                                         | R         | 0     |
| <b>7</b>    | <b>CTSEN</b>   | CTS enable bit<br>0: Disable Auto-CTS flow control.<br>1: Enable Auto-CTS flow control. | R/W       | 0     |
| <b>6</b>    | <b>RTSEN</b>   | RTS enable bit<br>0: Disable Auto-RTS flow control.<br>1: Enable Auto-RTS flow control. | R/W       | 0     |
| <b>5:2</b>  | Reserved       |                                                                                         | R         | 0     |
| <b>1</b>    | <b>RTSCTRL</b> | Source for modem output pin <u>RTS</u> .                                                | R/W       | 0     |
| <b>0</b>    | Reserved       |                                                                                         | R         | 0     |

#### 14.11.11 USART n Modem Status register (USARTn\_MS) (n=0,1)

Address Offset: 0x18

This register is a read-only register that provides status information on USART input signals.

**\* Note:** Whenever the CTS bit changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

| Bit         | Name        | Description                                                                                                                                                                                                 | Attribute | Reset |
|-------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:5</b> | Reserved    |                                                                                                                                                                                                             | R         | 0     |
| <b>4</b>    | <b>CTS</b>  | Clear To Send State.<br>Complement of input signal <u>CTS</u> . This bit is connected to USARTn_MC[1] in modem loopback mode.                                                                               | R         | 0     |
| <b>3:1</b>  | Reserved    |                                                                                                                                                                                                             | R         | 0     |
| <b>0</b>    | <b>DCTS</b> | Delta CTS.<br>Set upon state change of input <u>CTS</u> . Cleared after reading this register.<br>0: No change detected on modem input <u>CTS</u> .<br>1: State change detected on modem input <u>CTS</u> . | R         | 0     |

**14.11.12 USART n Scratch Pad register (USARTn\_SP) (n=0,1)**

Address Offset: 0x1C

This register has no effect on the USART operation. This register can be written and/or read at user's discretion. There is no provision in the interrupt interface that would indicate to the host that a read or write of this register has occurred.

| Bit  | Name     | Description                | Attribute | Reset |
|------|----------|----------------------------|-----------|-------|
| 31:8 | Reserved |                            | R         | 0     |
| 7:0  | PAD[7:0] | A readable, writable byte. | R/W       | 0     |

**14.11.13 USART n Auto-baud Control register (USARTn\_ABCTRL) (n=0,1)**

Address Offset: 0x20

This register controls the process of measuring the incoming clock/data rate for the baud rate generation and can be read and written at user's discretion. Besides, it also controls the clock pre-scaler for the baud rate generation. The reset value of the register keeps the fractional capabilities of USART disabled making sure that USART is fully SW and HW compatible with USARTs not equipped with this feature.

| Bit   | Name        | Description                                                                                                                                                                                                                                         | Attribute | Reset |
|-------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:10 | Reserved    |                                                                                                                                                                                                                                                     | R         | 0     |
| 9     | ABTOIFC     | Auto-baud time-out interrupt flag clear bit<br>0: No effect<br>1: Clear ABTOIF bit. This bit is automatically cleared by HW.                                                                                                                        | W         | 0     |
| 8     | ABEOIFC     | End of auto-baud interrupt flag clear bit<br>0: No effect.<br>1: Clear ABEOIF bit. This bit is automatically cleared by HW.                                                                                                                         | W         | 0     |
| 7:3   | Reserved    |                                                                                                                                                                                                                                                     | R         | 0     |
| 2     | AUTORESTART | Restart mode<br>0: No restart<br>1: Restart in case of timeout (counter restarts at next USART RX falling edge)                                                                                                                                     | R/W       | 0     |
| 1     | MODE        | Auto-baud mode select bit.<br>0: Mode 0.<br>1: Mode 1.                                                                                                                                                                                              | R/W       | 0     |
| 0     | START       | This bit is automatically cleared after auto-baud completion.<br>0: Auto-baud stop (auto-baud is not running).<br>1: Auto-baud start (auto-baud is running). Auto-baud run bit. This bit is automatically cleared by HW after auto-baud completion. | R/W       | 0     |

**14.11.14 USART n Fractional Divider register (USARTn\_FD) (n=0,1)**

Address Offset: 0x28

This register controls the clock prescaler for the baud rate generation and can be read and written at the user's discretion. This prescaler takes the APB clock and generates an output clock according to the specified fractional requirements.

In most applications, the USART samples received data 16 times in each nominal bit time, and sends bits that are 16 input clocks wide. OVER8 bit allows software to control the ratio between the input clock and bit clock. This is required for smart card mode, and provides an alternative to fractional division for other modes.

**\* Note:**

**1. If the fractional divider is active (DIVADDVAL>0) and USARTn\_DLM=0, the value of the**

**USARTn\_DLL register must  $\geq 3$ .**  
**2. MUL – DIVADDVAL  $\neq 2$ , so MULVAL[3:0] – DIVADDVAL[3:0]  $\neq 1$ .**

| Bit  | Name           | Description                                                                                                                                                                                                                                                 | Attribute | Reset |
|------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:9 | Reserved       |                                                                                                                                                                                                                                                             | R         | 0     |
| 8    | OVER8          | Oversampling value<br>0: Oversampling by 16<br>1: Oversampling by 8 (Not supported for IrDA mode)                                                                                                                                                           | R/W       | 0     |
| 7:4  | MULVAL[3:0]    | Baud rate pre-scaler multiplier value MUL = MULVAL[3:0] +1<br>0000: Baud rate pre-scaler multiplier value is 1 for HW<br>0001: Baud rate pre-scaler multiplier value is 2 for HW<br>...<br>...<br>1111: Baud rate pre-scaler multiplier value is 16 for HW. | R/W       | 0     |
| 3:0  | DIVADDVAL[3:0] | Baud rate generation pre-scaler divisor value. If this field is 0, fractional baud rate generator will not impact the USART baud rate                                                                                                                       | R/W       | 0     |

#### 14.11.15 USART n Control register (USARTn\_CTRL) (n=0,1)

Address Offset: 0x30

In addition to HW flow control (Auto-CTS and Auto-RTS mechanisms), this register enables implementation of SW flow control.

When TXEN = 1, the USART transmitter will keep sending data as long as they are available. As soon as TXEN bit becomes 0, USART transmission will stop.

It is strongly suggested to let the USART HW implemented auto flow control features take care of limit the scope of TXEN to SW flow control.

**\* Note: It is advised that TXEN and RXEN are set in the same instruction if needed in order to minimize the setup and the hold time of the receiver.**

| Bit  | Name      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Attribute | Reset |
|------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:8 | Reserved  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | R         | 0     |
| 7    | TXEN      | When this bit is 1, data written to the USARTn_TH register is output on the TXD pin as soon as any preceding data has been sent.<br>If this bit is cleared to 0 while a character is being sent, the transmission of that character is completed, but no further characters are sent until this bit is set again.<br>In other words, a 0 in this bit blocks the transfer of characters from the USARTn_TH register or TX FIFO into the transmit shift register. SW can clear this bit when it detects that the HW-handshaking TX-permit signal (CTS) has gone false, or with SW handshaking, when it receives an XOFF character (DC3). SW can set this bit again when it detects that the TX-permit signal has gone true, or when it receives an XON (DC1) character. | R/W       | 1     |
| 6    | RXEN      | 0: Disable RX related function<br>1: Enable RX                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | R/W       | 1     |
| 5:4  | Reserved  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | R         | 0     |
| 3:1  | MODE[2:0] | USARTn Mode<br>000: UART mode. HW will switch GPIO to UTXDn and URXDn.<br>001: Modem mode. HW will switch GPIO to UTXDn, URXDn, UDSRn, UCTS <sub>n</sub> , UDCDn, URIn, UDTRn and URTSn.<br>010: Reserved<br>011: Smart Card mode. HW will switch GPIO to UTXDn, and enable UTXDn pin with open-drain.<br>100: Synchronous mode. HW will switch GPIO to UTXDn, URXDn , and USCLK pin.                                                                                                                                                                                                                                                                                                                                                                                 | R/W       | 0     |

|   |         |                                                                                                                                                   |     |   |
|---|---------|---------------------------------------------------------------------------------------------------------------------------------------------------|-----|---|
|   |         | 101:RS-485 mode. HW will switch GPIO to UTXDn, URXDn pin.                                                                                         |     |   |
| 0 | USARTEN | USART enable<br>0: Disable . All USART shared pins act as GPIO.<br>1: Enable. HW switches GPIO to USART pin according to MODE bits automatically. | R/W | 0 |

#### 14.11.16 USART n Half-duplex Enable register (USARTn\_HDEN) (n=0,1)

Address Offset: 0x34

After reset the USART will be in full-duplex mode, meaning that both TX and RX work independently. After setting the HDEN bit, the USART will be in half-duplex mode. In this mode, the USART ensures that the receiver is locked when idle, or will enter a locked state after having received a complete ongoing character reception. Line conflicts must be handled in SW.

The behavior of the USART is unpredictable when data is presented for reception while data is being transmitted. For this reason, the value of the HDEN register should not be modified while sending or receiving data, or data may be lost or corrupted.

**\* Note: This register should be disabled when in smart card mode or IrDA mode (Smart card and IrDA by default run in half-duplex mode).**

| Bit  | Name     | Description                                            | Attribute | Reset |
|------|----------|--------------------------------------------------------|-----------|-------|
| 31:1 | Reserved |                                                        | R         | 0     |
| 0    | HDEN     | Half-duplex mode enable bit<br>0: Disable<br>1: Enable | R/W       | 0     |

#### 14.11.17 USART n Smart card Interface Control register (USARTn\_SCICTRL) (n=0,1)

Address Offset: 0x38

| Bit   | Name         | Description                                                                                                                                                                                                                                                                                                                                                      | Attribute | Reset |
|-------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:24 | Reserved     |                                                                                                                                                                                                                                                                                                                                                                  | R         | 0     |
| 23:16 | TC[7:0]      | Count for SCLK clock cycle when SCLKEN=1. SCLK will toggle every (TC[7:0]+1) * USARTn_PCLK cycle                                                                                                                                                                                                                                                                 | R/W       | 0x0   |
| 15:8  | XTRAGUARD    | When the protocol selection T= 0, this field indicates the number of bit times (ETUs) by which the guard time after a character transmitted by the USART should exceed the nominal 2 bit times. 0xFF in this field may indicate that there is just a single bit after a character and 11 bit times/character                                                     | R/W       | N/A   |
| 7:5   | TXRETRY[2:0] | When the protocol selection T = 0, the field controls the maximum number of retransmissions that the USART will attempt if the remote device signals NACK. When NACK has occurred this number of times plus one, the TX Error (TXERR) bit in USARTn_LS register is set, an interrupt is requested if enabled, and the USART is locked until the FIFO is cleared. | R/W       | N/A   |
| 4     | Reserved     |                                                                                                                                                                                                                                                                                                                                                                  | R         | 0     |
| 3     | SCLKEN       | SCLK enable<br>Enable if the smart card to be communicated with requires a clock.<br>0: Disable<br>1: Enable. HW will switch GPIO to UnSCLK pin.                                                                                                                                                                                                                 | R/W       | 0     |
| 2     | PROTSEL      | Protocol selection as defined in the ISO7816-3 standard.<br>0: T = 0<br>1: T = 1                                                                                                                                                                                                                                                                                 | R/W       | 0     |
| 1     | NACKDIS      | NACK response disable bit. Only applicable in T=0.<br>0: A NACK response is enabled.<br>1: A NACK response is inhibited.                                                                                                                                                                                                                                         | R/W       | 0     |

|   |          |  |   |   |
|---|----------|--|---|---|
| 0 | Reserved |  | R | 0 |
|---|----------|--|---|---|

### 14.11.18 USART n RS485 Control register (USARTn\_RS485CTRL) (n=0,1)

Address Offset: 0x3C

| Bit  | Name     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Attribute | Reset |
|------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:6 | Reserved |                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | R         | 0     |
| 5    | OINV     | Polarity control. This bit reverses the polarity of the direction control signal on the <u>RTS</u> pin.<br>0: The direction control pin will be driven to logic 0 when the transmitter has data to be sent. It will be driven to logic 1 after the last bit of data has been transmitted.<br>1: The direction control pin will be driven to logic 1 when the transmitter has data to be sent. It will be driven to logic 0 after the last bit of data has been transmitted. | R/W       | 0     |
| 4    | ADCEN    | Auto Direction control enable bit.<br>0: Disable<br>1: Enable. <u>RTS</u> pin is used for direction control. HW will switch GPIO to <u>URTSn</u> pin automatically.                                                                                                                                                                                                                                                                                                         | R/W       | 0     |
| 3    | Reserved |                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | R         | 0     |
| 2    | AADEN    | Auto Address Detect (AAD) enable bit.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                                                                            | R/W       | 0     |
| 1    | RXEN     | RS-485/EIA-485 Receiver enable bit. (Only work when NMMEN = 1)<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                                                   | R/W       | 0     |
| 0    | NMMEN    | RS-485/EIA-485 Normal Multidrop Mode (NMM) enable bit.<br>0: Disable<br>1: Enable. In this mode, an address is detected when a received byte causes the USART to set the parity error and generate an interrupt.                                                                                                                                                                                                                                                            | R/W       | 0     |

### 14.11.19 USART n RS485 Address Match register (USARTn\_RS485ADRMATCH) (n=0,1)

Address Offset: 0x40

This register contains the address match value for RS-485/EIA-485 mode.

| Bit  | Name       | Description                      | Attribute | Reset |
|------|------------|----------------------------------|-----------|-------|
| 31:8 | Reserved   |                                  | R         | 0     |
| 7:0  | MATCH[7:0] | The address value to be matched. | R/W       | 0     |

### 14.11.20 USART n RS485 Delay Value register (USARTn\_RS485DLYV) (n=0,1)

Address Offset: 0x44

The user may program this register with a delay between the last stop bit leaving the TXFIFO and the de-assertion of RTS. This delay time is in periods of the baud clock. Any delay time from 0 to 255 bit times may be programmed.

| Bit  | Name     | Description                                                                                        | Attribute | Reset |
|------|----------|----------------------------------------------------------------------------------------------------|-----------|-------|
| 31:8 | Reserved |                                                                                                    | R         | 0     |
| 7:0  | DLY[7:0] | The direction control (RTS) delay value. This register works in conjunction with an 8-bit counter. | R/W       | 0     |

**14.11.21 USART n Synchronous Mode Control Register (USARTn\_SYNCCTRL)  
(n=0,1)**

Address Offset: 0x48

This register controls the synchronous mode. When this mode is in effect, the USART generates or receives a bit clock on the SCLK pin and applies it to transmit and receive shift registers.  
Synchronous mode should not be used with smart card mode.

| Bit  | Name     | Description                                                                                                     | Attribute | Reset |
|------|----------|-----------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:3 | Reserved |                                                                                                                 | R         | 0     |
| 2    | CPHA     | Clock phase for edge sampling.<br>0: Sample on the rising edge of SCLK<br>1: Sample on the falling edge of SCLK | R/W       | 0     |
| 1    | CPOL     | Clock polarity selection bit<br>0: SCLK idles at Low level.<br>1: SCLK idles at High level.                     | R/W       | 0     |
| 0    | Reserved |                                                                                                                 | R         | 0     |

# 15 I2S

## 15.1 OVERVIEW

The I2S bus specification defines a 5-wire serial bus, having data in, data out, BCLK, MCLK, and word select signal. The basic I2S connection has one master, which is always the master, and one slave.

## 15.2 FEATURES

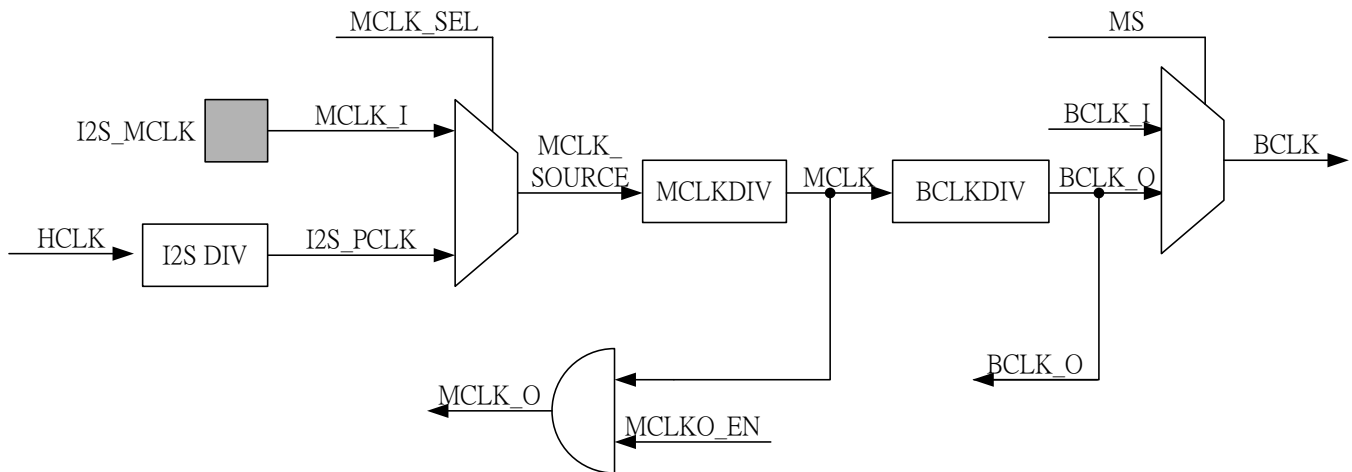
- I2S can operate as either master or slave.
- Capable of handling 8/16/24/32-bit data length.
- Mono and stereo audio data supported.
- I2S and MSB justified data format supported.
- 8 word (32-bit) FIFO data buffers are provided.
- Generate interrupt requests when buffer levels cross a programmable boundary.
- Controls include reset, stop and mute options separately for I2S input and I2S output.

## 15.3 PIN DESCRIPTION

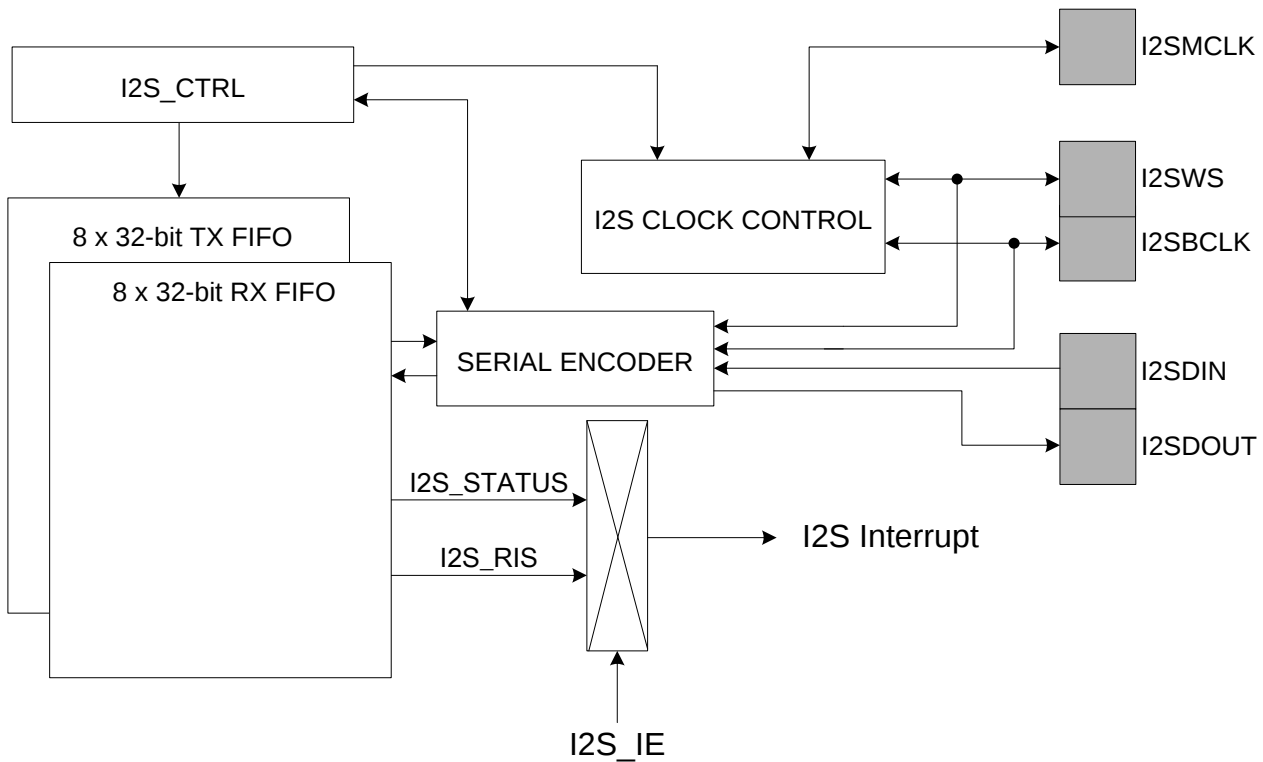
| Pin Name | Type | Description                      | GPIO Configuration   |
|----------|------|----------------------------------|----------------------|
| I2SBCLK  | O    | I2S Bit clock (Master)           |                      |
|          | I    | I2S Bit clock (Slave)            | Depends on GPIOn_CFG |
| I2SWS    | O    | I2S Word Select (Master)         |                      |
|          | I    | I2S Word Select (Slave)          | Depends on GPIOn_CFG |
| I2SDIN   | I    | I2S Received Serial data         | Depends on GPIOn_CFG |
| I2SDOUT  | O    | I2S Transmitted Serial data      |                      |
| I2SMCLK  | O    | I2S Master clock output          |                      |
|          | I    | I2S Master clock input from GPIO | Depends on GPIOn_CFG |

## 15.4 BLOCK DIAGRAM

### 15.4.1 I2S CLCOK CONTROL



### 15.4.2 I2S BLOCK DIAGRAM

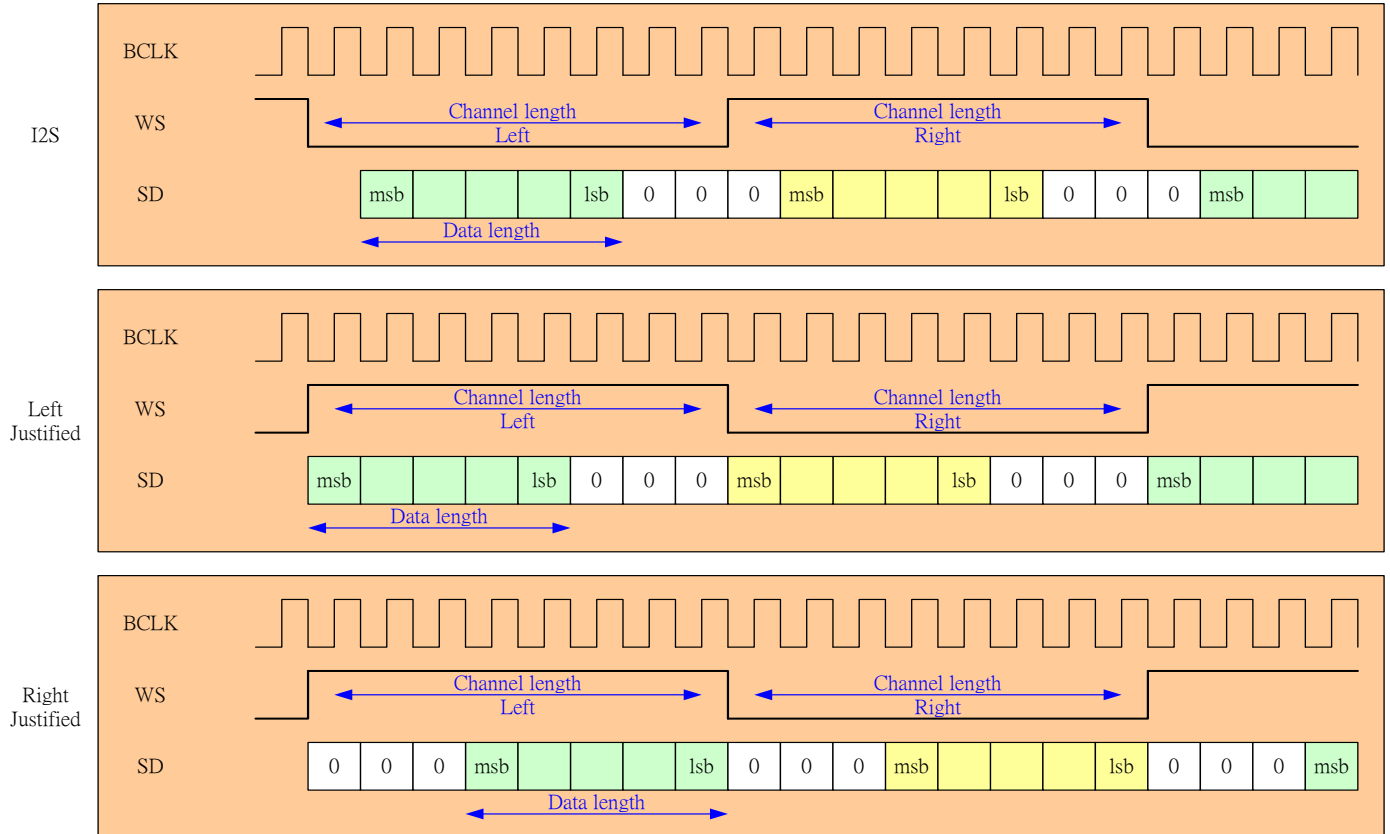


## 15.5 FUNCTIONAL DESCRIPTION

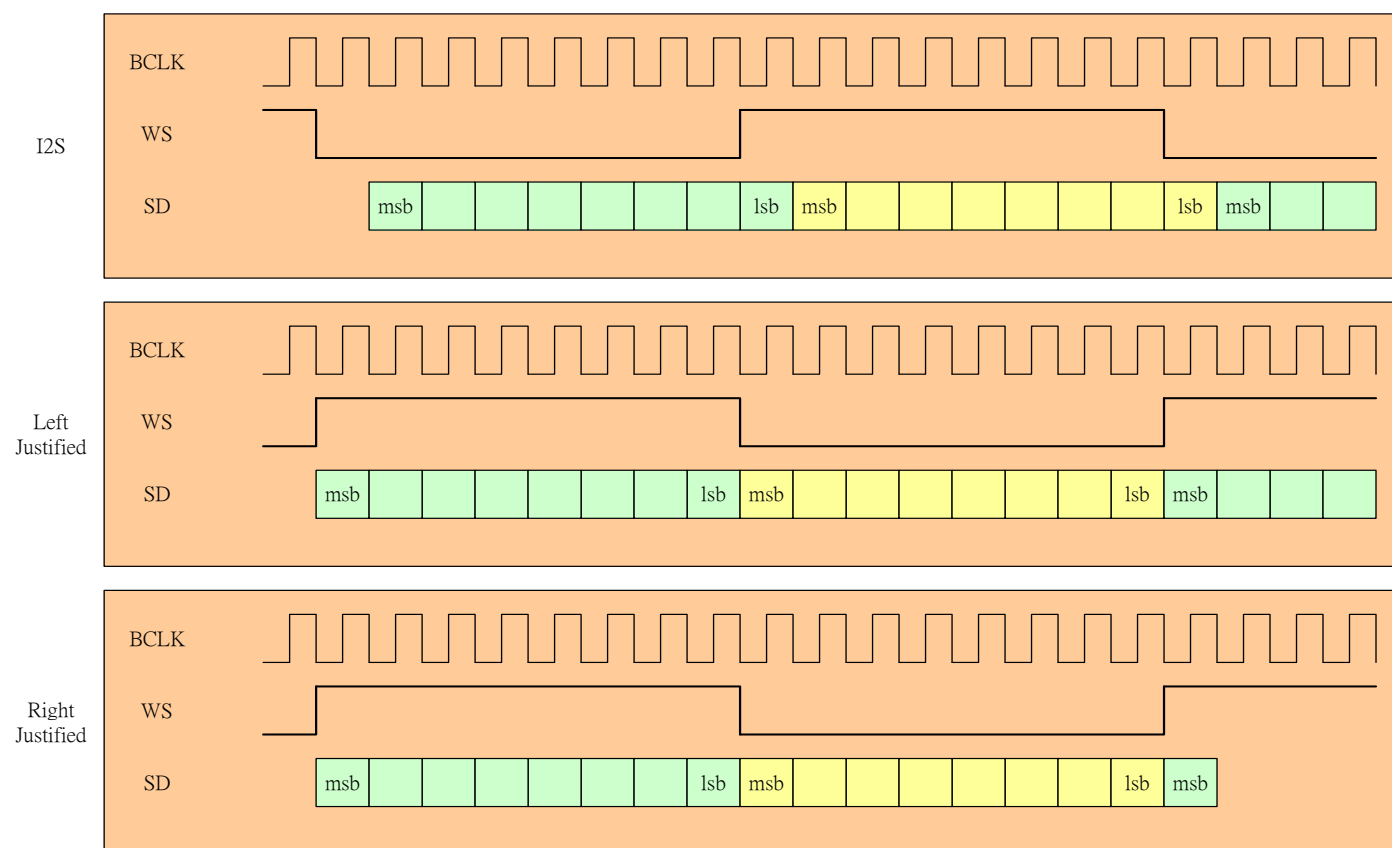
### 15.5.1 I2S OPERATION

- Standard I2S
- Right-justified Data Format
- MSB (Left)-justified Data Format

Channel Length > Data Length:



Channel Length = Data Length



## 15.5.2 I2S FIFO OPERAION

### 15.5.2.1 MONO

8bit

|     |     |     |     |
|-----|-----|-----|-----|
| N+3 | N+2 | N+1 | N   |
| N+7 | N+6 | N+5 | N+4 |

16bit

|     |     |
|-----|-----|
| N+1 | N   |
| N+3 | N+2 |

24 bit

|  |     |
|--|-----|
|  | N   |
|  | N+1 |

32 bit

|     |
|-----|
| N   |
| N+1 |

### 15.5.2.2 STEREO

8bit

|          |         |          |         |
|----------|---------|----------|---------|
| RIGHT +1 | LEFT +1 | RIGHT    | LEFT    |
| RIGHT +3 | LEFT +3 | RIGHT +2 | LEFT +2 |

16bit

|          |        |
|----------|--------|
| RIGHT    | LEFT   |
| RIGHT +1 | LEFT+1 |

24 bit

|  |       |
|--|-------|
|  | LEFT  |
|  | RIGHT |

32 bit

|       |
|-------|
| LEFT  |
| RIGHT |

## 15.6 I2S REGISTERS

Base Address: 0x4001 A000

### 15.6.1 I2S Control register (I2S\_CTRL)

Address Offset: 0x00

\* **Note: START bit shall be set at last.**

| Bit   | Name          | Description                                                                                                                                                                     | Attribute | Reset |
|-------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31    | I2SEN         | I2S enable bit<br>0: Disable<br>1: Enable                                                                                                                                       | R/W       | 0     |
| 30:25 | Reserved      |                                                                                                                                                                                 | R         | 0     |
| 24:20 | CHLENGTH[4:0] | Bit number of single channel = CHLENGTH[4:0]+1.<br>0~6: Reserved<br>7: 8 bits<br>8: 9 bits<br>...<br>...<br>31: 32bits (Max)                                                    | R/W       | 0x1F  |
| 19    | Reserved      |                                                                                                                                                                                 | R         | 0     |
| 18:16 | RXFIFOTH[2:0] | RX FIFO Threshold level<br>0: RX FIFO threshold level = 0<br>1: RX FIFO threshold level = 1<br>...<br>...<br>n: RX FIFO threshold level = n                                     | R/W       | 0x3   |
| 15    | Reserved      |                                                                                                                                                                                 | R         | 0     |
| 14:12 | TXFIFOTH[2:0] | TX FIFO Threshold level<br>0: TX FIFO threshold level = 0<br>1: TX FIFO threshold level = 1<br>...<br>...<br>n: TX FIFO threshold level = n                                     | R/W       | 0x3   |
| 11:10 | DL[1:0]       | Data Length<br>00: 8 bit<br>01: 16 bits<br>10: 24 bits<br>11: 32 bits                                                                                                           | R/W       | 0x1   |
| 9     | CLRRXFIFO     | Clear I2S RX FIFO<br>0: No effect.<br>1: Reset RX FIFO (RXFIFOLV bit becomes 0, RXFIFOEMPTY bit becomes 1, Data in RX FIFO will be cleared). This bit returns "0" automatically | W         | 0     |
| 8     | CLRTXFIFO     | Clear I2S TX FIFO<br>0: No effect.<br>1: Reset TX FIFO (TXFIFOLV bit becomes 0, TXFIFOEMPTY bit becomes 1, Data in TX FIFO will be cleared). This bit returns "0" automatically | W         | 0     |
| 7     | RXEN          | Receiver enable bit<br>0: Disable<br>1: Enable                                                                                                                                  | R/W       | 0     |
| 6     | TXEN          | Transmit enable bit<br>0: Disable<br>1: Enable                                                                                                                                  | R/W       | 0     |
| 5:4   | FORMAT[1:0]   | I2S operation format.<br>00: Standard I2S format                                                                                                                                | R/W       | 0     |

|          |              |                                                                                                                                                         |     |   |
|----------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---|
|          |              | 01: Left-justified format<br>10: Right(MSB)-justified format<br>11: Reserved                                                                            |     |   |
| <b>3</b> | <b>MS</b>    | Master/Slave selection bit<br>0: Act as Master using internally generated BCLK and WS signals.<br>1: Act as Slave using externally BCLK and WS signals. | R/W | 0 |
| <b>2</b> | <b>MONO</b>  | Mono/Stereo selection bit<br>0: Stereo<br>1: Mono                                                                                                       | R/W | 0 |
| <b>1</b> | <b>MUTE</b>  | Mute enable bit<br>0: Disable Mute<br>1: Enable. I2SSDA Output = 0                                                                                      | R/W | 0 |
| <b>0</b> | <b>START</b> | Start Transmit/Receive bit.<br>0: Disable<br>1: Start Transmit/Receive                                                                                  | R/W | 0 |

### 15.6.2 I2S Clock register (I2S\_CLK)

Address Offset: 0x04

| Bit          | Name                | Description                                                                                                                                         | Attribute | Reset |
|--------------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:17</b> | Reserved            |                                                                                                                                                     | R         | 0     |
| <b>16</b>    | <b>CLKSEL</b>       | I2S clock source selection<br>0: HCLK<br>1: EHS XTAL                                                                                                | R/W       | 0     |
| <b>15:8</b>  | <b>BCLKDIV[7:0]</b> | BCLK divider<br>0: BCLK = MCLK / 2<br>1: BCLK = MCLK / 4<br>2: BCLK = MCLK / 6<br>3: BCLK = MCLK / 8<br>...<br>...<br>n: BCLK = MCLK / (2*n + 2)    | R/W       | 1     |
| <b>7:5</b>   | Reserved            |                                                                                                                                                     | R         | 0     |
| <b>4</b>     | <b>MCLKSEL</b>      | MCLK source selection bit<br>0: MCLK source of master is from I2S_PCLK<br>1: MCLK source of master is from GPIO                                     | R/W       | 0     |
| <b>3</b>     | <b>MCLKOEN</b>      | MCLK output enable bit<br>0: Disable<br>1: Enable                                                                                                   | R/W       | 0     |
| <b>2:0</b>   | <b>MCLKDIV[2:0]</b> | MCLK divider<br>0: MCLK = MCLK source<br>1: MCLK = MCLK source / 2<br>2: MCLK = MCLK source / 4<br>...<br>...<br>n: MCLK = MCLK source / (2*n), n>0 | R/W       | 0     |

### 15.6.3 I2S Status register (I2S\_STATUS)

Address Offset: 0x08

| Bit          | Name                 | Description                                                                                                                                                         | Attribute | Reset |
|--------------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:21</b> | Reserved             |                                                                                                                                                                     | R         | 0     |
| <b>20:17</b> | <b>RXFIFOLV[3:0]</b> | RX FIFO used level<br>0000: 0/8 RX FIFO is used (Empty)<br>0001: 1/8 RX FIFO is used<br>0010: 2/8 RX FIFO is used<br>...<br>...<br>1000: 8/8 RX FIFO is used (Full) | R         | 0     |

|              |               |                                                                                                                                                                                        |   |   |
|--------------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|---|
|              |               | Other: Reserved                                                                                                                                                                        |   |   |
| <b>16</b>    | Reserved      |                                                                                                                                                                                        | R | 0 |
| <b>15:12</b> | TXFIFOLV[3:0] | TX FIFO used level<br>0000: 0/8 TX FIFO is used (Empty)<br>0001: 1/8 TX FIFO is used<br>0010: 2/8 TX FIFO is used<br>...<br>...<br>1000: 8/8 TX FIFO is used (Full)<br>Other: Reserved | R | 0 |
| <b>11</b>    | RXFIFOEMPTY   | RX FIFO empty flag<br>0: RX FIFO is not empty.<br>1: RX FIFO is empty. Data read from RX FIFO will be zero.                                                                            | R | 1 |
| <b>10</b>    | TXFIFOEMPTY   | TX FIFO empty flag<br>0: TX FIFO is not empty.<br>1: TX FIFO is empty.                                                                                                                 | R | 1 |
| <b>9</b>     | RXFIFOFULL    | RX FIFO full flag<br>0: RX FIFO is not full.<br>1: RX FIFO is full.                                                                                                                    | R | 0 |
| <b>8</b>     | TXFIFOFULL    | TX FIFO full flag<br>0: TX FIFO is not full.<br>1: TX FIFO is full. Write operation to TX FIFO will be ignored.                                                                        | R | 0 |
| <b>7</b>     | RXFIFOTHF     | RX FIFO threshold flag<br>0: RXFIFOLV $\leq$ RXFIFOTH<br>1: RXFIFOLV > RXFIFOTH                                                                                                        | R | 0 |
| <b>6</b>     | TXFIFOTHF     | TX FIFO threshold flag<br>0: TXFIFOLV $\geq$ TXFIFOTH<br>1: TXFIFOLV < TXFIFOTH                                                                                                        | R | 1 |
| <b>5:2</b>   | Reserved      |                                                                                                                                                                                        | R | 0 |
| <b>1</b>     | RIGHTCH       | Current channel status<br>0: Current channel is Left channel<br>1: Current channel is Right channel                                                                                    | R | 1 |
| <b>0</b>     | I2SINT        | I2S interrupt flag<br>0: No I2S interrupt<br>1: I2S interrupt occurs.                                                                                                                  | R | 0 |

#### 15.6.4 I2S Interrupt Enable register (I2S\_IE)

Address Offset: 0x0C

| Bit         | Name        | Description                                                       | Attribute | Reset |
|-------------|-------------|-------------------------------------------------------------------|-----------|-------|
| <b>31:8</b> | Reserved    |                                                                   | R         | 0     |
| <b>7</b>    | RXFIFOTHIE  | RX FIFO threshold interrupt enable bit<br>0: Disable<br>1: Enable | R/W       | 0     |
| <b>6</b>    | TXFIFOTHIE  | TX FIFO threshold interrupt enable bit<br>0: Disable<br>1: Enable | R/W       | 0     |
| <b>5</b>    | RXFIFOUDFIE | RX FIFO underflow interrupt enable bit<br>0: Disable<br>1: Enable | R/W       | 0     |
| <b>4</b>    | TXFIFOOVFIE | TX FIFO overflow interrupt enable bit<br>0: Disable<br>1: Enable  | R/W       | 0     |
| <b>3:0</b>  | Reserved    |                                                                   | R         | 0     |

#### 15.6.5 I2S Raw Interrupt Status register (I2S\_RIS)

Address Offset: 0x10

| Bit  | Name       | Description                                                                                                                  | Attribute | Reset |
|------|------------|------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:8 | Reserved   |                                                                                                                              | R         | 0     |
| 7    | RXFIFOTHIF | RX FIFO threshold interrupt flag<br>0: No RX FIFO threshold interrupt<br>1: RX FIFO threshold triggered.                     | R         | 0     |
| 6    | TXFIFOTHIF | TX FIFO threshold interrupt flag<br>0: No TX FIFO threshold interrupt<br>1: TX FIFO threshold triggered.                     | R         | 0     |
| 5    | RXFIFOUDIF | RX FIFO underflow interrupt flag<br>0: No RX FIFO underflow<br>1: RX FIFO underflow (RX FIFO is empty and still being read). | R         | 0     |
| 4    | TXFIFOOVIF | TX FIFO overflow interrupt flag<br>0: No TX FIFO overflow<br>1: TX FIFO overflow (TX FIFO is full and still being written).  | R         | 0     |
| 3:0  | Reserved   |                                                                                                                              | R         | 0     |

### 15.6.6 I2S Interrupt Clear register (I2S\_IC)

Address Offset: 0x14

| Bit  | Name       | Description                             | Attribute | Reset |
|------|------------|-----------------------------------------|-----------|-------|
| 31:8 | Reserved   |                                         | R         | 0     |
| 7    | RXFIFOTHIC | 0: No effect<br>1: Clear RXFIFOTHIF bit | W         | 0     |
| 6    | TXFIFOTHIC | 0: No effect<br>1: Clear TXFIFOTHIF bit | W         | 0     |
| 5    | RXFIFOUDIC | 0: No effect<br>1: Clear RXFIFOUDIF bit | W         | 0     |
| 4    | TXFIFOOVIC | 0: No effect<br>1: Clear TXFIFOOVIF bit | W         | 0     |
| 3:0  | Reserved   |                                         | R         | 0     |

### 15.6.7 I2S RXFIFO register (I2S\_RXFIFO)

Address Offset: 0x18

| Bit  | Name         | Description        | Attribute | Reset |
|------|--------------|--------------------|-----------|-------|
| 31:0 | RXFIFO[31:0] | 8 x 32-bit RX FIFO | R/W       | 0     |

### 15.6.8 I2S TXFIFO register (I2S\_TXFIFO)

Address Offset: 0x1C

| Bit  | Name         | Description        | Attribute | Reset |
|------|--------------|--------------------|-----------|-------|
| 31:0 | TXFIFO[31:0] | 8 x 32-bit TX FIFO | R/W       | 0     |

# 16 4x32 LCD DRIVER

## 16.1 OVERVIEW

The MCU builds in 4x32 (4 commons and up to 32 segments, 128 dots) LCD driver, includes R type and C type (1C and 4C) structures with 4 common pins and up to 32 segment pins. The LCD scan timing can support 1/2 duty, 1/3 duty, and 1/4 duty, besides, 1/2 bias or 1/3 bias structure are supported. Of these pins, all common and segment pins are shared with GPIO, and can be selected by programming LCD\_CTRL register. R type is using internal or external bias circuit to adjust LCD power and bias voltage. C type is using internal charge pump to adjust LCD power and bias voltage.

## 16.2 FEATURES

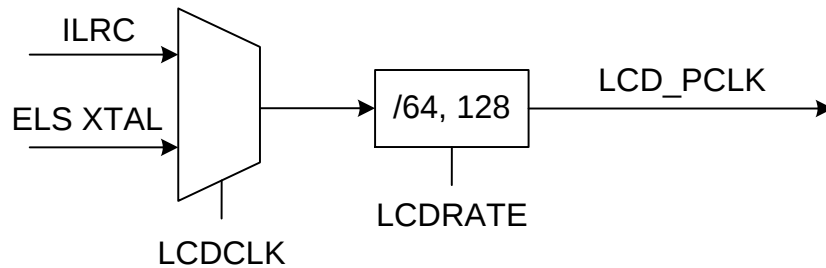
1. Support R/C-type
2. Support up to 128 (4 x 32) dots
3. Common 0~3 and Segment 0~31, V3, V2, CL+, CL- are all shared with GPI/O pins
4. Support 1/2 bias and 1/3 bias voltage
5. Support 1/2 duty, 1/3 duty, 1/4 duty
6. Configurable frame frequency
7. Internal Charge pump, adjustable contrast adjustment , and configurable charge pump frequency
8. Embedded LCD bias reference ladder (R-Type)
9. LCD frame interrupt

## 16.3 PIN DESCRIPTION

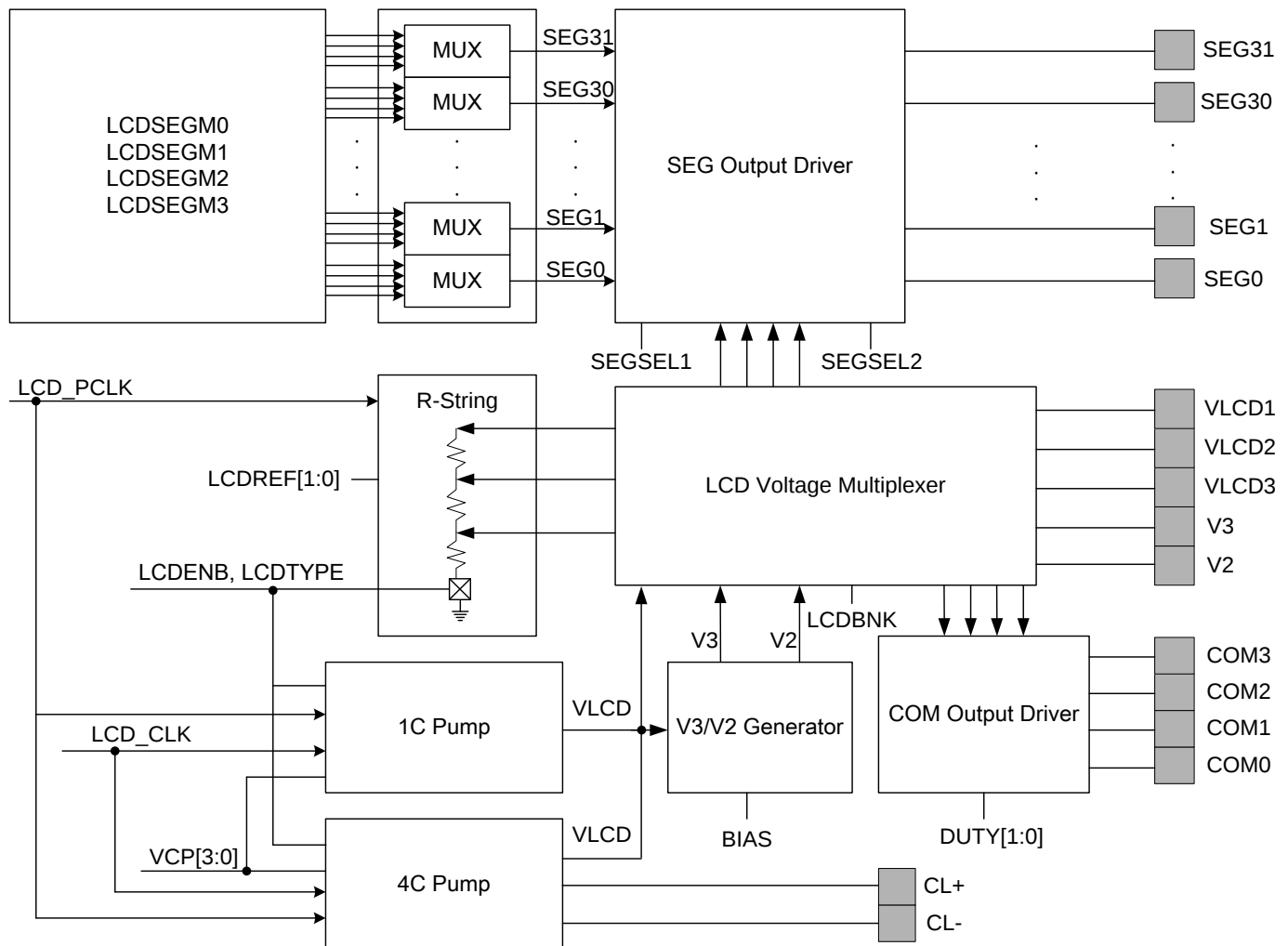
| Pin Name | Type | Description                                    | GPIO Configuration |
|----------|------|------------------------------------------------|--------------------|
| SEGx     | O    | LCD driver segment pins                        |                    |
| COMx     | O    | LCD driver common pins                         |                    |
| CL+      | P    | C-Type LCD charge pump capacitor               |                    |
| CL-      | P    | C-Type LCD charge pump capacitor               |                    |
| VLCD1    | P    | LCD driver power input pin for COM0~3, SEG0~11 |                    |
| VLCD2    | P    | LCD driver power input pin for SEG12~23        |                    |
| VLCD3    | P    | LCD driver power pin for SEG24~31              |                    |
| V3       | P    | 2/3 VLCD bias voltage                          |                    |
| V2       | P    | 1/3 VLCD bias voltage                          |                    |

## 16.4 BLOCK DIAGRAM

### 16.4.1 LCD CLOCK CONTROL



### 16.4.2 LCD BLOCK DIAGRAM

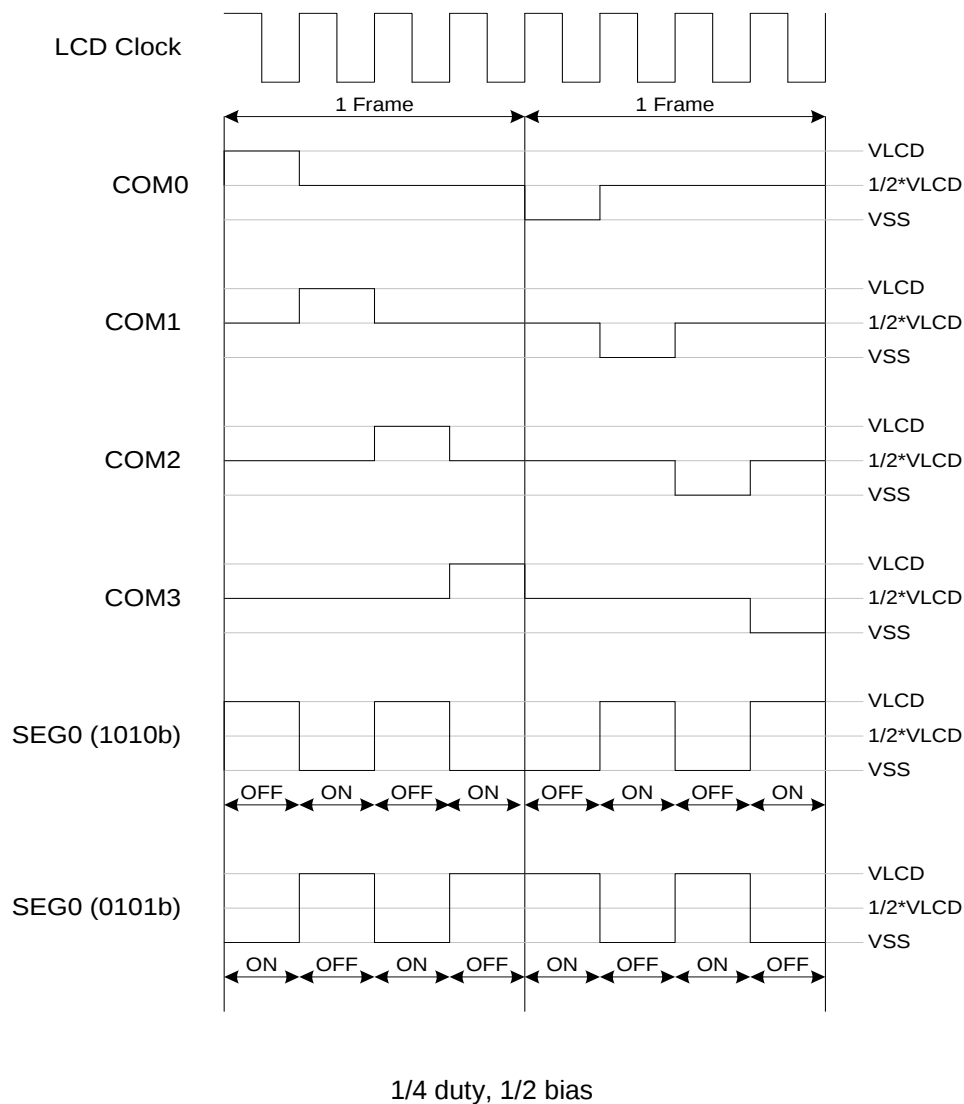


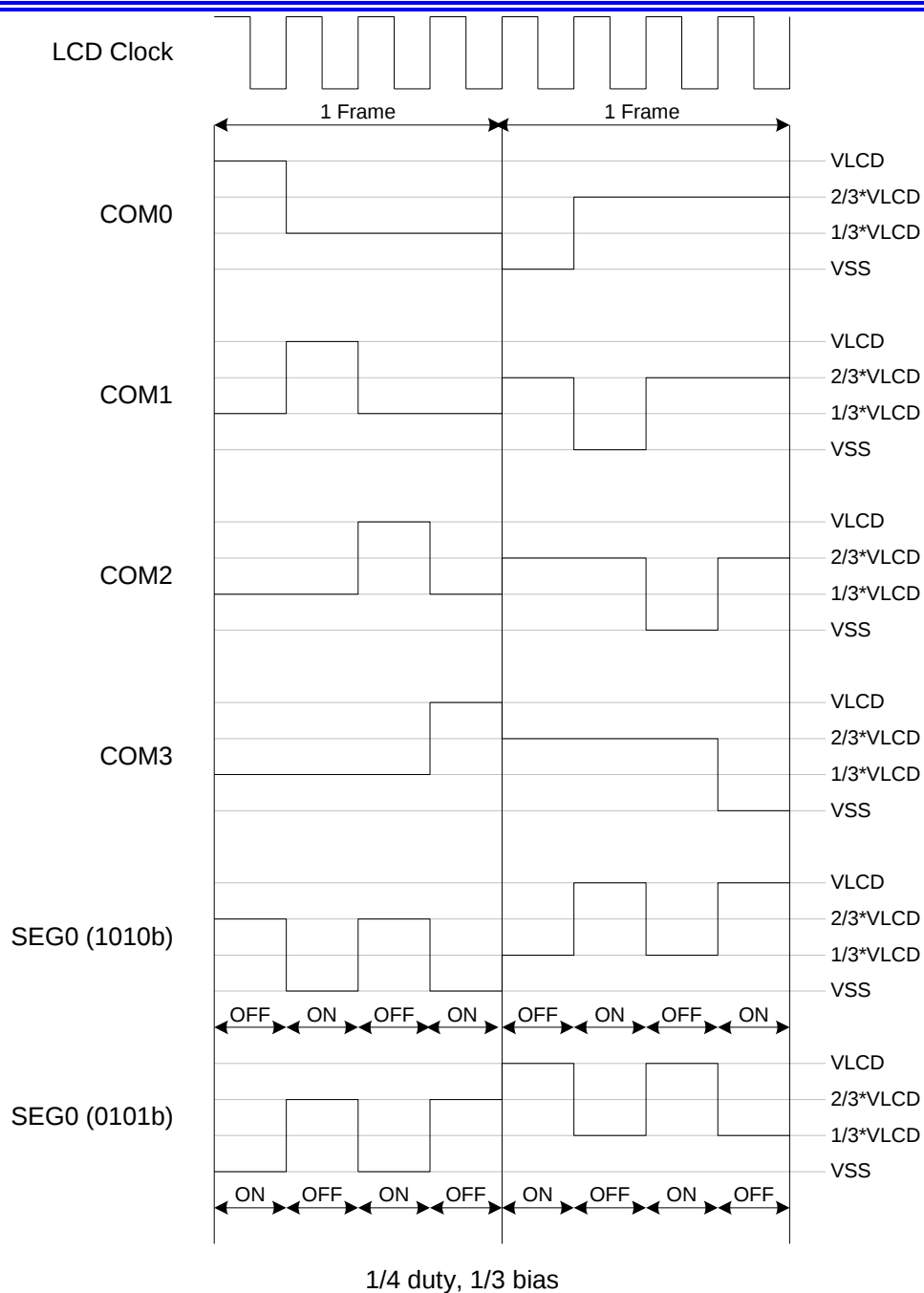
## 16.5 LCD TIMING

### 16.5.1 LCD Timing Table

| LCDCLK | LCD Clock Source | LCDRATE | LCD Clock Rate<br>(LCD_PCLK)          | Duty | Frame Rate<br>= LCD clock rate * Duty |
|--------|------------------|---------|---------------------------------------|------|---------------------------------------|
| 0      | ILRC 32KHz       | 0       | $32\text{KHz} / 64 = 500\text{Hz}$    | 1/4  | $500\text{Hz} / 4 = 125\text{Hz}$     |
|        |                  | 1       | $32\text{KHz} / 128 = 250\text{Hz}$   | 1/2  | $250\text{Hz} / 2 = 125\text{Hz}$     |
|        |                  | 1       | $32\text{KHz} / 128 = 250\text{Hz}$   | 1/4  | $250\text{Hz} / 4 = 62.5\text{Hz}$    |
| 1      | ELS XTAL 32768Hz | 0       | $32768\text{Hz} / 64 = 512\text{Hz}$  | 1/4  | $512\text{Hz} / 4 = 128\text{Hz}$     |
|        |                  | 1       | $32768\text{Hz} / 128 = 256\text{Hz}$ | 1/4  | $256\text{Hz} / 4 = 64\text{Hz}$      |

### 16.5.2 LCD Driver Waveform



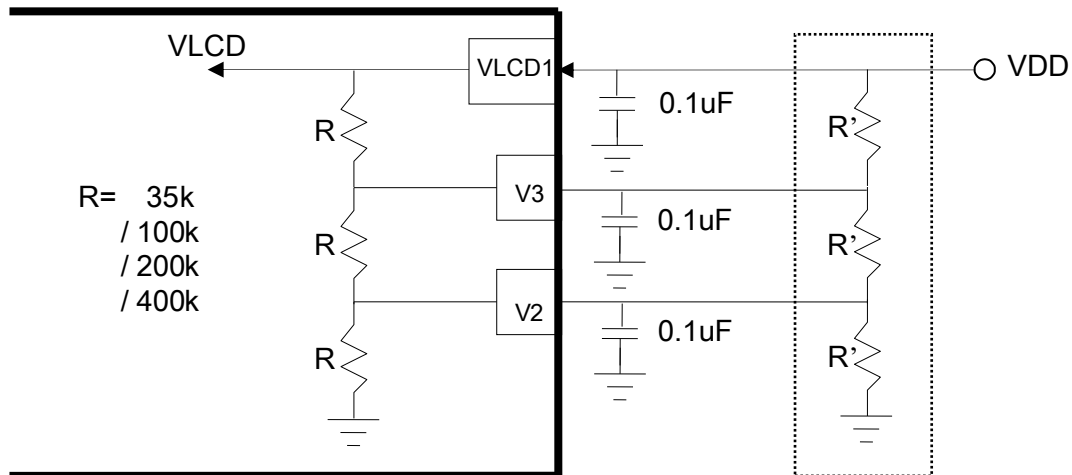


## 16.6 R-TYPE LCD APPLICATION CIRCUIT

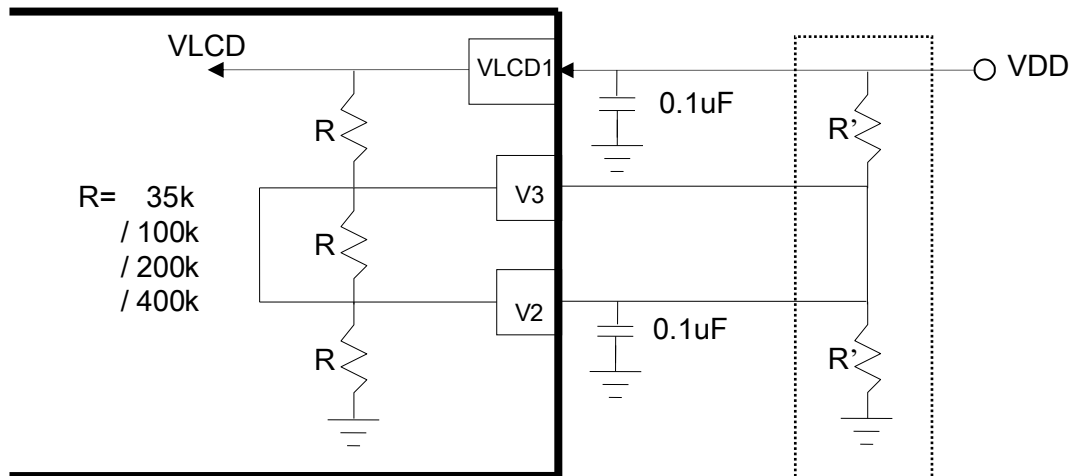
When R-type LCD is enabled (LCDENB=1, LCDTYPE[1:0]=00b in [LCD\\_CTRL](#) register), LCD power source (VLCD) is from external power via VLCD1 pad, and shall be connected to VDD with PCB layout, not internal short to VDD. HW will assign COM0~3 (refer to DUTY[1:0]), SEG0~11, V3, V2 pin as LCD pins instead of GPIO automatically.

V3 and V2 bias voltage is sourced by internal resistor voltage division, and the internal selective 35k, 100k, 200k, 400k resistor are selected by REF[1:0] bits in [LCD\\_CTRL1](#) register. User can connect additional external resistance between VLCD1/V3/V2 for more driving current.

➤ **1/3 Bias ( $V3 = 2/3 \cdot VLCD$ ,  $V2 = 1/3 \cdot VLCD$ )**



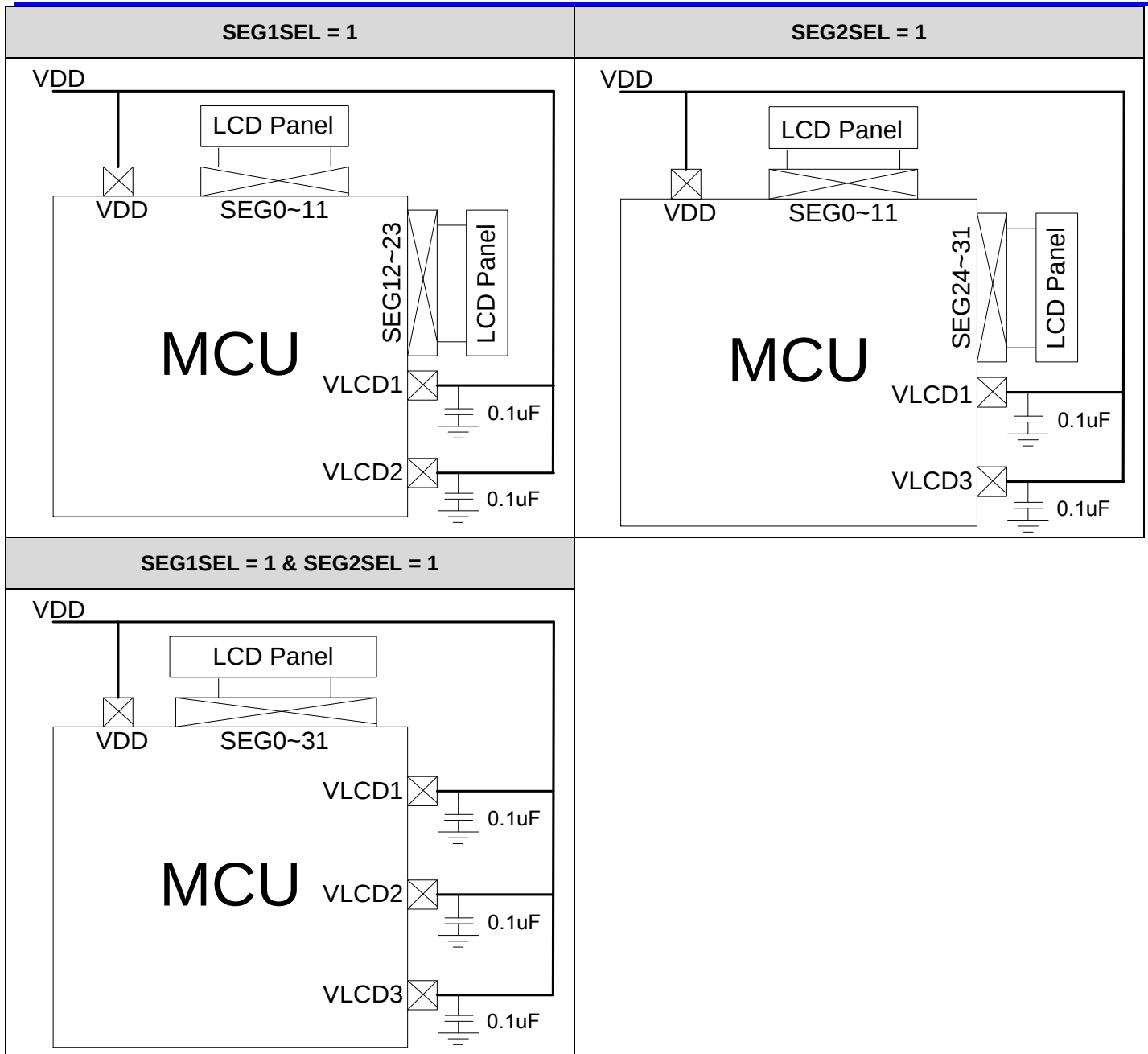
➤ **1/2 Bias ( $V3 = V2 = 1/2 \cdot VLCD$ )**



\* **Note: The 0.1uF capacitors of VLCD1/V3/V2 pins are necessary for power stable, and please put close to VLCD1/V3/V2 pins.**

Segment 12~Segment 23 pins are shared with P0.10~P0.15 and P1.0~P1.5. When these pins are used as LCD pins, the SEG1SEL bit shall be set as "1", and VLCD2 shall also be connected to VDD with PCB layout.

Segment 24~Segment 31 pins are shared with P0.0~P0.7. When these pins are used as LCD pins, the SEG2SEL bit shall be set as "1", and VLCD3 shall also be connected to VDD with PCB layout.



## 16.7 C-TYPE LCD APPLICATION CIRCUIT

When C-type LCD is enabled (LCDENB=1, LCDTYPE[1:0]=01b or 10b) in [LCD\\_CTRL](#) register), The LCD power (VLCD) is supplied by internal LCD charge-pump, and is internal short to VLCD1. HW will assign COM0~3, SEG0~11, V3, V2, CL+, CL- pin as LCD pins instead of GPIO automatically.

The charge-pump voltage VLCD level is controlled by VCP[3:0] bits in [LCD\\_CCTRL1](#) register. In 1/3 bias condition, V2 is the charge pump output voltage which level is 1/3\*VLCD. V3 is 2 times of V2 by charge-pump which level is 2/3\*VLCD; in 1/2 bias condition, V2 is the charge-pump output voltage which level is 1/2\*VLCD, the voltage level of V3 is equal to V2.

Segment 12~Segment 23 pins are shared with P0.10~P0.15 and P1.0~P1.5. When these pins are used as LCD pins, the SEG1SEL bit shall be set as "1", and VLCD2 shall also be connected to VLCD1 with PCB layout.

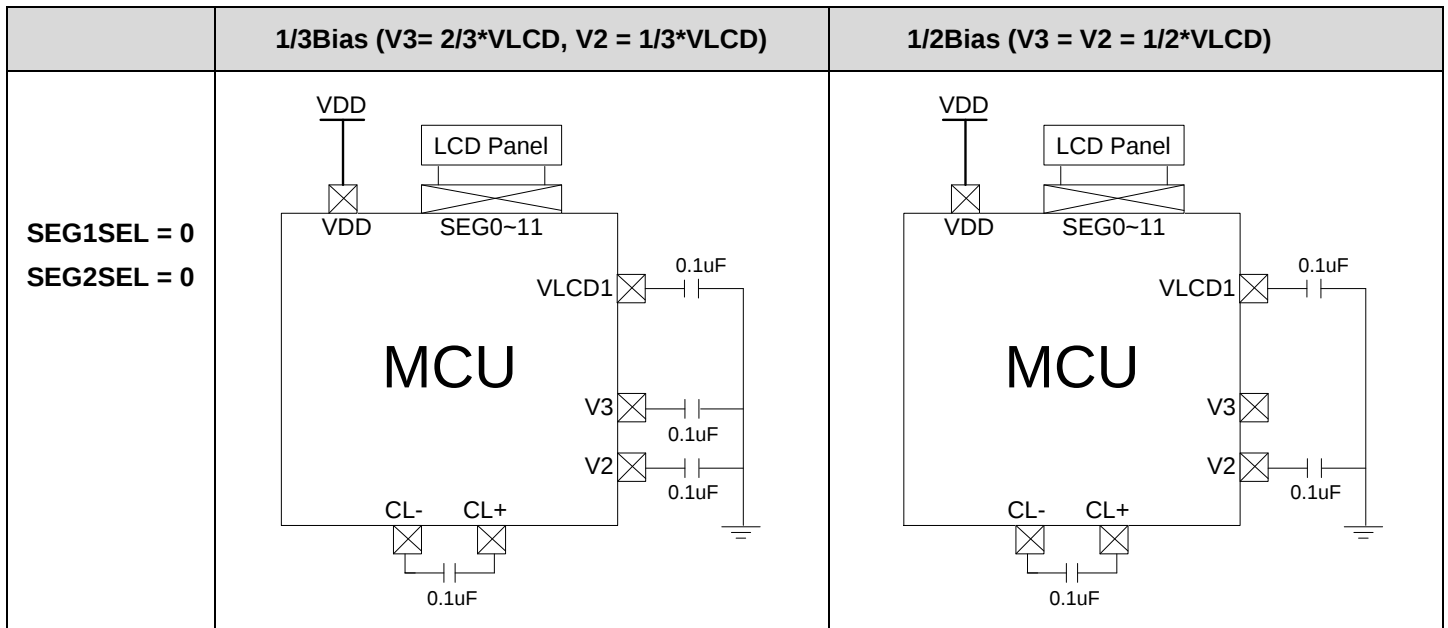
Segment 24~Segment 31 pins are shared with P0.0~P0.7. When these pins are used as LCD pins, the SEG2SEL bit shall be set as "1", and VLCD3 shall also be connected to VLCD1 with PCB layout.

\* **Note:** V2 voltage is charge-pump output voltage.

### 16.7.1 4C-TYPE

\* **Note:**

1. Charge-pump voltage for VLCD is 2.7V~5.0V
2. In 1/2 bias condition, VDD shall be larger than V3.
3. In 1/3 bias condition, VDD shall be larger than V3-0.3V if VLCD > 3.6V
4. Connect a 0.1uF or 0.47uF capacitor between CL+ and CL- pins. Users can adjust the capacitor value depend on the LCD panel size.
5. The 0.1uF capacitors of VLCD1/V3/V2 pins are necessary for power stable. Users can adjust the capacitor value depend on the LCD panel size. Besides, please put close to VLCD1/V3/V2 pins.

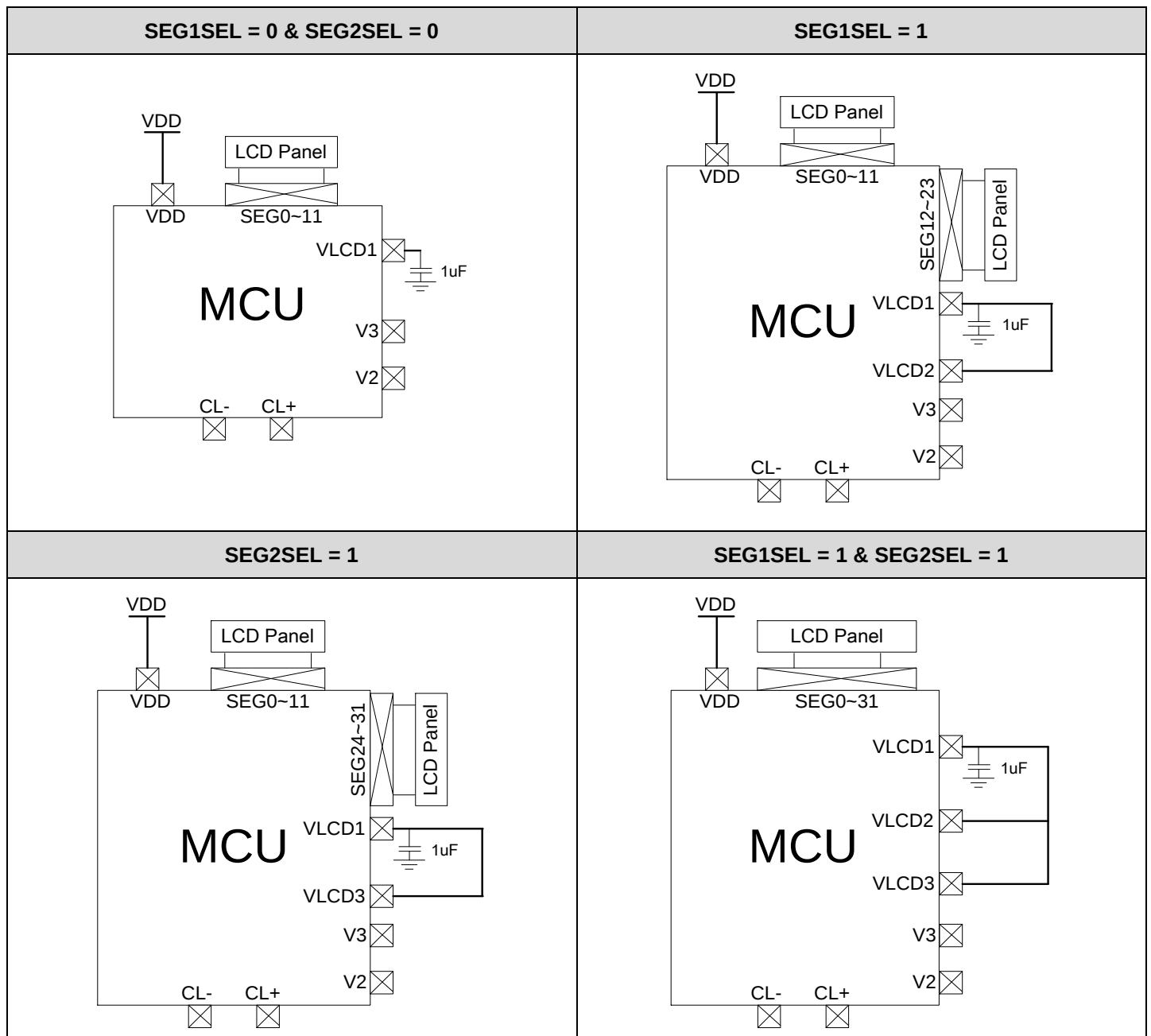


|                                                  |  |  |
|--------------------------------------------------|--|--|
| <p><b>SEG1SEL = 1</b></p>                        |  |  |
| <p><b>SEG2SEL = 1</b></p>                        |  |  |
| <p><b>SEG1SEL = 1</b><br/><b>SEG2SEL = 1</b></p> |  |  |

## 16.7.2 1C-Type

**\* Note:**

1. Maximal charge-pump voltage is 3.4V
2. NOT necessary to connect capacitors between CL+ and CL- pins.
3. NOT necessary to connect capacitors for V3/V2 pins.
4. The 1uF capacitors of VLCD1 pin is necessary for power stable. Users can adjust the capacitor value depend on the LCD panel size. Besides, please put close to VLCD1 pin.



## 16.8 LCD DISPLAY MEMORY MAP

| Bit | LCD_SEGM3 | LCD_SEGM2 | LCD_SEGM1 | LCD_SEGM0 |      |
|-----|-----------|-----------|-----------|-----------|------|
| 31  | SEG31     | SEG23     | SEG15     | SEG7      | COM3 |
| 30  |           |           |           |           | COM2 |
| 29  |           |           |           |           | COM1 |
| 28  |           |           |           |           | COM0 |
| 27  | SEG30     | SEG22     | SEG14     | SEG6      | COM3 |
| 26  |           |           |           |           | COM2 |
| 25  |           |           |           |           | COM1 |
| 24  |           |           |           |           | COM0 |
| 23  | SEG29     | SEG21     | SEG13     | SEG5      | COM3 |
| 22  |           |           |           |           | COM2 |
| 21  |           |           |           |           | COM1 |
| 20  |           |           |           |           | COM0 |
| 19  | SEG28     | SEG20     | SEG12     | SEG4      | COM3 |
| 18  |           |           |           |           | COM2 |
| 17  |           |           |           |           | COM1 |
| 16  |           |           |           |           | COM0 |
| 15  | SEG27     | SEG19     | SEG11     | SEG3      | COM3 |
| 14  |           |           |           |           | COM2 |
| 13  |           |           |           |           | COM1 |
| 12  |           |           |           |           | COM0 |
| 11  | SEG26     | SEG18     | SEG10     | SEG2      | COM3 |
| 10  |           |           |           |           | COM2 |
| 9   |           |           |           |           | COM1 |
| 8   |           |           |           |           | COM0 |
| 7   | SEG25     | SEG17     | SEG9      | SEG1      | COM3 |
| 6   |           |           |           |           | COM2 |
| 5   |           |           |           |           | COM1 |
| 4   |           |           |           |           | COM0 |
| 3   | SEG24     | SEG16     | SEG8      | SEG0      | COM3 |
| 2   |           |           |           |           | COM2 |
| 1   |           |           |           |           | COM1 |
| 0   |           |           |           |           | COM0 |

## 16.9 LCD REGISTERS

Base Address: 0x4003 4000

### 16.9.1 LCD Control register (LCD\_CTRL)

Address Offset: 0x00

Reset value: 0x1000 0302

**\* Note:**

1. Segment 24~Segment 31 pins are shared with P0.0~P0.7.
2. When these pins are used as general purpose I/O mode, the SEG2SEL bit shall be set as "0", and VDD3 shall be connected to VDD with PCB layout.
3. When these pins are used as LCD pins, the SEG2SEL bit shall be set as "1", and please refer to [R-type LCD application circuit](#) or [C-type LCD application circuit](#).
4. Segment 12~Segment 23 pins are shared with P0.10~P0.15 and P1.0~P1.5.
5. When these pins are used as general purpose I/O mode, the SEG1SEL bit shall be set as "0", and VDD2 shall be connected to VDD with PCB layout.
6. When these pins are used as LCD pins, the SEG1SEL bit shall be set as "1", and please refer to [R-type LCD application circuit](#) or [C-type LCD application circuit](#).

| Bit   | Name         | Description                                                                                                                                                                                                                                                                                                                                                     | Attribute | Reset |
|-------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:30 | Reserved     |                                                                                                                                                                                                                                                                                                                                                                 | R/W       | 0     |
| 29:28 | DRIVEP[1:0]  | LCD panel driving ability<br>00: Strong (Larger panel)<br>01: Medium (Medium panel)<br>10: Reserved<br>11: Low (Smaller panel)                                                                                                                                                                                                                                  | R/W       | 01b   |
| 27:12 | Reserved     |                                                                                                                                                                                                                                                                                                                                                                 | R/W       | 0     |
| 11    | LCDRATE      | LCD clock rate (LCD_PCLK)<br>0: LCD clock source / 64<br>1: LCD clock source / 128                                                                                                                                                                                                                                                                              | R/W       | 0     |
| 10    | LCDCLK       | LCD clock source selection<br>0: ILRC<br>1: ELS XTAL                                                                                                                                                                                                                                                                                                            | R/W       | 0     |
| 9:8   | DUTY[1:0]    | Duty selection<br>00: Reserved<br>01: 1/2 duty. HW will assign COM0~1 as LCD pins instead of GPIO. P1.13, P1.12 is still available to be used as GPIO in R-type.<br>10: 1/3 duty. HW will assign COM0~2 as LCD pins instead of GPIO. P1.13 is still available to be used as GPIO in R-type.<br>11: 1/4 duty. HW will assign COM0~3 as LCD pins instead of GPIO. | R/W       | 11b   |
| 7     | Reserved     |                                                                                                                                                                                                                                                                                                                                                                 | R/W       | 0     |
| 6     | SEGSEL2      | SEG24~31 enable bit<br>0: Disable. SEG24~31 pins are GPIO.<br>1: Enable. HW will assign SEG24~31 pins as LCD pins instead of GPIO.                                                                                                                                                                                                                              | R/W       | 0     |
| 5     | SEGSEL1      | SEG12~23 enable bit<br>0: Disable. SEG12~23 pins are GPIO.<br>1: Enable. HW will assign SEG12~23 pins as LCD pins instead of GPIO.                                                                                                                                                                                                                              | R/W       | 0     |
| 4     | BIAS         | LCD Bias selection<br>0: 1/3 Bias<br>1: 1/2 Bias                                                                                                                                                                                                                                                                                                                | R/W       | 0     |
| 3:2   | LCDTYPE[1:0] | LCD type control bit<br>00: R-Type                                                                                                                                                                                                                                                                                                                              | R/W       | 00b   |

|          |        |                                                                                                                                                                  |     |   |
|----------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---|
|          |        | 01: 4C Type. HW will assign CL+, CL- pins as LCD pins instead of GPIO.<br>10: 1C Type. HW will assign CL+, CL- pins as LCD pins instead of GPIO.<br>11: Reserved |     |   |
| <b>1</b> | ITB    | Used for internal testing and the only value "1" is allowed.                                                                                                     | R/W | 1 |
| <b>0</b> | LCDENB | LCD driver enable bit.<br>0: Disable<br>1: Enable. HW will assign SEG0~11, V3, V2 pin as LCD pins instead of GPIO.                                               | R/W | 0 |

### 16.9.2 LCD Control register 1(LCD\_CTRL1)

Address Offset: 0x04

Reset value: 0x1000 0000

| Bit          | Name     | Description                                                                                        | Attribute | Reset |
|--------------|----------|----------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:29</b> | Reserved |                                                                                                    | R/W       | 0     |
| <b>28</b>    | ITB      | Used for internal testing and the only value "0" is allowed.                                       | R/W       | 1     |
| <b>27:3</b>  | Reserved |                                                                                                    | R/W       | 0     |
| <b>2:1</b>   | REF[1:0] | Resistance selection for LCD Bias Voltage-division.<br>00: 400K<br>01: 200K<br>10: 100K<br>11: 35K | R/W       | 00b   |
| <b>0</b>     | LCDBNK   | LCD blank control bit<br>0: Normal display<br>1: All LCD dots off.                                 | R/W       | 0     |

### 16.9.3 LCD C-Type Control register 1 (LCD\_CCTRL1)

Address Offset: 0x08

Reset value: 0x6002 0003

LCD\_CCTRL1 is available for C-Type LCD, and the charge pump clock source is controlled by LCDCLK bit in [LCD\\_CTRL](#) register.

| LCDCLK | Charge-pump Clock Source |
|--------|--------------------------|
| 0      | ILRC 32KHz               |
| 1      | ELS XTAL 32.768KHz       |

| Bit          | Name     | Description                                                      | Attribute | Reset   |
|--------------|----------|------------------------------------------------------------------|-----------|---------|
| <b>31:30</b> | Reserved | The only value "01b" is allowed.                                 | R/W       | 01b     |
| <b>29:28</b> | IT1[1:0] | Used for internal testing and the only value "00b" is allowed.   | R/W       | 10b     |
| <b>27:24</b> | IT2[3:0] | Used for internal testing and the only value "0100b" is allowed. | R/W       | 00b     |
| <b>23:4</b>  | Reserved |                                                                  | R/W       | 0x02000 |
| <b>3:0</b>   | VCP[3:0] | C-type VLCD output voltage                                       | R/W       | 0011b   |

| 1C Type  |       |          |       |          |
|----------|-------|----------|-------|----------|
| VCP[3:0] | VLCD  | 1/3 Bias |       | 1/2 Bias |
|          |       | V2       | V3    | V2 = V3  |
| 0000     | 2.70V | 0.90V    | 1.80V | 1.35V    |
| 0001     | 2.80V | 0.94V    | 1.87V | 1.40V    |
| 0010     | 2.90V | 0.98V    | 1.96V | 1.45V    |
| 0011     | 3.00V | 1.00V    | 2.00V | 1.50V    |
| 0100     | 3.10V | 1.04V    | 2.08V | 1.53V    |
| 0101     | 3.20V | 1.08V    | 2.14V | 1.57V    |
| 0110     | 3.30V | 1.10V    | 2.20V | 1.61V    |
| 0111     | 3.40V | 1.14V    | 2.28V | 1.66V    |
| Reserved | N/A   | N/A      | N/A   | N/A      |

| 4C Type  |       |          |       |          |
|----------|-------|----------|-------|----------|
| VCP[3:0] | VLCD  | 1/3 Bias |       | 1/2 Bias |
|          |       | V2       | V3    | V2 = V3  |
| 0000     | 2.70V | 0.90V    | 1.80V | 1.35V    |
| 0001     | 2.80V | 0.93V    | 1.86V | 1.40V    |
| 0010     | 2.90V | 0.96V    | 1.93V | 1.45V    |
| 0011     | 3.00V | 1.00V    | 2.00V | 1.50V    |
| 0100     | 3.06V | 1.02V    | 2.04V | 1.53V    |
| 0101     | 3.14V | 1.05V    | 2.10V | 1.57V    |
| 0110     | 3.20V | 1.07V    | 2.14V | 1.61V    |
| 0111     | 3.30V | 1.10V    | 2.20V | 1.66V    |
| 1000     | 3.40V | 1.13V    | 2.26V | 1.70V    |
| 1001     | 3.60V | 1.20V    | 2.40V | 1.80V    |
| 1010     | 3.80V | 1.27V    | 2.54V | 1.90V    |
| 1011     | 4.00V | 1.33V    | 2.67V | 2.00V    |
| 1100     | 4.20V | 1.40V    | 2.80V | 2.12V    |
| 1101     | 4.40V | 1.49V    | 2.98V | 2.23V    |
| 1110     | 4.70V | 1.57V    | 3.14V | 2.35V    |
| 1111     | 5.00V | 1.66V    | 3.32V | 2.50V    |

## 16.9.4 LCD C-Type Control register 2 (LCD\_CCTRL2)

Address Offset: 0x0C

LCD\_CCTRL2 register is for internal testing, and the only value "0x00000004" is allowed.

## 16.9.5 LCD Frame Counter Control register (LCD\_FCC)

Address offset: 0x10

Reset value: 0x0000 0002

The frame counter (FC) will start to count up from 0x0 when FCENB = 1, and add 1 when a frame is updated. When the counter value reaches FCT[5:0], FC will reset as 0x0 by HW, the LCD frame interrupt flag will become 1. If LCD frame interrupt is enabled (FCIE =1), the LCD frame interrupt is generated and sent to the interrupt controller.

| Bit   | Name     | Description | Attribute | Reset |
|-------|----------|-------------|-----------|-------|
| 31:10 | Reserved |             | R         | 0     |

|            |                 |                                                           |     |         |
|------------|-----------------|-----------------------------------------------------------|-----|---------|
| <b>7</b>   | <b>FCIE</b>     | LCD frame interrupt enable bit<br>0: Disable<br>1: Enable | R/W | 0       |
| <b>6:1</b> | <b>FCT[5:0]</b> | LCD frame counter threshold value                         | R/W | 000001b |
| <b>0</b>   | <b>FCENB</b>    | LCD frame counter enable bit<br>0: Disable<br>1: Enable   | R/W | 0       |

### 16.9.6 LCD Raw Interrupt Status register (LCD\_RIS)

Address offset: 0x14

Reset value: 0x0000 0000

| Bit         | Name        | Description                                                                                                                                                    | Attribute | Reset |
|-------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| <b>31:1</b> | Reserved    |                                                                                                                                                                | R         | 0     |
| <b>0</b>    | <b>FCIF</b> | LCD frame interrupt flag.<br>0: Read→No interrupt<br>Write→Write "0" to clear this bit and reset the interrupt if FCIE=1.<br>1: FC interrupt requirements met. | R/W       | 0     |

### 16.9.7 LCD SEG Memory register 0 (LCD\_SEGM0)

Address Offset: 0x20

Reset value: 0x0000 0000

| Bit          | Name             | Description             | Attribute | Reset |
|--------------|------------------|-------------------------|-----------|-------|
| <b>31:28</b> | <b>SEG7[3:0]</b> | SEG7 data for COM0~COM3 | R/W       | 0     |
| <b>27:24</b> | <b>SEG6[3:0]</b> | SEG6 data for COM0~COM3 | R/W       | 0     |
| <b>23:20</b> | <b>SEG5[3:0]</b> | SEG5 data for COM0~COM3 | R/W       | 0     |
| <b>19:16</b> | <b>SEG4[3:0]</b> | SEG4 data for COM0~COM3 | R/W       | 0     |
| <b>15:12</b> | <b>SEG3[3:0]</b> | SEG3 data for COM0~COM3 | R/W       | 0     |
| <b>11:8</b>  | <b>SEG2[3:0]</b> | SEG2 data for COM0~COM3 | R/W       | 0     |
| <b>7:4</b>   | <b>SEG1[3:0]</b> | SEG1 data for COM0~COM3 | R/W       | 0     |
| <b>3:0</b>   | <b>SEG0[3:0]</b> | SEG0 data for COM0~COM3 | R/W       | 0     |

### 16.9.8 LCD SEG Memory register 1 (LCD\_SEGM1)

Address Offset: 0x24

Reset value: 0x0000 0000

| Bit          | Name              | Description              | Attribute | Reset |
|--------------|-------------------|--------------------------|-----------|-------|
| <b>31:28</b> | <b>SEG15[3:0]</b> | SEG15 data for COM0~COM3 | R/W       | 0     |
| <b>27:24</b> | <b>SEG14[3:0]</b> | SEG14 data for COM0~COM3 | R/W       | 0     |

|              |            |                          |     |   |
|--------------|------------|--------------------------|-----|---|
| <b>23:20</b> | SEG13[3:0] | SEG13 data for COM0~COM3 | R/W | 0 |
| <b>19:16</b> | SEG12[3:0] | SEG12 data for COM0~COM3 | R/W | 0 |
| <b>15:12</b> | SEG11[3:0] | SEG11 data for COM0~COM3 | R/W | 0 |
| <b>11:8</b>  | SEG10[3:0] | SEG10 data for COM0~COM3 | R/W | 0 |
| <b>7:4</b>   | SEG9[3:0]  | SEG9 data for COM0~COM3  | R/W | 0 |
| <b>3:0</b>   | SEG8[3:0]  | SEG8 data for COM0~COM3  | R/W | 0 |

### 16.9.9 LCD SEG Memory register 2 (LCD\_SEG2)

Address Offset: 0x28

Reset value: 0x0000 0000

| Bit          | Name       | Description              | Attribute | Reset |
|--------------|------------|--------------------------|-----------|-------|
| <b>31:28</b> | SEG23[3:0] | SEG23 data for COM0~COM3 | R/W       | 0     |
| <b>27:24</b> | SEG22[3:0] | SEG22 data for COM0~COM3 | R/W       | 0     |
| <b>23:20</b> | SEG21[3:0] | SEG21 data for COM0~COM3 | R/W       | 0     |
| <b>19:16</b> | SEG20[3:0] | SEG20 data for COM0~COM3 | R/W       | 0     |
| <b>15:12</b> | SEG19[3:0] | SEG19 data for COM0~COM3 | R/W       | 0     |
| <b>11:8</b>  | SEG18[3:0] | SEG18 data for COM0~COM3 | R/W       | 0     |
| <b>7:4</b>   | SEG17[3:0] | SEG17 data for COM0~COM3 | R/W       | 0     |
| <b>3:0</b>   | SEG16[3:0] | SEG16 data for COM0~COM3 | R/W       | 0     |

### 16.9.10 LCD SEG Memory register 3 (LCD\_SEG3)

Address Offset: 0x2C

Reset value: 0x0000 0000

| Bit          | Name       | Description              | Attribute | Reset |
|--------------|------------|--------------------------|-----------|-------|
| <b>31:28</b> | SEG31[3:0] | SEG31 data for COM0~COM3 | R/W       | 0     |
| <b>27:24</b> | SEG30[3:0] | SEG30 data for COM0~COM3 | R/W       | 0     |
| <b>23:20</b> | SEG29[3:0] | SEG29 data for COM0~COM3 | R/W       | 0     |
| <b>19:16</b> | SEG28[3:0] | SEG28 data for COM0~COM3 | R/W       | 0     |
| <b>15:12</b> | SEG27[3:0] | SEG27 data for COM0~COM3 | R/W       | 0     |
| <b>11:8</b>  | SEG26[3:0] | SEG26 data for COM0~COM3 | R/W       | 0     |
| <b>7:4</b>   | SEG25[3:0] | SEG25 data for COM0~COM3 | R/W       | 0     |
| <b>3:0</b>   | SEG24[3:0] | SEG24 data for COM0~COM3 | R/W       | 0     |

# 17 FLASH

## 17.1 OVERVIEW

SONiX 32-bit MCU integrated device feature in-system programmable (ISP) FLASH memory for convenient, upgradeable code storage. The FLASH memory may be programmed via the SONiX 32-bit MCU programming interface or by application code for maximum flexibility. SONiX 32-bit MCU provides security options at the disposal of the designer to prevent unauthorized access to information stored in FLASH memory.

- The MCU is stalled during Flash program and erase operations, although peripherals (Timers, WDT, I/O, PWM, etc.) remain active.
- Watchdog timer should be cleared if enabled before the Flash write or erase operation.
- The erase operation sets all the bits in the Flash page to logic 1.
- HW will hold system clock and automatically move out data from RAM and do programming, after programming finished, HW will release system clock and let MCU execute the next instruction.

**\* Note: HCLK MUST be less or equal to 24MHz during Flash program and erase operations.**

## 17.2 EMBEDDED FLASH MEMORY

The Flash memory is organized as 32-bit wide memory cells that can be used for storing both code and data constants, and is located at a specific base address in the memory map of chip.

The high-performance Flash memory module in chip has the following key features:

- Memory organization: the Flash memory is organized as a User ROM, Boot ROM.

|          |                                                         |
|----------|---------------------------------------------------------|
| User ROM | Up to 16K × 32 bits divided into 64 pages of 1024 Bytes |
| Boot ROM | Up to 1K × 32 bits divided into 4 pages of 1024 Bytes   |

The Flash interface implements instruction access and data access based on the AHB protocol. It implements the logic necessary to carry out Flash memory operations (Program/Erase). Program/Erase operations can be performed over the whole product voltage range.

## 17.3 FEATURES

- Read interface (32-bit)
- Flash Program / Erase operation
- Code Option includes Code Security (CS)

Write operations to the main memory block and the code options are managed by an embedded Flash Memory Controller (FMC). The high voltage needed for Program/Erase operations is internally generated. The main Flash memory can be read/write protected against different levels of Code Security (CS).

During a write operation to the Flash memory, any attempt to read the Flash memory will stall the bus. The read operation will proceed correctly once the write operation has completed. This means that code or data fetches cannot be made while a write/erase operation is ongoing.

For write and erase operations on the Flash memory, the IHRC will be turn ON by FMC. The Flash memory can be

programmed and erased using ICP and ISP.

## 17.4 ORGANIZATION

| Block       | Name    | Base Address            | Size (Byte) |
|-------------|---------|-------------------------|-------------|
| User ROM    | Page 0  | 0x00000000 ~ 0x000003FF | 1024        |
|             | Page 1  | 0x00000400 ~ 0x000007FF | 1024        |
|             | .       | .                       |             |
|             | Page 63 | 0x0000FC00 ~ 0x0000FFFF | 1024        |
| Boot Loader | Page 0  | 0x1FFF0000 ~ 0x1FFF03FF | 1024        |
|             | Page 1  | 0x1FFF0400 ~ 0x1FFF07FF | 1024        |
|             | Page 2  | 0x1FFF0800 ~ 0x1FFF0BFF |             |
|             | Page 3  | 0x1FFF0C00 ~ 0x1FFF0FFF | 1024        |

## 17.5 READ

The embedded Flash module can be addressed directly, as a common memory space. Any data read operation accesses the content of the Flash module through dedicated read senses and provides the requested data.

The read interface consists of a read controller on one side to access the Flash memory, and an AHB interface on the other side to interface with the CPU. The main task of the read interface is to generate the control signals to read from the Flash memory as required by the CPU.

## 17.6 PROGRAM/ERASE

The Flash memory erase operation can be performed at page level.

To ensure that there is no over-programming, the Flash programming and erase controller blocks are clocked by IHRC.

## 17.7 EMBEDDED BOOT LOADER

The embedded boot loader is used to reprogram the Flash memory using the USART0 serial interface. This program is located in the Boot ROM and is programmed by SONiX during production.

## 17.8 FLASH MEMORY CONTROLLER (FMC)

The FMC handles the program and erase operations of the Flash memory.

### 17.8.1 CODE SECURITY (CS)

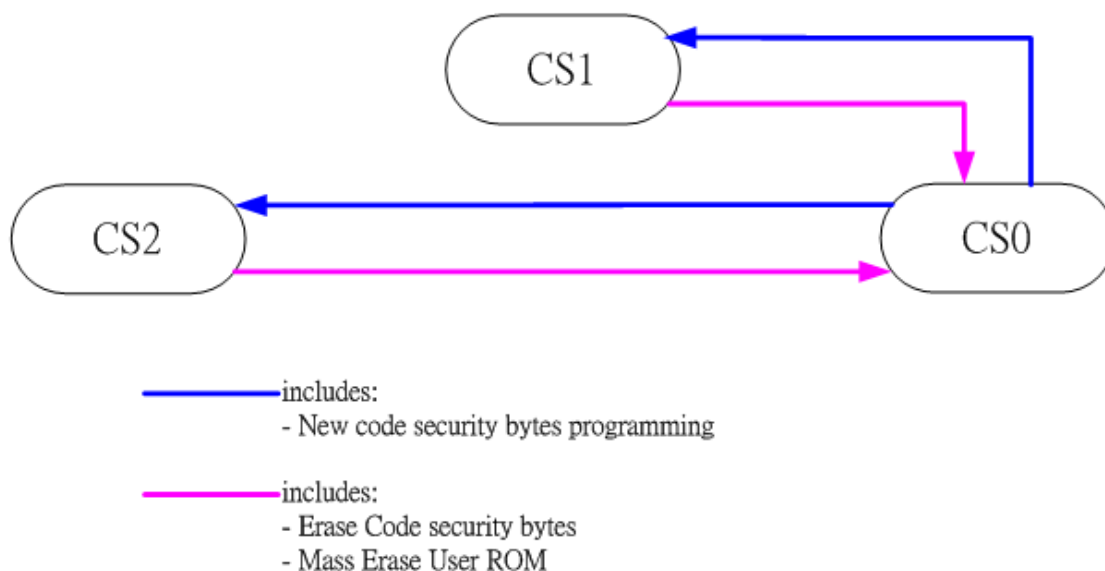
Code Security is a mechanism that allows the user to enable different levels of security in the system so that access to the on-chip Flash and use of the ISP can be restricted.

\* **Note:** Any Code Security change becomes effective only after the MCU has been Reboot.

| User ROM                 |         | CS0 | CS1  | CS2  | CS3  | Description                                 |
|--------------------------|---------|-----|------|------|------|---------------------------------------------|
| WRITER                   | Read    | O   | X    | X    | X    |                                             |
|                          | Erase   | O   | O(*) | O(*) | O(*) | (*) WRITER will change the CS level to CS0. |
|                          | Program | O   | O    | O    | O    |                                             |
| FW<br>(EEPROM emulation) | Read    | O   | O    | O    | O    |                                             |
|                          | Erase   | O   | O    | O    | X    |                                             |
|                          | Program | O   | O    | O    | X    |                                             |
| SWD                      | Read    | O   | X    | X    | X    |                                             |
|                          | Erase   | O   | X    | X    | X    |                                             |
|                          | Program | O   | X    | X    | X    |                                             |

\* **Note:** User may try to change security level from CS3 to CS0, from CS2 to CS0, or from CS1 to CS0. HW shall:

1. Mass erase the User ROM first. User shall NOT execute this operation in debug mode, since the SWD communication may fail during the mass erase procedure.
2. Update security level.



### 17.8.2 PROGRAM FLASH MEMORY

The Flash memory can be programmed 32 bits at a time. CPU can program the main Flash memory by performing

standard word write operations. The PG bit in the FLASH\_CTRL register must be set. FMC preliminarily reads the value at the addressed main Flash memory location and checks that it has been erased. If not, the program operation is skipped and a warning is issued by the PGERR bit in FLASH\_STATUS register. The end of the program operation is indicated by the EOP bit in the FLASH\_STATUS register.

The main Flash memory programming sequence in standard mode is as follows:

1. Set the PG bit in the FLASH\_CTRL register.
2. Perform the data write at the desired address.
3. Wait for the BUSY bit to be reset.
4. (Optional) Read the programmed value and verify.

### 17.8.3 ERASE

The Flash memory can be erased page by page or completely (Mass Erase).

#### 17.8.3.1 PAGE ERASE

A page of the Flash memory can be erased using the Page Erase feature of the FMC. To erase a page, the procedure below should be followed:

1. Set the PER bit in the FLASH\_CTRL register
2. Program the FLASH\_ADDR register to select a page to be erased
3. Set the STARTE bit in the FLASH\_CTRL register
4. Wait for the BUSY bit to be reset
5. (Optional) Read the erased page and verify

#### 17.8.3.2 MASS ERASE

When the Flash memory read protection is changed from protected to unprotected, a Mass Erase of the User ROM is performed by HW before reprogramming the read protection option.

## 17.9 READ PROTECTION

The read protection is activated by setting the Code Security bytes in Code option.

When the Flash memory read protection is changed from protected to unprotected, a Mass Erase of the User ROM is performed by HW before reprogramming the read protection option.

## 17.10 HW CHECKSUM

HW checksum is the checksum of User ROM. If the read protection is enabled, the users can still readout the HW checksum through Writer or ISP AP.

## 17.11 FMC REGISTERS

Base Address: 0x4006 2000

### 17.11.1 Flash Low Power Control register (FLASH\_LPCTRL)

Address offset: 0x00

| Bit   | Name        | Description                                                                                                                                           | Attribute | Reset |
|-------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:16 | FMCKEY      | FMC verify key.<br>Read as 0. When writing to the register you must write 0x5AFA to FMCKEY, otherwise behavior of writing to the register is ignored. | W         | 0     |
| 15:2  | Reserved    |                                                                                                                                                       | R         | 0     |
| 1:0   | LPMODE[1:0] | Flash Low Power mode enable bit<br>00b: Disable<br>01b: Reserved<br>10b: Slow mode power saving (HCLK=ILRC=32KHz)<br>11b: Reserved                    | R/W       | 0     |

### 17.11.2 Flash Status register (FLASH\_STATUS)

Address offset: 0x04

Reset value: 0x0000 0000

| Bit  | Name     | Description                                                                                                                                                                                                                               | Attribute | Reset |
|------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:3 | Reserved |                                                                                                                                                                                                                                           | R         | 0     |
| 2    | PGERR    | Programming error flag<br>0: Read→No error.<br>Write→Clear this flag.<br>1: Set by HW when<br>* The address to be programmed contains a value different from 0xFFFFFFFF before programming.<br>* The address to be programmed is illegal. | R/W       | 0     |
| 1    | Reserved |                                                                                                                                                                                                                                           | R         | 0     |
| 0    | BUSY     | Busy flag<br>0: Flash operation is not busy.<br>1: Flash operation is in progress. This is set on the beginning of a Flash operation and reset when the operation finishes or when an error occurs by HW.                                 | R         | 0     |

### 17.11.3 Flash Control register (FLASH\_CTRL)

Address offset: 0x08

**\* Note: HCLK MUST be equal to 12MHz during Flash program and erase operations.**

| Bit  | Name     | Description                                                                                   | Attribute | Reset |
|------|----------|-----------------------------------------------------------------------------------------------|-----------|-------|
| 31:7 | Reserved |                                                                                               | R         | 0     |
| 7    | CHK      | Checksum calculation chosen<br>This bit is set only by SW and reset when the BUSY bit resets. | R/W       | 0     |
| 6    | STARTE   | Start Erase operation                                                                         | R/W       | 0     |

|     |          |                                                                                                                                                            |     |   |
|-----|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---|
|     |          | 1: Triggers an ERASE operation when set. This bit is set only by SW and resets when the BUSY bit resets.<br>PER bit shall also be 1 when setting this bit. |     |   |
| 5:2 | Reserved |                                                                                                                                                            | R   | 0 |
| 1   | PER      | Page Erase chosen.<br>This bit is set only by SW and reset when the BUSY bit resets.                                                                       | R/W | 0 |
| 0   | PG       | Flash Programming chosen.<br>This bit is set only by SW and reset when the BUSY bit resets.                                                                | R/W | 0 |

#### 17.11.4 Flash Data register (FLASH\_DATA)

Address offset: 0x0C

For Page Program operations, this should be updated by SW to indicate the data to be programmed.

| Bit  | Name       | Description            | Attribute | Reset |
|------|------------|------------------------|-----------|-------|
| 31:0 | DATA[31:0] | Data to be programmed. | R/W       | 0     |

#### 17.11.5 Flash Address register (FLASH\_ADDR)

Address offset: 0x10

The Flash address to be erased or programmed should be updated by SW, and the PG bit or PER bit shall be set before filling in the Flash address.

**\* Note: Write access to this register is blocked when the BUSY bit in the FLASH\_STATUS register is set.**

| Bit  | Name      | Description                                                                                                                  | Attribute | Reset |
|------|-----------|------------------------------------------------------------------------------------------------------------------------------|-----------|-------|
| 31:0 | FAR[31:0] | Flash Address<br>Choose the Flash address to erase when Page Erase is selected, or to program when Page Program is selected. | R/W       | 0     |

#### 17.11.6 Flash Checksum register (FLASH\_CHKSUM)

Address offset: 0x14

| Bit   | Name         | Description           | Attribute | Reset |
|-------|--------------|-----------------------|-----------|-------|
| 31:16 | Reserved     |                       | R         | 0     |
| 15:0  | CHKSUM[15:0] | Checksum of User ROM. | R         | 0     |

# 18 SERIAL-WIRE DEBUG (SWD)

## 18.1 OVERVIEW

SWD functions are integrated into the ARM Cortex-M0. The ARM Cortex-M0 is configured to support up to four breakpoints and two watch points.

## 18.2 FEATURES

- Supports ARM Serial Wire Debug (SWD) mode.
- Direct debug access to all memories, registers, and peripherals.
- No target resources are required for the debugging session.
- Up to four breakpoints.
- Up to two data watch points that can also be used as triggers.

## 18.3 PIN DESCRIPTION

| Pin Name | Type | Description                                    | GPIO Configuration |
|----------|------|------------------------------------------------|--------------------|
| SWCLK    | I    | Serial Wire Clock pin in SWD mode.             |                    |
| SWDIO    | I/O  | Serial Wire Data Input/Output pin in SWD mode. |                    |

## 18.4 DEBUG NOTE

### 18.4.1 LIMITATIONS

Debug mode changes the way in which reduced power modes work internal to the ARM Cortex-M0 CPU, and this ripples through the entire system. These differences mean that power measurements should not be made while debugging, the results will be higher than during normal operation in an application.

During a debugging session, the SysTick Timer is automatically stopped whenever the CPU is stopped. Other peripherals are not affected.

### 18.4.2 DEBUG RECOVERY

User code may disable SWD function in order to use P0.8 and P0.9 as GPIO, and may not debug by SWD function to debug or download FW any more.

SONiX provide Boot loader to check the status of P2.2 (BOOT pin) during boot procedure. If P2.2 is Low during Boot procedure, MCU will execute code in Boot loader instead of User code, so SWD function is not disabled.

Exit Boot loader, user code can still configure P2.2 as other functions such as GPIO.

\* **Note: We strongly recommended NOT using BOOT pin as output pin to drive the LED, otherwise, the BOOT pin status may be low during boot procedure.**

### 18.4.3 INTERNAL PULL-UP/DOWN RESISTORS on SWD PINS

To avoid any uncontrolled IO levels, the device embeds internal pull-up and pull-down resistor on the SWD input pins:

- NJTRST: Internal pull-up

- SWDIO/JTMS: Internal pull-up
- SWCLK/JTCK: Internal pull-down

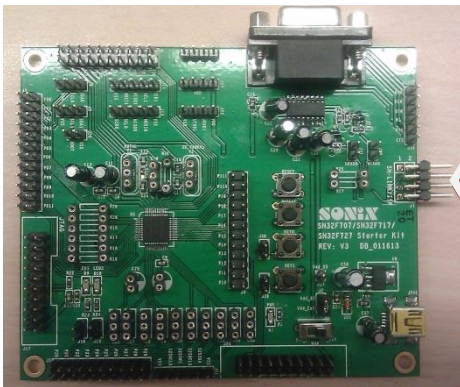
Once a SWD function is disabled by SW, the GPIO controller takes control again.

# 19 DEVELOPMENT TOOL

SONiX provides an Embedded ICE emulator system to offer 32-bit series MCU firmware development.

**SONiX 32-bit series Embedded ICE Emulator System includes:**

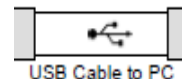
- SONiX 32-bit MCU Starter-Kit.
- SN-LINK-V3
- USB cable to provide communications between the SN-LINK-V3 and PC.
- IDE Tools (KEIL RVMDK)



SONiX 32-bit MCU Starter-Kit.



SN-LINK-V3



USB Cable to PC



IDE Tools

**SONiX 32-bit series Embedded ICE Emulator Feature:**

- ✱ Target's Operating Voltage: 1.8V~5.5V.
- ✱ Up to 4 hardware break points.
- ✱ System clock rate up to 50MHz.
- ✱ Oscillator supports IHRC, ILRC, EHS/ELS X'tal.

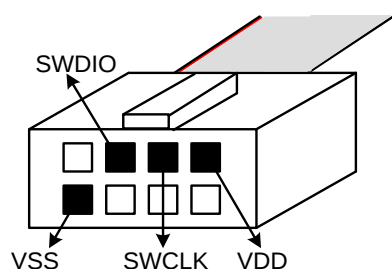
**SONiX 32-bit series Embedded ICE Emulator Limitation:**

- ✱ SWCLK and SWDIO pins are shared with GPIO pins. In embedded ICE mode, the shared GPIO function can't work.

## 19.1 SN-LINK-V3

SN-LINK-V3 is a high speed emulator for SONiX 32-bit MCU. It debugs and programs based on SWD protocol. In addition to debugger functions, the SN-LINK-V3 also may be used as a programmer to load firmware from PC to MCU for engineering production, even mass production.

SN-LINK-V3 communicates with SONiX 32-bit MCU through SWD interface. The pin definition of the Modular cable is as following:



## 19.2 SN32F760 STARTER-KIT

SONiX 32-bit MCU Starter-kit is an easy-development platform. It includes real chip and I/O connectors to input signal or drive extra device of user's application. It is a simple platform to develop application as target board not ready. The starter-kit can be replaced by target board because of integrated SWD debugger circuitry.



- JP23: External Power (USB Type B connector)
- S1: VDD power source is from external power or Writer.
- J9: External power voltage is 5V or 3.3V.
- U3: SN32F769FG real chip.
- D2: Power LED.
- C2.0~C2.13: 14-ch ADC AINx capacitors.
- RESET button: External reset trigger source.
- Y1: External high-speed X'tal
- Y2: External low-speed 32.768KHz X'tal
- JP10: SN-LINK connector
- JP3: Short to force MCU stay in Boot loader.
- JP6: LCD segment connector

\* **Note:** Follow the notice in R-TYPE LCD APPLICATION CIRCUIT, C-TYPE LCD APPLICATION CIRCUIT sections, and the STARTER-KIT introduction section in the datasheet to avoid VDD, VDD1, VDD2, or VDD3 being short with VLCD.

|             | <i>LCD Disabled / R-Type Enabled</i> | <i>C-Type Enabled</i>                                                                                                         |
|-------------|--------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|
| <b>JP19</b> | <b>Short</b>                         | <b>Short</b>                                                                                                                  |
| <b>JP20</b> | <b>Short</b>                         | <b>Open</b>                                                                                                                   |
| <b>JP21</b> | <b>Short</b>                         | Short → P1.0~P1.5 & P0.10~P0.15 are LCD SEGx pins<br>Open → P1.0~P1.5 & P0.10~P0.15 are GPIO pins, and connect VDD2 with VDD. |
| <b>JP22</b> | <b>Short</b>                         | Short → P0.0~P0.7 are LCD SEGx pins<br>Open → P0.0~P0.7 are GPIO pins, and connect VDD3 with VDD with VDD.                    |

# 20 ELECTRICAL CHARACTERISTIC

## 20.1 ABSOLUTE MAXIMUM RATING

|                                           |                         |
|-------------------------------------------|-------------------------|
| Supply voltage (Vdd).....                 | - 0.3V ~ 5.5V           |
| Input in voltage (Vin).....               | Vss – 0.2V ~ Vdd + 0.2V |
| Operating ambient temperature (Topr)..... | -40°C ~ + 85°C          |
| Storage ambient temperature (Tstor) ..... | -40°C ~ + 125°C         |

## 20.2 ELECTRICAL CHARACTERISTIC

| All of voltages refer to Vss, Typical Vdd = 3.3V, Fosc = 12MHz, ambient temperature is 25℃ unless otherwise note. |                    |                                                 |                                                                            |          |      |          |                      |
|-------------------------------------------------------------------------------------------------------------------|--------------------|-------------------------------------------------|----------------------------------------------------------------------------|----------|------|----------|----------------------|
| PARAMETER                                                                                                         | SYM.               | DESCRIPTION                                     |                                                                            | MIN.     | TYP. | MAX.     | UNIT                 |
| Operating Voltage                                                                                                 | Vdd                | Supply voltage for core and external rail       |                                                                            | 1.8      | 3.3  | 5.5      | V                    |
| VDD rise rate                                                                                                     | V <sub>POR</sub>   | VDD rise rate to ensure internal power-on reset |                                                                            | 0.05     | -    | -        | V/ms                 |
| Power Consumption                                                                                                 |                    |                                                 |                                                                            |          |      |          |                      |
| Supply Current                                                                                                    | Idd1               | Normal mode                                     | System clock = 12MHz<br>[1][2][3]                                          | -        | 5    | -        | mA                   |
|                                                                                                                   |                    |                                                 | System clock = 50MHz<br>[1][3][4]                                          | -        | 16   | -        | mA                   |
|                                                                                                                   | Idd2               | Sleep Mode                                      | System clock = 12MHz<br>[1][2][3][5]                                       | -        | 1    | -        | mA                   |
|                                                                                                                   | Idd3               | Sleep Mode                                      | System clock = 32KHz<br>[1][3][5][7]                                       | -        | 100  | -        | uA                   |
|                                                                                                                   | Idd4               | Deep-sleep Mode                                 | Vdd=3.3V<br>[1][3][5]                                                      | -        | 5    | 12       | uA                   |
|                                                                                                                   |                    |                                                 | R-type LCD ON with 1/3 bias, 1/4 duty, 35k bias resistor, LCD rate=ILRC/64 | -        | 10   | 15       | uA                   |
|                                                                                                                   |                    |                                                 | 1C-type LCD ON with 1/3 bias, 1/4 duty, LCD rate=ILRC/64                   | -        | 50   | 65       | uA                   |
|                                                                                                                   |                    |                                                 | 4C-type LCD ON with 1/3 bias, 1/4 duty, LCD rate=ILRC/64                   | -        | 20   | 32       | uA                   |
| Port Pins, RESET pin <sub>[8]</sub>                                                                               |                    |                                                 |                                                                            |          |      |          |                      |
| High-level input voltage                                                                                          | V <sub>IH</sub>    |                                                 |                                                                            | 0.8Vddio | -    | Vddio    | V                    |
| Low-level input voltage                                                                                           | V <sub>IL</sub>    |                                                 |                                                                            | Vss      | -    | 0.2Vddio | V                    |
| Input voltage                                                                                                     | V <sub>i</sub>     |                                                 |                                                                            | 0        | -    | Vddio    | V                    |
| Output voltage                                                                                                    | V <sub>o</sub>     |                                                 |                                                                            | 0        | -    | Vddio    | V                    |
| I/O port pull-up resistor                                                                                         | R <sub>PU</sub>    | Vin = Vss , Vddio = 5.0V                        |                                                                            | 50       | 75   | 100      | KΩ                   |
| I/O port pull-down resistor                                                                                       | R <sub>PD</sub>    | Vin = 5.0V                                      |                                                                            | 50       | 75   | 100      | KΩ                   |
| I/O High-level output source current                                                                              | I <sub>OH</sub>    | Typical 10mA mode                               | V <sub>OP</sub> = Vddio– 0.5V                                              | 5        | 10   | -        | mA                   |
|                                                                                                                   |                    | Typical 20mA mode                               |                                                                            | 12       | 20   | -        | mA                   |
| I/O Low-level output sink current                                                                                 | I <sub>OL</sub>    | Typical 10mA mode                               | V <sub>OP</sub> = Vss + 0.5V                                               | 5        | 10   | -        | mA                   |
|                                                                                                                   |                    | Typical 20mA mode                               |                                                                            | 12       | 20   | -        | mA                   |
| ADC                                                                                                               |                    |                                                 |                                                                            |          |      |          |                      |
| ADC Operating Voltage                                                                                             | V <sub>ADC</sub>   |                                                 |                                                                            | 2.5      | -    | 5.5      | V                    |
| AIN0 ~ AIN13 input voltage                                                                                        | V <sub>ani</sub>   |                                                 |                                                                            | 0        | -    | Avrefh   | V                    |
| ADC reference Voltage                                                                                             | V <sub>ref</sub>   |                                                 |                                                                            | 2.5      | -    | -        | V                    |
| *ADC enable time                                                                                                  | T <sub>ast</sub>   | Ready to start convert after set ADENB = “1”    |                                                                            | 100      | -    | -        | us                   |
| *ADC current consumption                                                                                          | I <sub>ADC</sub>   | Vdd=3.3V, ADS=0                                 |                                                                            | -        | 220  | -        | uA                   |
| ADC Clock Frequency                                                                                               | F <sub>ADCLK</sub> | Vdd=3.3V                                        |                                                                            | -        | -    | 16       | MHz                  |
| ADC Conversion Cycle Time                                                                                         | F <sub>ADCYL</sub> | VDD=2.5V~5.5V                                   |                                                                            | 64       | -    | -        | 1/F <sub>ADCLK</sub> |

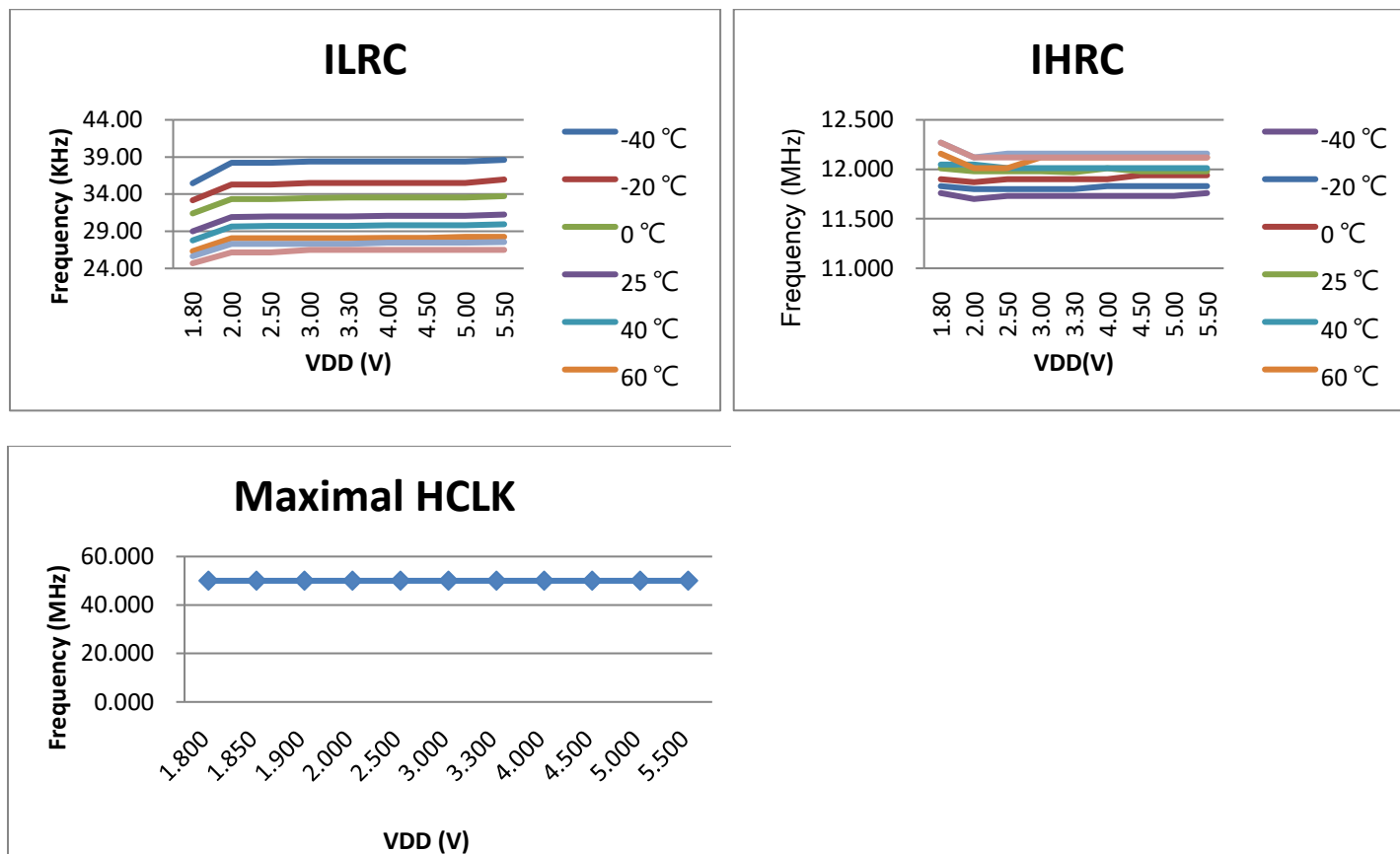
|                               |                        |                                                    |         |       |       |       |   |
|-------------------------------|------------------------|----------------------------------------------------|---------|-------|-------|-------|---|
| ADC Sampling Rate             | F <sub>ADSMP</sub>     | Vdd=3.3V                                           | -       | -     | 250   | KHz   |   |
| Differential Nonlinearity     | DNL                    | Vdd=5.5V , AVREFH=2.4V                             | -1      | -     | +1    | LSB   |   |
| Integral Nonlinearity         | INL                    | Vdd=5.5V , AVREFH=2.4V                             | -1      | -     | +1    | LSB   |   |
| No Missing Code               | NMC                    | Vdd=5.5V , AVREFH=2.4V                             | 10      | -     | 12    | Bits  |   |
| ADC offset Voltage            | V <sub>ADCOffset</sub> |                                                    | -5      | -     | +5    | mV    |   |
| Temperature sensor Range      | TR                     | Temperature Sensor Operation Range                 | -10     | -     | +70   | ℃     |   |
| Temperature Sensitivity       | TS                     | Temperature Sensor Sensitivity.                    | -       | 3.53  | -     | mV/℃  |   |
| Temperature Sensor Accuracy   | ETS                    | One Temperature point Calibration.                 | -10     | -     | +10   | %     |   |
|                               |                        | Two Temperature points Calibration.                | -1      | -     | +1    | %     |   |
| FLASH                         |                        |                                                    |         |       |       |       |   |
| Supply Voltage                | Vdd1                   |                                                    | 1.8     | -     | Vdd   | V     |   |
| Endurance time                | T <sub>EN</sub>        | Erase + Program                                    | 20K     | *100K | -     | Cycle |   |
| Page erase time               | T <sub>PE</sub>        | 1-Page (1024 bytes).                               | -       | 25    | 30    | ms    |   |
| 1-Word Programming time       | T <sub>PG</sub>        | 1-Word (32 bits).                                  | -       | 60    | 70    | us    |   |
| LCD Driver                    |                        |                                                    |         |       |       |       |   |
| R-Type LCD Operation Current  | I <sub>RLCD</sub>      | Vdd = 3.3V, 1/3 bias, 400k,bias resistor, No panel | -       | 3     | 5     | uA    |   |
|                               |                        | Vdd = 3.3V, 1/3 bias, 35k,bias resistor, No panel  | -       | 5     | 10    | uA    |   |
| 1C-Type LCD Operation Current | I <sub>1CLCD</sub>     | Vdd = 3.3V, 1/3 bias, No panel                     | -       | 18    | 25    | uA    |   |
| 4C-Type LCD Operation Current | I <sub>4CLCD</sub>     | Vdd = 3.3V, 1/3 bias, No panel                     | -       | 7     | 15    | uA    |   |
| C-Type VLCD Output Voltage    | V <sub>LCD1</sub>      | Vdd = 1.8~5.5V. VCP[3:0] = 0011b                   | 2.85    | 3.0   | 3.15  | V     |   |
| MISC                          |                        |                                                    |         |       |       |       |   |
| Low Voltage Detector          | LVD                    | Interrupt/Reset                                    | Level 0 | 1.70  | 1.80  | 1.90  | V |
|                               |                        |                                                    | Level 1 | 1.90  | 2.00  | 2.10  | V |
|                               |                        |                                                    | Level 2 | 2.30  | 2.40  | 2.50  | V |
|                               |                        |                                                    | Level 3 | 2.80  | 2.70  | 2.60  | V |
|                               |                        |                                                    | Level 4 | 2.90  | 3.00  | 3.10  | V |
|                               |                        |                                                    | Level 5 | 3.50  | 3.60  | 3.70  | V |
| IHRC Freq.                    | F <sub>IHRC</sub>      | T=25℃, Vdd=1.8V~ 5.5V                              | 11.88   | 12    | 12.12 | MHz   |   |
|                               |                        | T=-40℃~85℃, Vdd=1.8V~5.5V                          | 11.70   | 12    | 12.30 | MHz   |   |
| ESD_HBM                       | V <sub>ESD_HBM</sub>   | ESD human body mode                                | 2500    | -     | -     | V     |   |
| ESD_MM                        | V <sub>ESD_MM</sub>    | ESD machine mode                                   | 250     | -     | -     | V     |   |

**\* These parameters are for design reference, not tested.**

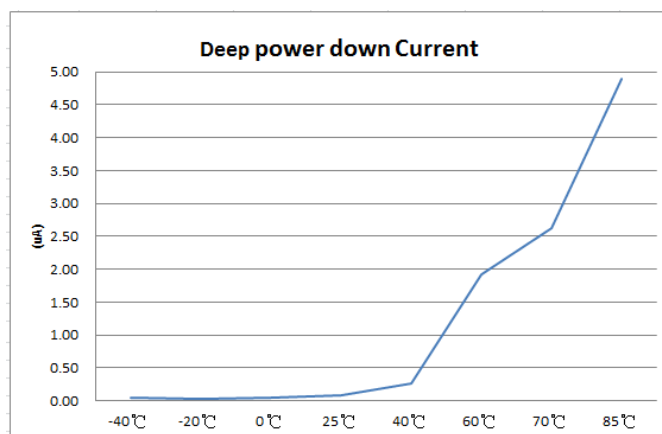
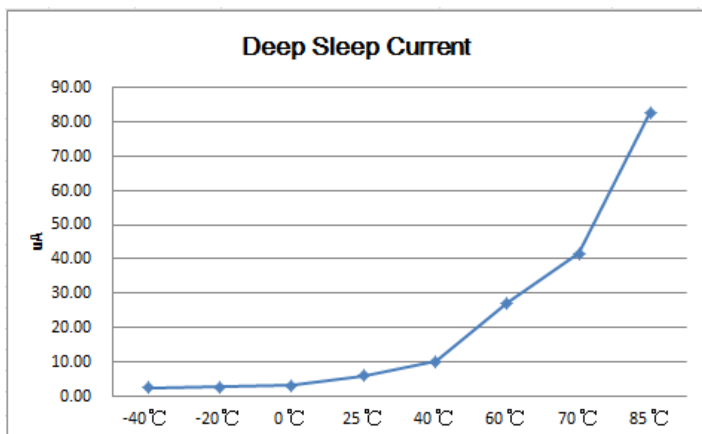
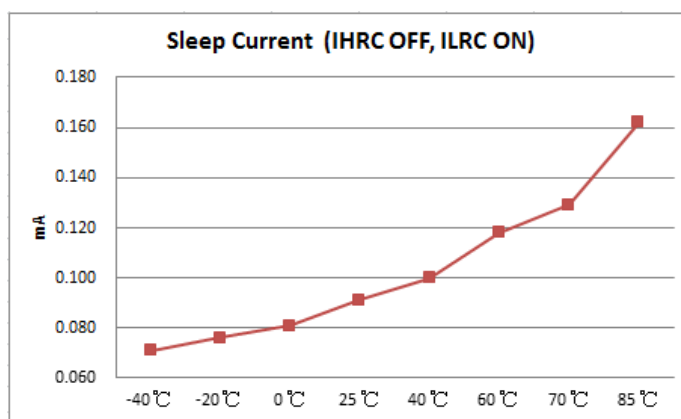
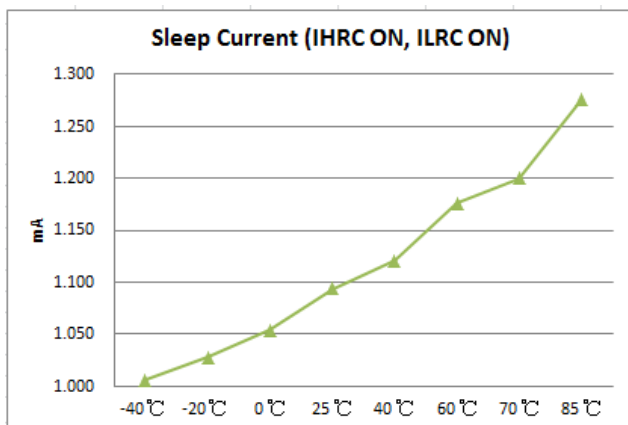
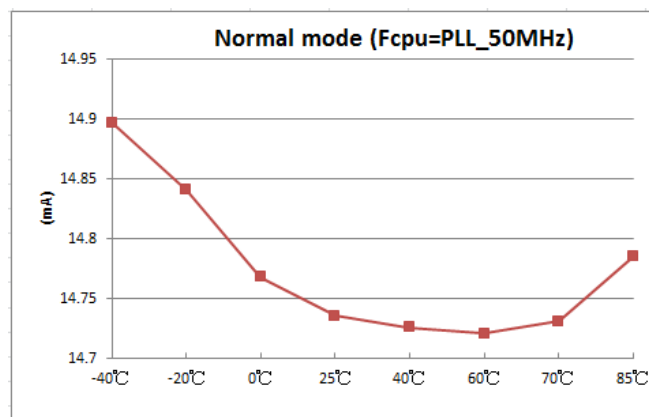
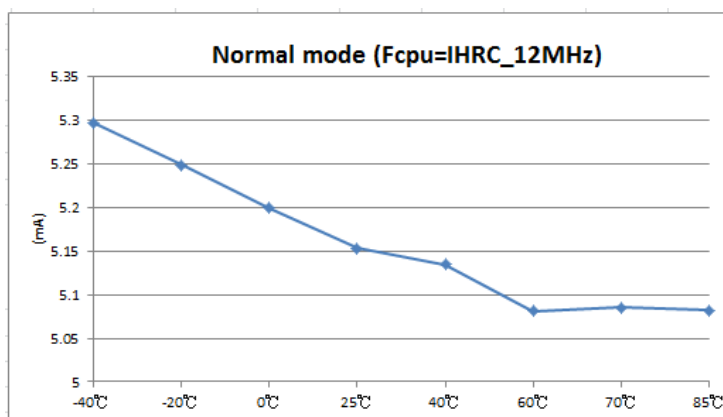
- [1] I<sub>DD</sub> measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled and VDD=3.3V
- [2] IHRC and ILRC are enabled, external X'tal is disabled, and PLL is disabled.
- [3] LVD and all peripherals are disabled.
- [4] IHRC is disabled, external high X'tal is enabled, and PLL is enabled.
- [5] All oscillators and analog blocks are turned off.
- [6] DPDWAKEUP pin is pulled HIGH internally.
- [7] ILRC is enabled, IHRC and external X'tal are disabled, and PLL is disabled.
- [8] VDD is the Vddio of P0.8~P0.9, P2.0~P2.15, and P3.10~P3.15; VDD1 is the Vddio of P1.6~P1.15, and P3.0~P3.9; VDD2 is the Vddio of P1.0~P1.5, and P0.10~P0.15; VDD3 is the Vddio of P0.0~P0.7.

## 20.3 CHARACTERISTIC GRAPHS

The Graphs in this section are for design guidance, not tested or guaranteed. In some graphs, the data presented are outside specified operating range. This is for information only and devices are guaranteed to operate properly only within the specified range.



\*Supply Current V.S. Operating Temperature (Operating Conditions: All pins configured as GPIO outputs driven Low and pull-up resistors disabled and VDD = 3.3V)

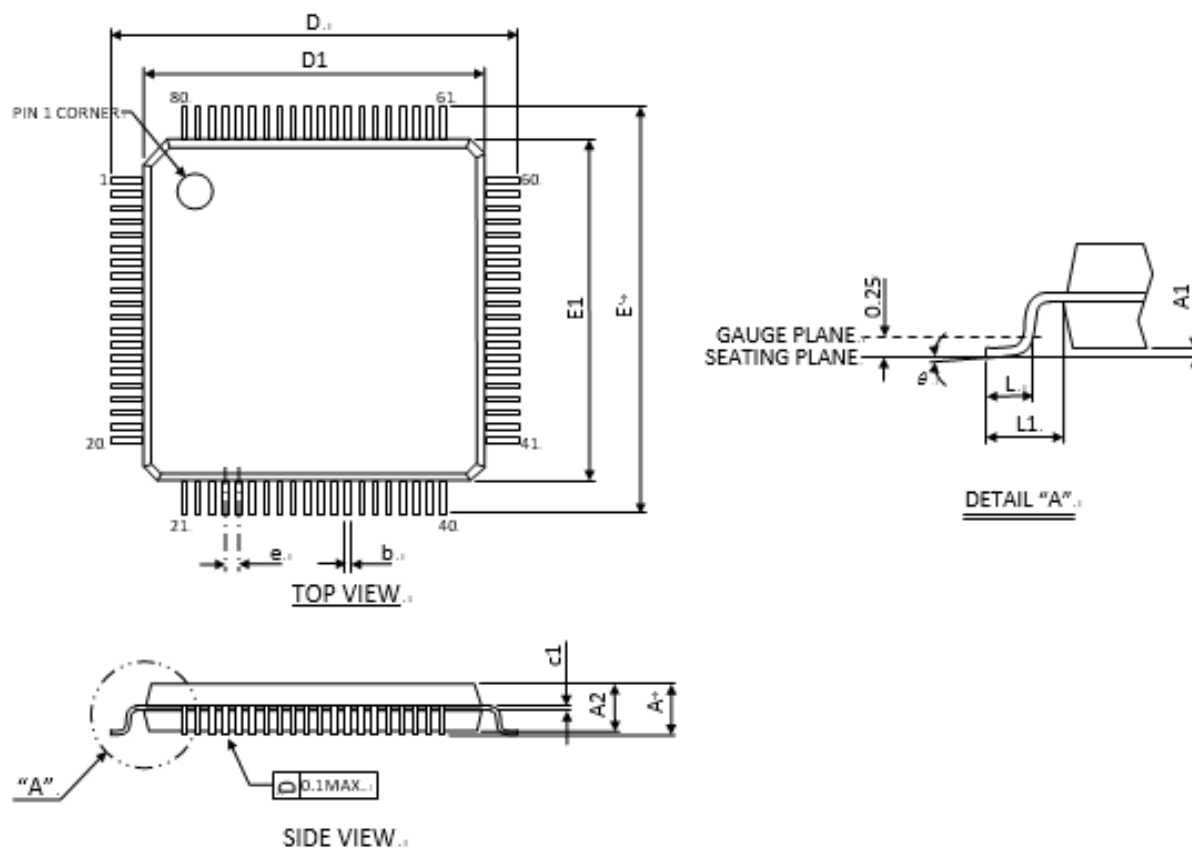


# 21 FLASH ROM PROGRAMMING PIN

| Programming Information of SN32F760/750/740/730 Series |          |                               |       |                        |       |                        |       |                        |       |                        |       |
|--------------------------------------------------------|----------|-------------------------------|-------|------------------------|-------|------------------------|-------|------------------------|-------|------------------------|-------|
| Chip Name                                              |          | SN32F769F<br>SN32F759F        |       | SN32F768F<br>SN32F758F |       | SN32F767F<br>SN32F757F |       | SN32F766J<br>SN32F756J |       | SN32F765J<br>SN32F755J |       |
| Writer Connector<br>JP5                                |          | Flash IC / JP3 Pin Assignment |       |                        |       |                        |       |                        |       |                        |       |
| Number                                                 | Name     | Number                        | Pin   | Number                 | Pin   | Number                 | Pin   | Number                 | Pin   | Number                 | Pin   |
| 1                                                      | VDD      | 20<br>41<br>42<br>67          | VDD   | 16<br>33<br>34<br>55   | VDD   | 13<br>25<br>39         | VDD   | 12<br>23<br>37         | VDD   | 10<br>17<br>24         | VDD   |
| 2                                                      | GND      | 17<br>51<br>69                | VSS   | 56                     | VSS   | 40                     | VSS   | 38                     | VSS   | 25                     | VSS   |
| 3                                                      | CLK      | 74                            | P3.12 | 61                     | P3.12 | 45                     | P3.12 | 43                     | P3.12 | 30                     | P3.12 |
| 4                                                      | CE       |                               |       |                        |       |                        |       |                        |       |                        |       |
| 5                                                      | PGM      | 71                            | P0.8  | 58                     | P0.8  | 42                     | P0.8  | 40                     | P0.8  | 27                     | P0.8  |
| 6                                                      | OE       | 70                            | P0.9  | 57                     | P0.9  | 41                     | P0.9  | 39                     | P0.9  | 26                     | P0.9  |
| 7                                                      | D1       |                               |       |                        |       |                        |       |                        |       |                        |       |
| 8                                                      | D0       |                               |       |                        |       |                        |       |                        |       |                        |       |
| 9                                                      | D3       |                               |       |                        |       |                        |       |                        |       |                        |       |
| 10                                                     | D2       |                               |       |                        |       |                        |       |                        |       |                        |       |
| 11                                                     | D5       |                               |       |                        |       |                        |       |                        |       |                        |       |
| 12                                                     | D4       |                               |       |                        |       |                        |       |                        |       |                        |       |
| 13                                                     | D7       |                               |       |                        |       |                        |       |                        |       |                        |       |
| 14                                                     | D6       |                               |       |                        |       |                        |       |                        |       |                        |       |
| 15                                                     | VDD      |                               |       |                        |       |                        |       |                        |       |                        |       |
| 16                                                     | -        |                               |       |                        |       |                        |       |                        |       |                        |       |
| 17                                                     | HLS      |                               |       |                        |       |                        |       |                        |       |                        |       |
| 18                                                     | RST      |                               |       |                        |       |                        |       |                        |       |                        |       |
| 19                                                     | -        |                               |       |                        |       |                        |       |                        |       |                        |       |
| 20                                                     | ALSB/PDB | 73                            | P3.11 | 60                     | P3.11 | 44                     | P3.11 | 42                     | P3.11 | 29                     | P3.11 |

# 22 PACKAGE INFORMATION

## 22.1 LQFP 80 PIN

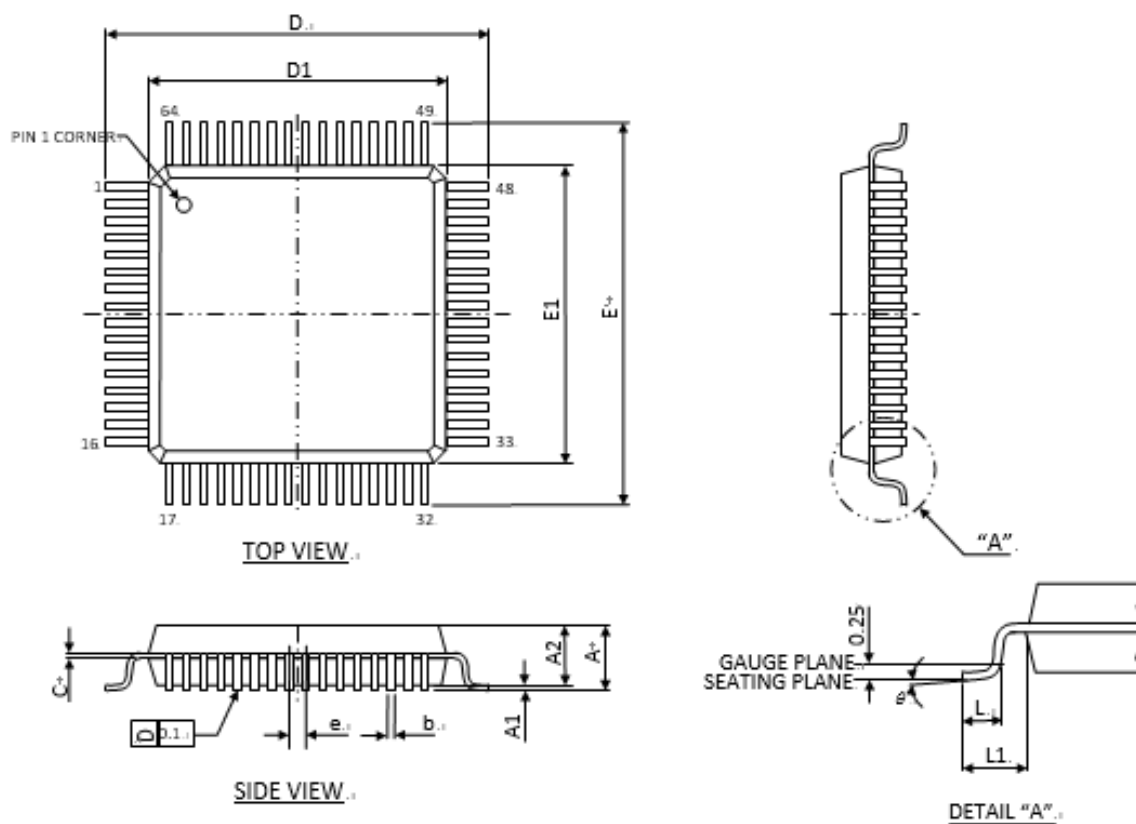


| SYMBOLS | Dimension in mm |      |      | Dimension in inch |       |       |
|---------|-----------------|------|------|-------------------|-------|-------|
|         | MIN.            | NOM. | MAX. | MIN.              | NOM.  | MAX.  |
| A       | —               | —    | 1.60 | —                 | —     | 0.063 |
| A1      | 0.05            | —    | 0.2  | 0.002             | —     | 0.008 |
| A2      | 1.35            | 1.40 | 1.45 | 0.053             | 0.055 | 0.057 |
| b       | 0.13            | 0.18 | 0.23 | 0.005             | 0.007 | 0.009 |
| c1      | 0.09            | —    | 0.18 | 0.004             | —     | 0.007 |
| D       | 12 BSC          |      |      | 0.472 BSC         |       |       |
| D1      | 10 BSC          |      |      | 0.394 BSC         |       |       |
| e       | 0.4 BSC         |      |      | 0.016 BSC         |       |       |
| E       | 12 BSC          |      |      | 0.472 BSC         |       |       |
| E1      | 10 BSC          |      |      | 0.394 BSC         |       |       |
| L       | 0.45            | 0.60 | 0.75 | 0.018             | 0.024 | 0.030 |
| L1      | 1.0 REF         |      |      | 0.039 REF         |       |       |
| θ       | 0°              | 3.5° | 7°   | 0°                | 3.5°  | 7°    |

Notes :

1. CONTROLLING DIMENSION : MILLIMETER (mm).
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

## 22.2 LQFP 64 PIN

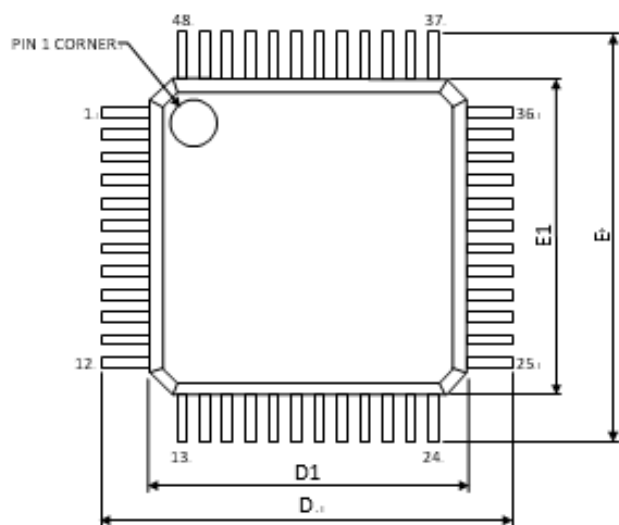


| SYMBOLS | Dimension in mm |      |      | Dimension in inch |       |       |
|---------|-----------------|------|------|-------------------|-------|-------|
|         | MIN             | NOM  | MAX  | MIN               | NOM   | MAX   |
| A       | —               | —    | 1.60 | —                 | —     | 0.063 |
| A1      | 0.05            | —    | 0.25 | 0.002             | —     | 0.01  |
| A2      | 1.35            | 1.40 | 1.45 | 0.053             | 0.055 | 0.057 |
| b       | 0.13            | 0.19 | 0.25 | 0.005             | 0.007 | 0.010 |
| c       | 0.09            | —    | 0.20 | 0.004             | —     | 0.008 |
| D       | 9.00 BSC        |      |      | 0.354 BSC         |       |       |
| D1      | 7.00 BSC        |      |      | 0.276 BSC         |       |       |
| e       | 0.40 BSC        |      |      | 0.016 BSC         |       |       |
| E       | 9.00 BSC        |      |      | 0.354 BSC         |       |       |
| E1      | 7.00 BSC        |      |      | 0.276 BSC         |       |       |
| L       | 0.4             | 0.60 | 0.8  | 0.016             | 0.024 | 0.032 |
| L1      | 1.00 REF        |      |      | 0.039 REF         |       |       |
| θ       | 0°              | 3.5° | 7°   | 0°                | 3.5°  | 7°    |

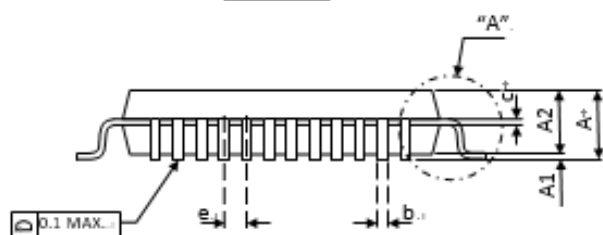
Notes :

1. CONTROLLING DIMENSION : MILLIMETER (mm).
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

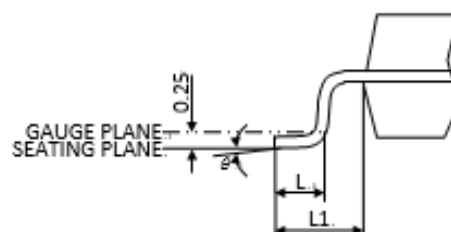
## 22.3 LQFP 48 PIN



**TOP VIEW**



**SIDE VIEW**



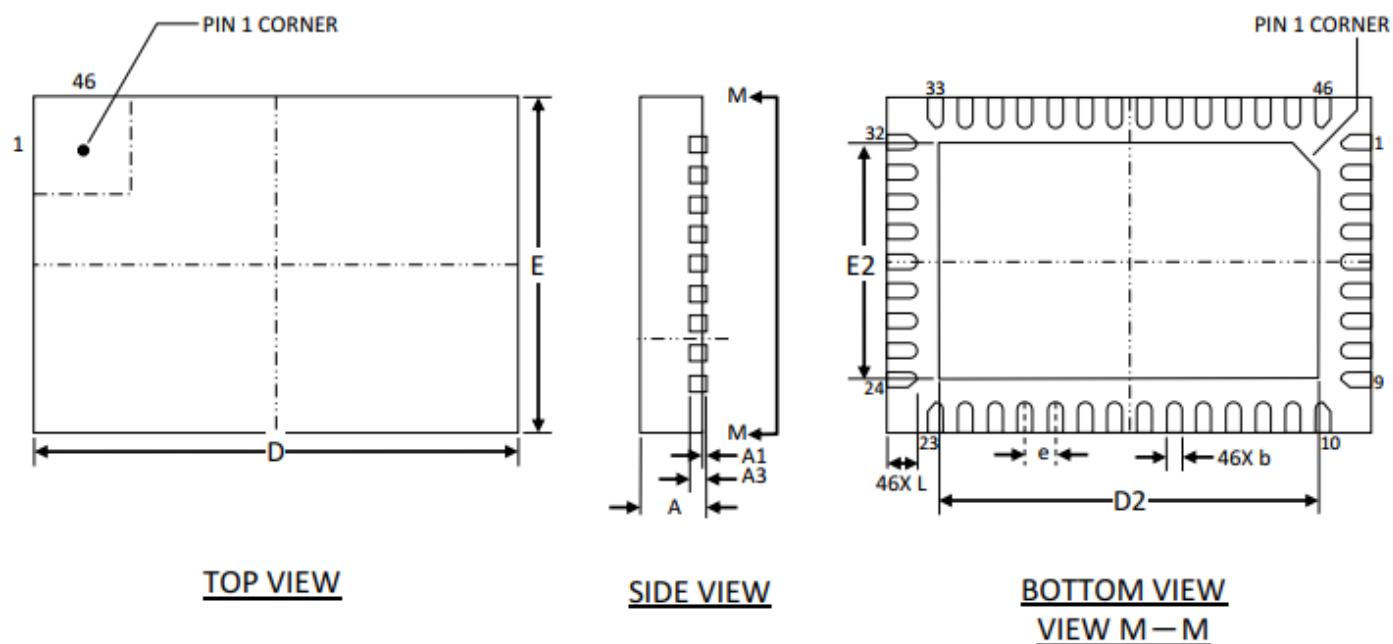
**DETAIL "A"**

| SYMBOLS | Dimension in mm |      |      | Dimension in inch |       |       |
|---------|-----------------|------|------|-------------------|-------|-------|
|         | MIN             | NOM  | MAX  | MIN               | NOM   | MAX   |
| A       | --              | --   | 1.60 | --                | --    | 0.063 |
| A1      | 0.05            | --   | 0.15 | 0.002             | --    | 0.006 |
| A2      | 1.35            | 1.40 | 1.45 | 0.053             | 0.055 | 0.057 |
| b       | 0.17            | 0.22 | 0.27 | 0.007             | 0.009 | 0.011 |
| c       | 0.09            | --   | 0.20 | 0.004             | --    | 0.008 |
| D       | 9.00 BSC        |      |      | 0.354 BSC         |       |       |
| D1      | 7.00 BSC        |      |      | 0.276 BSC         |       |       |
| E       | 9.00 BSC        |      |      | 0.354 BSC         |       |       |
| E1      | 7.00 BSC        |      |      | 0.276 BSC         |       |       |
| e       | 0.50 BSC        |      |      | 0.020 BSC         |       |       |
| L       | 0.40            | 0.60 | 0.80 | 0.016             | 0.024 | 0.031 |
| L1      | 1.00 REF        |      |      | 0.039 REF         |       |       |
| θ       | 0°              | 3.5° | 7°   | 0°                | 3.5°  | 7°    |

Notes :

1. CONTROLLING DIMENSION : MILLIMETER (mm).
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

## 22.4 QFN 46 PIN

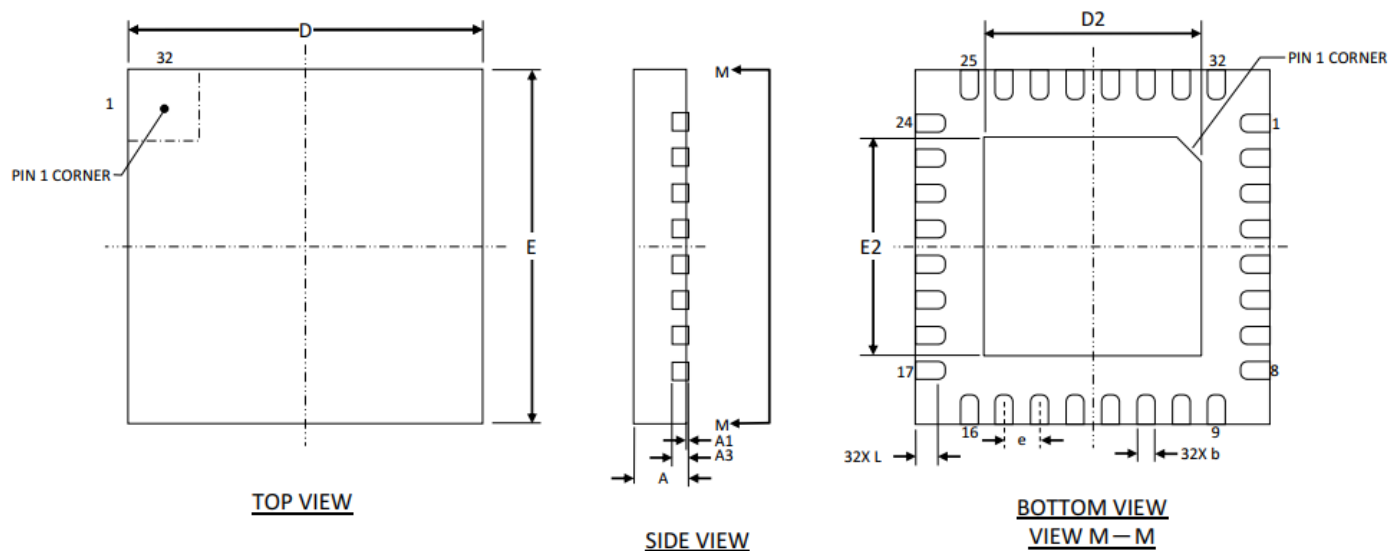


| SYMBOLS | Dimension in mm |      |      | Dimension in inch |       |       |
|---------|-----------------|------|------|-------------------|-------|-------|
|         | MIN.            | NOM. | MAX. | MIN.              | NOM.  | MAX.  |
| A       | 0.70            | 0.80 | 0.90 | 0.028             | 0.031 | 0.035 |
| A1      | 0.00            | 0.02 | 0.05 | 0.000             | 0.001 | 0.002 |
| A3      | 0.203 REF       |      |      | 0.008 REF         |       |       |
| b       | 0.20            | 0.25 | 0.30 | 0.008             | 0.010 | 0.012 |
| D       | 6.40            | 6.50 | 6.60 | 0.252             | 0.256 | 0.260 |
| E       | 4.40            | 4.50 | 4.60 | 0.173             | 0.177 | 0.181 |
| e       | 0.40 BSC        |      |      | 0.016 BSC         |       |       |
| D2      | 5.00            | 5.10 | 5.20 | 0.197             | 0.201 | 0.205 |
| E2      | 3.00            | 3.10 | 3.20 | 0.118             | 0.122 | 0.126 |
| L       | 0.30            | 0.40 | 0.50 | 0.012             | 0.016 | 0.020 |

Notes :

1. CONTROLLING DIMENSION : MILLIMETER (mm)

## 22.5 QFN 33 PIN 5x5



| SYMBOLS | Dimension in mm |      |      | Dimension in inch |       |       |
|---------|-----------------|------|------|-------------------|-------|-------|
|         | MIN.            | NOM. | MAX. | MIN.              | NOM.  | MAX.  |
| A       | 0.70            | 0.80 | 0.90 | 0.028             | 0.031 | 0.035 |
| A1      | 0.00            | 0.02 | 0.05 | 0.000             | 0.001 | 0.002 |
| A3      | 0.203 REF       |      |      | 0.008 REF         |       |       |
| b       | 0.18            | 0.25 | 0.30 | 0.007             | 0.010 | 0.012 |
| D       | 4.90            | 5.00 | 5.10 | 0.193             | 0.197 | 0.201 |
| E       | 4.90            | 5.00 | 5.10 | 0.193             | 0.197 | 0.201 |
| e       | 0.50 BSC        |      |      | 0.020 BSC         |       |       |
| D2      | 3.00            | 3.30 | 3.60 | 0.118             | 0.130 | 0.142 |
| E2      | 3.00            | 3.30 | 3.60 | 0.118             | 0.130 | 0.142 |
| L       | 0.30            | 0.40 | 0.50 | 0.012             | 0.016 | 0.020 |

Notes :

1. CONTROLLING DIMENSION : MILLIMETER (mm)

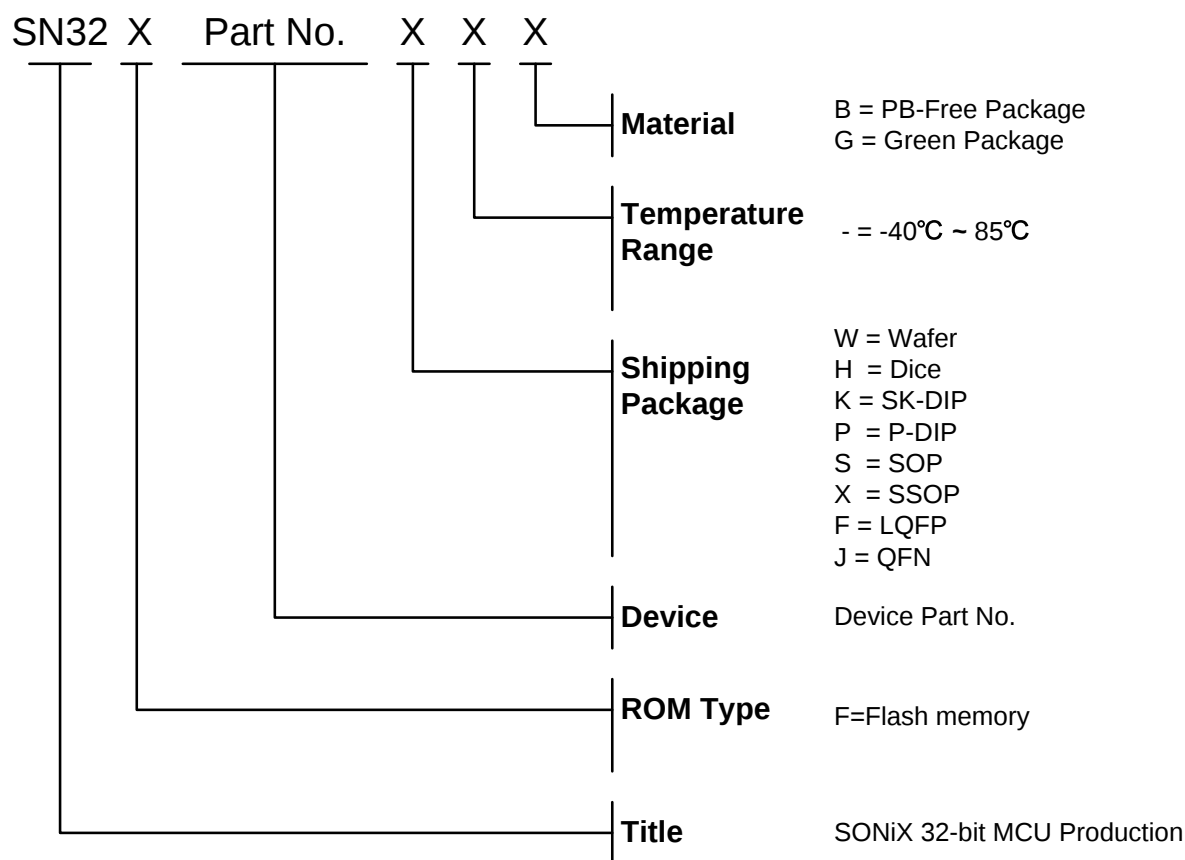
# 23 MARKING DEFINITION

## 23.1 INTRODUCTION

There are many different types in SONiX 32-bit MCU production line.

This note lists the marking definitions of all 32-bit MCU for order or obtaining information.

## 23.2 MARKING INDETIFICATION SYSTEM

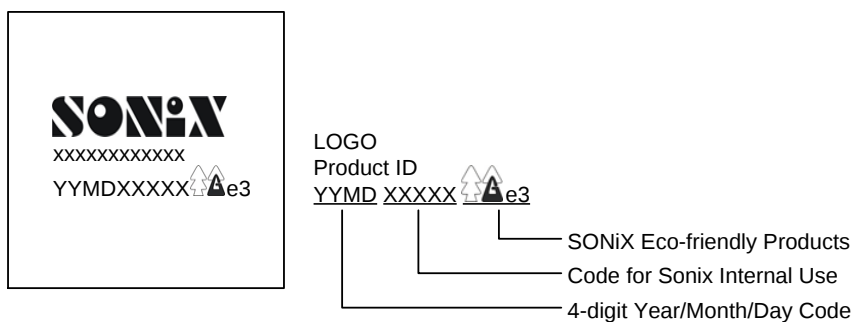


## 23.3 MARKING EXAMPLE

| Name       | ROM Type     | Device | Package | Temperature | Material      |
|------------|--------------|--------|---------|-------------|---------------|
| SN32F769FG | Flash memory | 769    | LQFP    | -40℃~85℃    | Green Package |
| SN32F768FG | Flash memory | 769    | LQFP    | -40℃~85℃    | Green Package |
| SN32F767FG | Flash memory | 769    | LQFP    | -40℃~85℃    | Green Package |
| SN32F769W  | Flash memory | 769    | Wafer   | -40℃~85℃    | -             |
| SN32F769H  | Flash memory | 769    | Dice    | -40℃~85℃    | -             |
| SN32F766JG | Flash memory | 769    | QFN     | -40℃~85℃    | Green Package |
| SN32F765JG | Flash memory | 769    | QFN     | -40℃~85℃    | Green Package |
| SN32F759FG | Flash memory | 759    | LQFP    | -40℃~85℃    | Green Package |
| SN32F758FG | Flash memory | 759    | LQFP    | -40℃~85℃    | Green Package |
| SN32F757FG | Flash memory | 759    | LQFP    | -40℃~85℃    | Green Package |
| SN32F756JG | Flash memory | 759    | QFN     | -40℃~85℃    | Green Package |
| SN32F755JG | Flash memory | 759    | QFN     | -40℃~85℃    | Green Package |

## 23.4 DATECODE SYSTEM

The figure below is an example of the marking. Contents such as the product ID or symbol may vary according to different packages.



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