SN32F290 Series

USER'S MANUAL

SN32F299
SN32F298
SN32F297

SONiX 32-Bit Cortex-M0 Micro-Controller

SONIX reserves the right to make change without further notice to any products herein to improve reliability, function or design. SONIX does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others. SONIX products are not designed, intended, or authorized for us as components in systems intended, for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SONIX product could create a situation where personal injury or death may occur. Should Buyer purchase or use SONIX products for any such unintended or unauthorized application. Buyer shall indemnify and hold SONIX and its officers, employees, subsidiaries, affiliates and distributors harmless against all claims, cost, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use even if such claim alleges that SONIX was negligent regarding the design or manufacture of the part.

AMENDMENT HISTORY

Version	Date	Description
1.0	2020/07/16	First version released.
1.1	2020/12/17	1. Fix typing errors. 2. Fix typing errors in Chap 10. 16-BIT TIMER WITH CAPTURE FUNCTION. 3. Update 4.4.2 WAKEUP TIME. 4. Add notice "User SHALL fill in more or equal to 8 bytes to FLASH_DATA register when programming the ROM." In 21.8.2 PROGRAM FLASH MEMORY. 5. Update 21.11.1 FLASH_LPCTRL register. 6. Fix the Pin Descriptions of VDDIO1. 7. Fix typing in 15.5 BAUD RATE CALCULATION & UART n Fractional Divider register (UARTn_FD).
1.2	2021/03/15	1. Fix the typing error of CMP output debounce register. 2. Add the 15.7.7 UART n FIFO Control register (UARTn_FIFOCTRL) & 15.7.14 UART n Half-duplex Enable register (UARTn_HDEN).
1.3	2021/07/16	1. Update 3.3.7 SYS0_LVDCTRL register.
1.4	2022/02/22	1. Update 1.5 PIN ALLOCATION TABLE for P0.11. 2. Fix the Description of 3.4.1 AHB Clock Enable register. 3. Remove USBRST of 3.4.4 Peripheral Reset register. 4. Fix the Reset Value of 20.9 USB REGISTERS. 5. Update 21.11.1 FLASH_LPCTRL register. 6. Remove 21.11.3 FLASH_CTRL note. 7. Add notice "Value must be multiples of 8 in the FLASH_ADDR register." In 21.11.5 FLASH_ADDR.
1.5	2022/10/17	1. Fix the typing error of PFPA_SPI register. 2. Fix the typing error of CMP Control register. 3. Modify pin circuit diagrams in 1.7 PIN CIRCUIT DIAGRAMS. 4. Modify circuit diagrams in 8.2.1 COMPARATOR ENABLE.
1.6	2023/05/15	1. Remove the Touch Key. 2. Update the graph of IHRC in 24.3 CHARACTERISTIC GRAPHS. 3. Update 24.7 DATECODE SYSTEM.
1.7	2024/05/23	1. Update 1.7 PIN CIRCUIT DIAGRAMS 2. Update 25 FLASH ROM PROGRAMMING PIN 3. Add new chapter 13.6 TIMING CHARACTERISTICS 4. Add ESD result in 24.2 ELECTRICAL CHARACTERISTIC. 5. Modify typing errors of description in 10.8.15 CT16Bn Match register 0~11 (CT16Bn_MR0~11) (n=1) and 10.8.16 CT16Bn Match register 12 (CT16Bn_MR12) (n=1) 6. Update 26 PACKAGE INFORMATION diagram
1.8	2025/12/19	1. Add notice in 10.8.5 CT16Bn Prescale register (CT16Bn_PRE) (n=0,1,2,3,4,5) and 10.8.7 CT16Bn Count Control register (CT16Bn_CNTCTRL) (n=0,1,2,3,4,5). 2. Add notice in 4.3.2 DEEP-SLEEP MOSE.

Table of Content

1 PRODUCT OVERVIEW

1.1 FEATURES

- **Memory configuration**
  256KB on-chip Flash programming memory.
  32KB SRAM.
  4KB Boot ROM

- **Operation Frequency up to 48MHz**

- **Interrupt sources**
  ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).

- **I/O pin configuration**
  Up to 74 General Purpose I/O (GPIO) pins with configurable pull-up resistors.
  GPIO pins can be used as edge and level sensitive interrupt sources.
  Up to 6 High-current (100 mA) output sink pins: P0.0, P0.1, P0.2, P0.3, P1.12, P1.13
  All IO 20mA driving/sinking current
  4 GPIO pins with configurable pull-down resistors: P3.10, P3.11, P3.12, P3.13

- **Programmable Watchdog Timer (WDT)**
  Programmable watchdog frequency with watchdog clock source and divider.

- **System tick timer**
  The 24-bit SysTick timer clock source is fixed to the system clock, and is intended to generate a fixed 10-ms interrupt.

- **Real-Time Clock (RTC)**

- **LVD with separate thresholds**
  Reset: 1.35V for V_{CORE} 1.5V
  Reset: 2.7V/3.0V/3.6V for VDD
  Interrupt: 2.7V/3.0V/3.6V for VDD

- **Fcpu (Instruction cycle)**
  $F_{CPU} = F_{HCLK} = F_{SYSCLK}/1$, $F_{SYSCLK}/2$, $F_{SYSCLK}/4$, …, $F_{SYSCLK}/128$

- **Operating modes**
  Normal, Sleep, Deep-sleep

- **Cyclic Redundancy Check (CRC)**
  CRC-16
  CRC-16-CCCITT
  CRC-32

- **Serial Wire Debug (SWD)**

- **Timer**
  3 16-bit timer support up-counting, down-counting, and center-aligned mode.
  3 16-bit timers support up-counting mode.
  28 sets PWM
  8 sets inverse PWM with programmable dead-band
  PCLK up to 96MHz

- **Working voltage 2.5V ~ 5.5V**

- **12-bit SAR ADC with 12 external and 3 internal channels, and 4-level Int. Ref. Voltage**
  16 external ADC input
  1 internal battery measurement
  2 internal channels from OPA0 and OPA1 outputs.
  4-level internal reference voltage source (VDD, 4.5V, 3V, 2V)

- **3 Rail to Rail Comparators**
  Internal reference voltage source 3V/2V/1.5V
  Programmable 16-level internal ref. voltage divider
  3 external negative inputs
  3 external positive inputs

- **2 OPA**
  Internal reference voltage source 3V/2V/1.5V shared with CMP

- **Interface**
  -Two I2C controllers supporting I2C-bus specification with multiple address recognition.
  -Four UART controllers with fractional baud rate generation.
  -Two SPI controllers.
  - EBI (8080 included) interface
  - Two I2S controllers with mono and stereo audio data supported, MSB justified data format supported, and can operate as either master or slave.

- **System clocks**
  -External high clock: Crystal type 10MHz~25MHz
  -External low clock: Crystal type 32.768 KHz
  -Internal high clock: RC type 12 MHz
  -Internal low clock: RC type 32 KHz
  -PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal.
  -Clock output function which can reflect the internal high/low RC oscillator, HCLK, PLL output, and external low clock.

- **In-Circuit Programming (ICP) supported**

- **LCD driver**
  Support R-type
  Up to 8 com
  4x40 or 6x38 or 7x37 or 8x36 dots
  1/3 bias voltage
  Adjustable VLCD Voltage: 0.5xVcc~Vcc
  Support 1/4 duty, 1/6 duty, 1/7 duty, and 1/8 duty
  LCD pin shared with I/O

- **Full Speed USB 2.0**
  3.3v regulator output for D+ internal 1.5k pull-up resistor.
  Supports one Full speed USB device address.
  Supports PS/2 mode.
  One control EP and 6 configurable INT/BULK Endpoints.
  EP0 supports 64-byte FIFO depth.
  Programmable EP1~EP6 FIFO depth.
  Total 7 endpoints share 512-byte USB RAM.

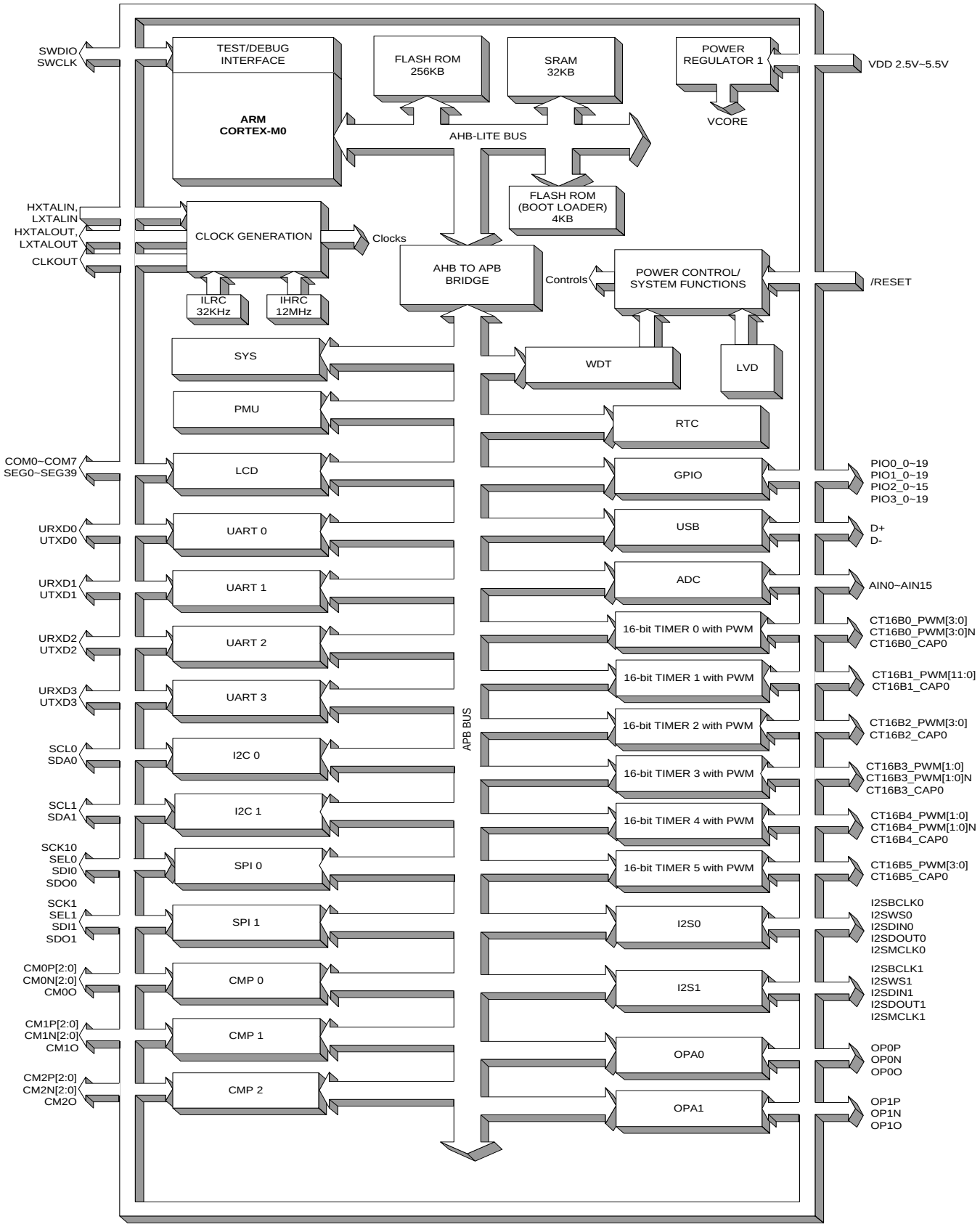
- **3.3V Regulator output**
  Driving current 60mA
  Power for USB D+ internal pull-up resistor.
  Can be IO power for P0.12~P0.15, P3.0~P3.6, P1.6~P1.11. (3.3V IOs)

- **Package (Chip form support)**
  LQFP80/64/48 pin

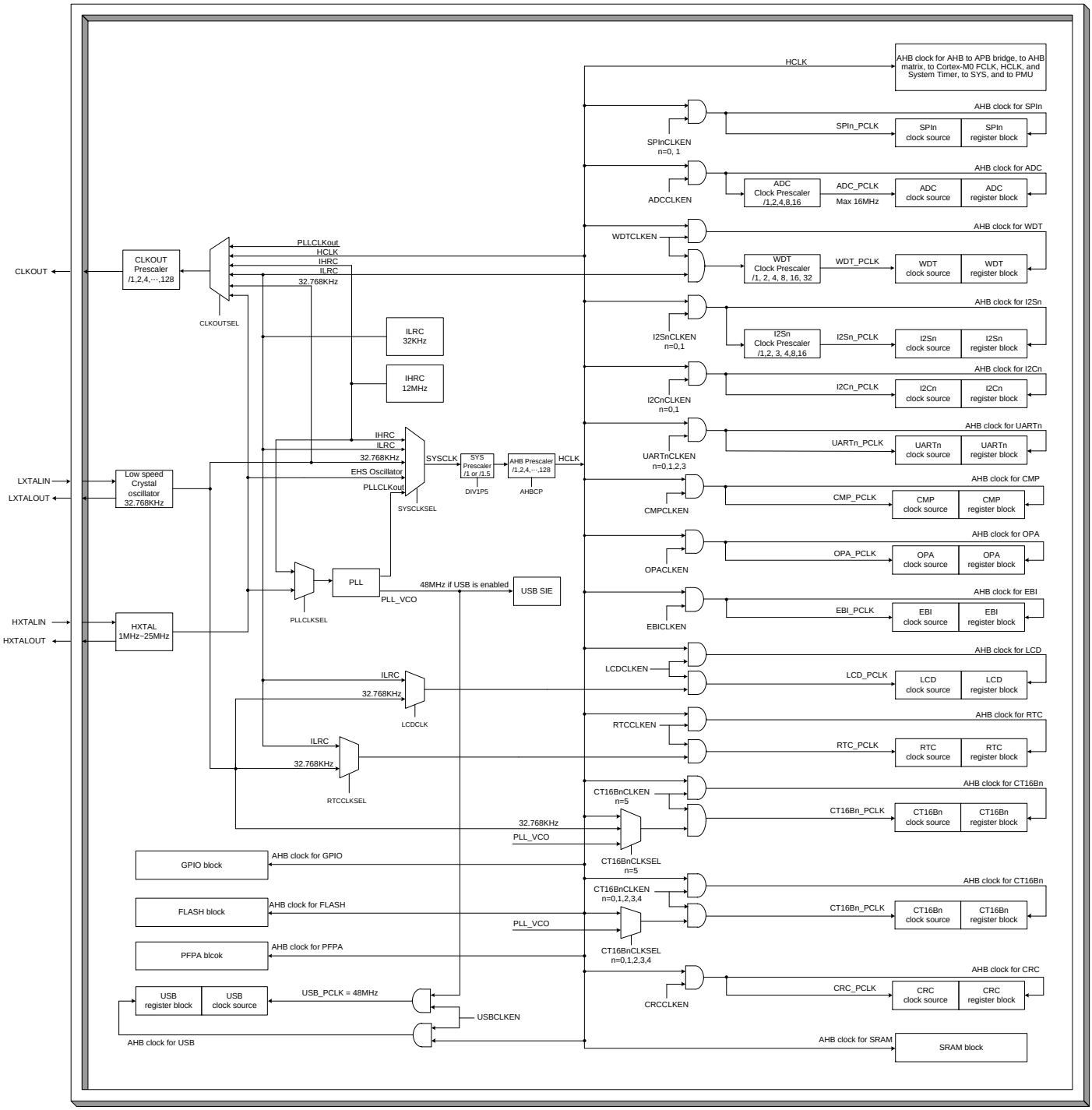
☞ **Features Selection Table**

Chip	ROM	RAM	F_{CPU} (Max MHz)	USB	16-Bit Timer	UART	SPI	I2C	I2S	PWM	12-bit ADC	CMP	OPA	LCD	EBI	GPIO	Package
SN32F299F	256KB	32KB	48	V	6	4	2	2	2	28+8	16+3	3	2	4x40 6x38 7x37 8x36	V	74	LQFP80
SN32F298F	256KB	32KB	48	V	6	4	2	2	2	28+8	16+3	3	2	4x35 6x33 7x32 8x31	V	58	LQFP64
SN32F297F	256KB	32KB	48	V	6	4	2	2	2	28+8	10+3	3	2	4x21	V	42	LQFP48

1.2 SYSTEM BLOCK DIAGRAM

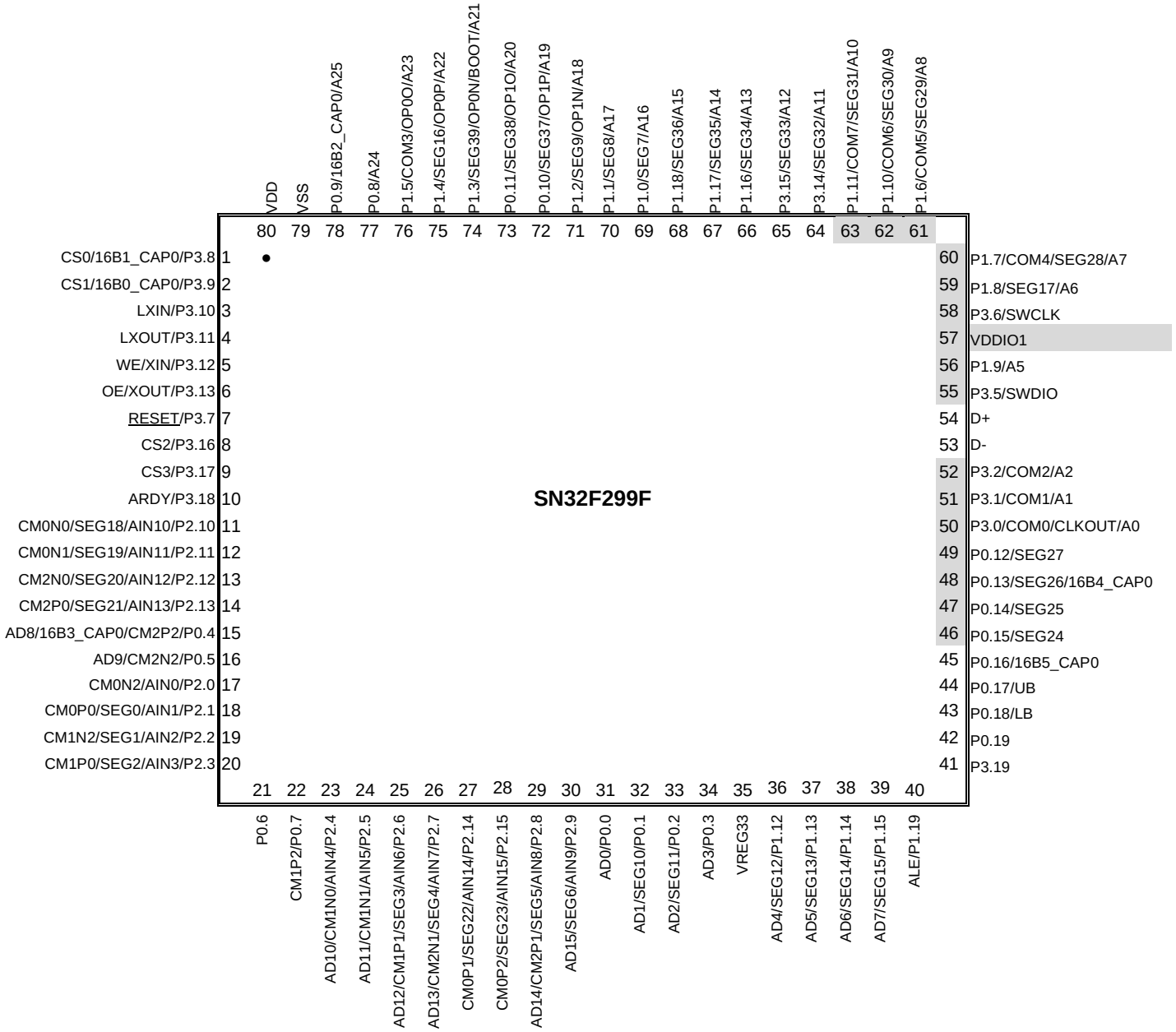


1.3 CLOCK GENERATION BLOCK DIAGRAM



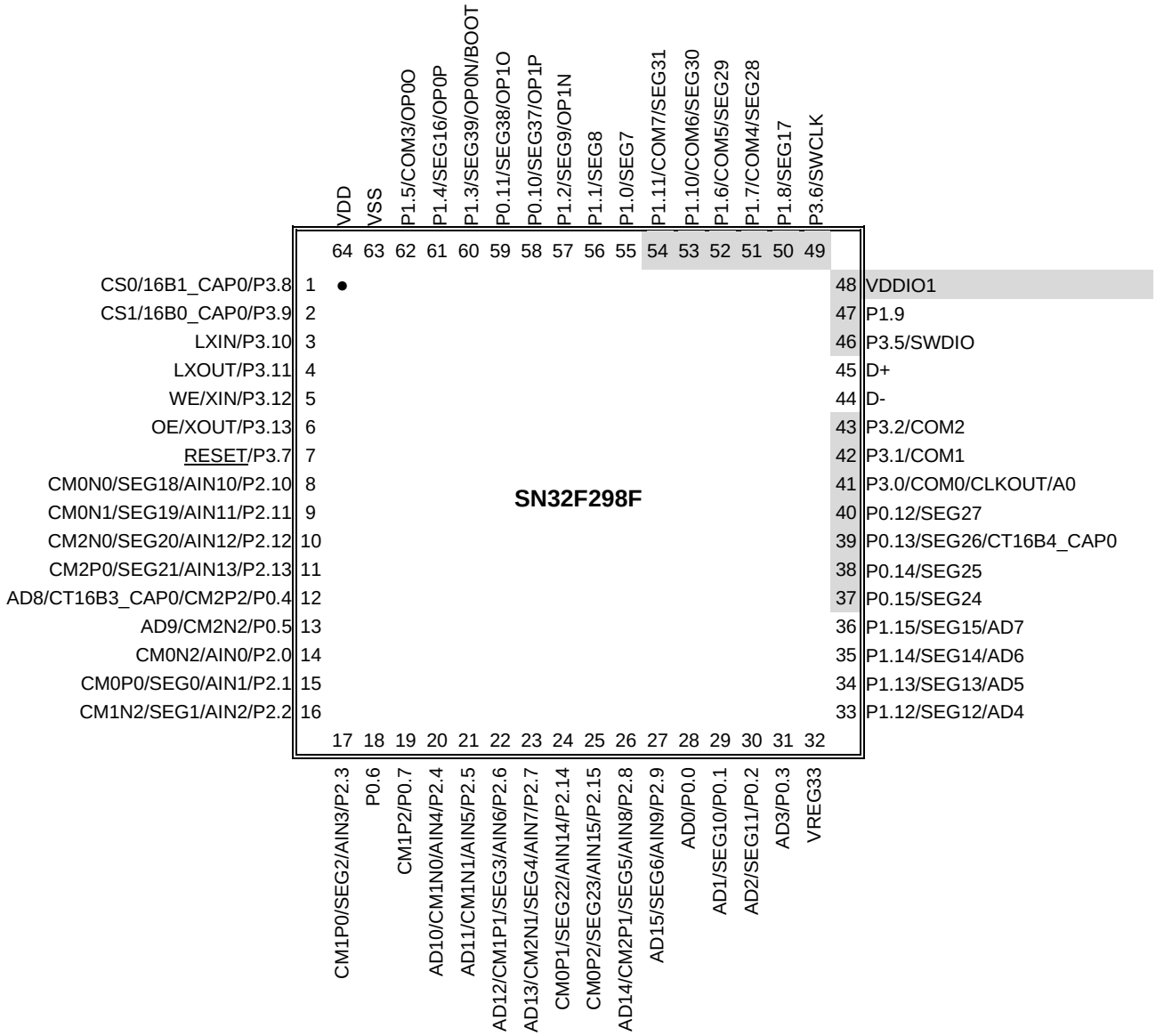
1.4 PIN ASSIGNMENT

SN32F299F (LQFP 80 pins)



✸ ***Note: SONiX provide Boot loader to check the status of P1.3 (BOOT pin) during boot procedure. If BOOT pin is Low during Boot procedure, MCU will execute code in Boot loader instead of User code. We strongly recommended NOT using BOOT pin as output pin to drive the LED, otherwise, the BOOT pin status may be low during boot procedure.***

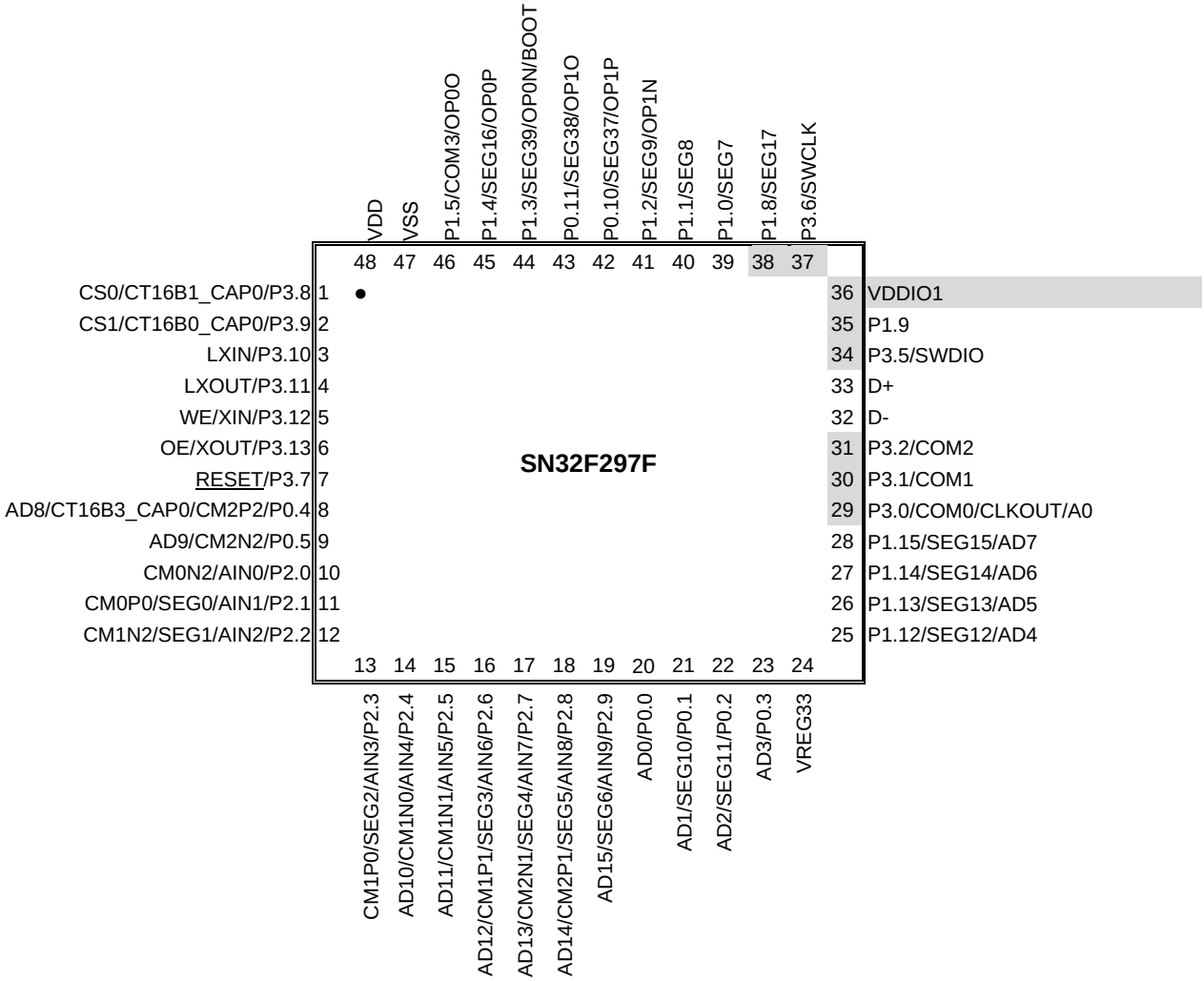
SN32F298F (LQFP 64 pins)



✸ ***Note: 1. The pins which are not pin-out shall be set correctly to decrease power consumption in low-power modes.*** **Strongly recommended to set these pins as input pull-up.**

2. SONiX provide Boot loader to check the status of P1.3 (BOOT pin) during boot procedure. If BOOT pin is Low during Boot procedure, MCU will execute code in Boot loader instead of User code. We strongly recommended NOT using BOOT pin as output pin to drive the LED, otherwise, the BOOT pin status may be low during boot procedure.

SN32F297F (LQFP 48 pins)



✷ ***Note: 1. The pins which are not pin-out shall be set correctly to decrease power consumption in low-power modes.*** **Strongly recommended to set these pins as input pull-up.**

2. SONiX provide Boot loader to check the status of P1.3 (BOOT pin) during boot procedure. If BOOT pin is Low during Boot procedure, MCU will execute code in Boot loader instead of User code. We strongly recommended NOT using BOOT pin as output pin to drive the LED, otherwise, the BOOT pin status may be low during boot procedure.

1.5 PIN ALLOCATION TABLE

I/O	UART	SPI	I2C	I2S	CT16	ADC	CMP	OPA	LCD	EBI	Other
P0.0		SCK0			B0_PWM1N B0_PWM2 B0_PWM3N B1_PWM0 B2_PWM0					AD0	
P0.1	UTXD2	SEL0 SCK1	SCL1	BCLK1	B0_PWM1 B0_PWM2N B0_PWM3 B1_ PWM1 B2_PWM2				SEG10	AD1	
P0.2	URXD2	MISO0	SDA1		B0_PWM0 B0_PWM3N B1_ PWM2 B2_PWM3				SEG11	AD2	
P0.3		MOSI0			B0_PWM0N B0_PWM3 B1_ PWM3 B2_PWM1		CM2O			AD3	
P0.4					B1_PWM4 B3_CAP0		CM2P2			AD8	
P0.5					B1_PWM5		CM2N2			AD9	
P0.6			SCL0		B1_PWM6						
P0.7			SDA0		B1_PWM7		CM1P2				
P0.8					B1_PWM8 B3_PWM1N B4_PWM0N					A24	
P0.9					B1_PWM9 B2_CAP0 B4_PWM0					A25	
P0.10	UTXD0		SCL0		B1_PWM10 B3_PWM0N B4_PWM0 B4_PWM1N			OP1P	SEG37	A19	
P0.11	URXD0		SDA0		B1_PWM11 B3_PWM1N B4_PWM0N			OP1O	SEG38	A20	
P0.12		SCK1			B0_PWM0N B5_PWM3		CM2O		SEG27		
P0.13		SEL1			B4_CAP0 B5_PWM2				SEG26		
P0.14					B5_PWM1				SEG25		
P0.15					B5_PWM0				SEG24		
P0.16					B5_CAP0						
P0.17										UB	
P0.18										LB	
P0.19											
P1.0		SCK0		BCLK0	B2_PWM1 B5_PWM2				SEG7	A16	
P1.1		MISO0	SCL0	MCLK0 DIN1	B5_PWM0				SEG8	A17	
P1.2		MOSI0	SDA0	DOUT0 DOUT1	B4_PWM0N B5_PWM1			OP1N	SEG9	A18	

P1.3	URXD2			DIN0	B3_PWM0N B4_PWM1N			OP0N	SEG39	A21	BOOT
I/O	**UART**	**SPI**	**I2C**	**I2S**	**CT16**	**ADC**	**CMP**	**OPA**	**LCD**	**EBI**	**Other**
P1.4	UTXD2		SCL0		B3_PWM0 B4_PWM1			OP0P	SEG16	A22	
P1.5		SEL1	SDA0	WS1	B3_PWM1 B4_PWM0			OP0O	COM3	A23	
P1.6	URXD2 URXD3			BCLK1	B2_PWM2				COM5 SEG29	A8	
P1.7	UTXD2 UTXD3	SEL0		MCLK1	B2_PWM1				COM4 SEG28	A7	
P1.8	URXD1	SEL0 SCK1	SCL1	WS0	B1_PWM0 B2_PWM0				SEG17	A6	
P1.9	UTXD1	SEL1	SDA1	WS1	B1_PWM1					A5	
P1.10		MISO1	SCL1	DIN1	B1_PWM2 B2_PWM3				COM6S30	A9	
P1.11		MOSI1	SDA1		B1_PWM3				COM7S31	A10	
P1.12		SEL1		WS1	B0_PWM0 B1_PWM4 B3_PWM1 B4_PWM1				SEG12	AD4	
P1.13		SCK1	SCL1	BCLK1	B0_PWM0N B1_PWM5 B3_PWM1N B4_PWM1N				SEG13	AD5	
P1.14		MISO1	SDA1	MCLK1	B0_PWM1N B1_PWM6 B3_PWM0				SEG14	AD6	
P1.15		MOSI1		DOUT1	B0_PWM2N B1_PWM7 B3_PWM0N B3_PWM1				SEG15	AD7	
P1.16	UTXD1								SEG34	A13	
P1.17	UTRD1				B2_PWM3				SEG35	A14	
P1.18					B2_PWM2 B5_PWM3				SEG36	A15	
P1.19				DIN1						ALE	
P2.0	UTXD3 URXD0				B1_PWM8 B2_PWM0	AIN0/ AVREF	CM0N2 CM0O				
P2.1	URXD3 UTXD0				B2_PWM1 B3_PWM0N	AIN1	CM0P0		SEG0		
P2.2	UTXD1				B2_PWM2 B3_PWM0	AIN2	CM1N2 CM1O		SEG1		
P2.3	URXD1				B2_PWM3 B3_PWM1	AIN3	CM1P0		SEG2		
P2.4		SEL0		WS0	B0_PWM1N B1_PWM9 B3_PWM1N B4_PWM1N	AIN4	CM1N0			AD10	
P2.5		SCK0		BCLK0	B0_PWM1 B2_PWM0 B4_PWM1	AIN5	CM1N1			AD11	
P2.6		MISO0		MCLK0	B0_PWM0 B0_PWM2N B3_PWM0 B4_PWM0N B4_PWM1 B5_PWM0	AIN6	CM0O CM1P1		SEG3	AD12	

P2.7		MOSI0		DOUT0	B0_PWM0N B0_PWM2 B1_PWM10 B4_PWM0 B5_PWM1	AIN7	CM1O CM2N1		SEG4	AD13	
I/O	**UART**	**SPI**	**I2C**	**I2S**	**CT16**	**ADC**	**CMP**	**OPA**	**LCD**	**EBI**	**Other**
P2.8				DIN0	B0_PWM1N B0_PWM2 B5_PWM2	AIN8	CM2P1		SEG5	AD14	
P2.9					B0_PWM1 B0_PWM2N B1_PWM11 B5_PWM3	AIN9			SEG6	AD15	
P2.10						AIN10	CM0N0		SEG18		
P2.11						AIN11	CM0N1		SEG19		
P2.12		MISO1		MCLK1		AIN12	CM2N0		SEG20		
P2.13		MOSI1		DOUT1		AIN13	CM2P0		SEG21		
P2.14	UTXD2				B0_PWM3	AIN14	CM0P1		SEG22		
P2.15	URXD2				B0_PWM3N	AIN15	CM0P2		SEG23		
P3.0		SCK0		MCLK0	B0_PWM0				COM0	A0	CLKOUT
P3.1	UTXD0	MISO0		BCLK0	B0_PWM1				COM1	A1	
P3.2	URXD0	MOSI0		WS0	B0_PWM2				COM2	A2	
P3.5											SWDIO
P3.6	UTXD1										SWCLK
P3.7											RESET
P3.8					B1_CAP0		CM2O			CS0	
P3.9					B0_CAP0					CS1	
P3.10											LXIN
P3.11											LXOUT
P3.12	UTXD3									WE	XIN
P3.13	URXD3									OE	XOUT
P3.14		MISO1		MCLK1					SEG32	A11	
P3.15		MOSI1		DOUT1					SEG33		
P3.16				WS1	B5_PWM0					CS2	
P3.17				BCLK1	B5_PWM1					CS3	
P3.18				DIN1	B5_PWM2					ARDY	
P3.19					B5_PWM3						

1.6 PIN DESCRIPTIONS

Pad NAME	TYPE	DESCRIPTION
VDD, VSS	P	Power supply input pins for digital circuit.
VDDIO1	P	I/O and LCD driver power input pins for P0.12~P0.15, P3.0~P3.2, P3.5~P3.6, P1.6~P1.11. VDDIO1 voltage shall be less and equal to VLCD if VLCD is enabled. This power input shall not be floating.
VREG33	O	3.3V voltage output from USB 3.3V regulator.
D+/PSCLK	I/O	**D+ —** USB differential signal line.
		PSCLK — PS/2's clock pin with internal 5K pull-up resistor.
D-/PSDATA	I/O	**D- —**USB differential signal line.
		PSDATA —PS/2's data pin with internal 5K pull-up resistor.
P0.0/AD0	I/O	**P0.0 —** General purpose digital input/output pin.
		AD0 — Address/Data 0 for EBI.
P0.1/SEG10/AD1	I/O	**P0.1 —** General purpose digital input/output pin.
		AD1 — Address/Data 1 for EBI.
	O	**SEG10 —** Segment output 10 for LCD driver.
P0.2/SEG11/AD2	I/O	**P0.2 —** General purpose digital input/output pin.
		AD2 — Address/Data 2 for EBI.
	O	**SEG11 —** Segment output 11 for LCD driver.
P0.3/AD3	I/O	**P0.3 —** General purpose digital input/output pin.
		AD3 — Address/Data 3 for EBI.
P0.4/CM2P2/AD8	I/O	**P0.4 —** General purpose digital input/output pin.
		AD8 — Address/Data 8 for EBI.
	I	**CM2P2 —** Positive input pin 2 of comparator 2.
P0.5/CM2N2/AD9	I/O	**P0.5 —** General purpose digital input/output pin.
		AD9 — Address/Data 9 for EBI.
	I	**CM2N2 —** Negative input pin 2 of comparator 2.
P0.6	I/O	**P0.6 —** General purpose digital input/output pin.
P0.7/CM1P2	I/O	**P0.7 —** General purpose digital input/output pin.
	I	**CM1P2 —** Positive input pin 2 of comparator 1.
P0.8/A24	I/O	**P0.8 —** General purpose digital input/output pin.
	O	**A24 —** Address 24 for EBI.

P0.9/CT16B2_CAP0/A25	I/O	**P0.9 —** General purpose digital input/output pin.
	I	**CT16B2_CAP0 —** Capture input 0 for CT16B2.
	O	**A25 —** Address 24 for EBI.
P0.10/SEG37/OP1P/A19	I/O	**P0.10 —** General purpose digital input/output pin.
	I	**OP1P —** Positive input pin of OPA 1.
	O	**SEG37 —** Segment output 37 for LCD driver.
		A19 — Address 19 for EBI.
P0.11/SEG38/OP1O/A20	I/O	**P0.11 —** General purpose digital input/output pin.
	O	**SEG38 —** Segment output 38 for LCD driver.
		A20 — Address 20 for EBI.
		OP1O — Output of OPA1
P0.12/SEG27	I/O	**P0.12 —** General purpose digital input/output pin.
	O	**SEG27 —** Segment output 27 for LCD driver.
P0.13/SEG26/CT16B4_CAP0	I/O	**P0.13 —** General purpose digital input/output pin.
	O	**SEG26 —** Segment output 26 for LCD driver.
	I	**CT16B4_CAP0 —** Capture input 0 for CT16B4.
P0.14/SEG25	I/O	**P0.14 —** General purpose digital input/output pin.
	O	**SEG25 —** Segment output 25 for LCD driver.
P0.15/SEG24	I/O	**P0.15 —** General purpose digital input/output pin.
	O	**SEG24 —** Segment output 24 for LCD driver.
P0.16/CT16B5_CAP0	I/O	**P0.16 —** General purpose digital input/output pin.
	I	**CT16B5_CAP0 —** Capture input 0 for CT16B5.
P0.17/UB	I/O	**P0.17 —** General purpose digital input/output pin.
	O	**UB —** Upper Byte output pin for EBI.
P0.18/LB	I/O	**P0.18 —** General purpose digital input/output pin.
	O	**LB —** Lower Byte output pin for EBI.
P0.19	I/O	**P0.19 —** General purpose digital input/output pin.
P1.0/SEG7/A16	I/O	**P1.0 —** General purpose digital input/output pin.
	O	**SEG7 —** Segment 7 output for LCD.
		A16 — Address 16 for EBI.
P1.1/SEG8/A17	I/O	**P1.1 —** General purpose digital input/output pin.

	O	**SEG8 —** Segment 8 output for LCD.
		A17 — Address 17 for EBI.
P1.2/SEG9/OP1N/A18	I/O	**P1.2 —** General purpose digital input/output pin.
	I	**OP1N —** Negative input pin of OPA 1.
	O	**SEG9 —** Segment 9 output for LCD.
		A18 — Address 18 for EBI.
P1.3/SEG39/OP0N/A21/BOOT	I/O	**P1.3 —** General purpose digital input/output pin.
	I	**OP0N —** Negative input pin of OPA 0.
	O	**SEG39 —** Segment 39 output for LCD.
		A21 — Address 21 for EBI.
	I	**BOOT —** Boot loader check pin. Internal pull-up in Boot loader, tie LOW to keep in Boot loader or left HIGH to exit Boot loader and execute User program at boot time.
P1.4/SEG16/OP0P/A22	I/O	**P1.4 —** General purpose digital input/output pin.
	I	**OP0P —** Positive input pin of OPA 0.
	O	**SEG16 —** Segment 16 output for LCD.
		A22 — Address 22 for EBI.
P1.5/COM3/OP0O/A23	I/O	**P1.5 —** General purpose digital input/output pin.
	O	**COM3 —** COM3 output for LCD.
		OP0O — Output of OPA0.
		A23 — Address 23 for EBI.
P1.6/COM5/SEG29/A8	I/O	**P1.6 —** General purpose digital input/output pin.
	O	**COM5 —** COM5 output for LCD.
		SEG29 — Segment 29 output for LCD.
		A8 — Address 8 for EBI.
P1.7/COM4/SEG28/A7	I/O	**P1.7 —** General purpose digital input/output pin.
	O	**COM4 —** COM4 output for LCD.
		SEG28 — Segment 28 output for LCD.
		A7 — Address 7 for EBI.
P1.8/SEG17/A6	I/O	**P1.8 —** General purpose digital input/output pin.
	O	**SEG17 —** Segment 17 output for LCD.
		A6 — Address 6 for EBI.

P1.9/A5	I/O	**P1.9 —** General purpose digital input/output pin.
	O	**A5 —** Address 5 for EBI.
P1.10/COM6/SEG30/A9	I/O	**P1.10 —** General purpose digital input/output pin.
	O	**COM6 —** COM6 output for LCD.
		SEG30 — Segment 30 output for LCD.
		A9 — Address 2 for EBI.
P1.11/COM7/SEG31/A10	I/O	**P1.11 —** General purpose digital input/output pin.
	O	**COM7 —** COM7 output for LCD.
		SEG31 — Segment 31 output for LCD.
		A10 — Address 10 for EBI.
P1.12/SEG12/AD4	I/O	**P1.12 —** General purpose digital input/output pin.
		AD4 — Address/Data 4 for EBI.
	O	**SEG12 —** Segment 12 output for LCD.
P1.13/SEG13/AD5	I/O	**P1.13 —** General purpose digital input/output pin.
		AD5 — Address/Data 5 for EBI.
	O	**SEG13 —** Segment 13 output for LCD.
P1.14/SEG14/AD6	I/O	**P1.14 —** General purpose digital input/output pin.
		AD6 — Address/Data 6 for EBI.
	O	**SEG14 —** Segment 14 output for LCD.
P1.15/SEG15/AD7	I/O	**P1.15 —** General purpose digital input/output pin.
		AD7 — Address/Data 7 for EBI.
	O	**SEG15 —** Segment 15 output for LCD.
P1.16/SEG34/A13	I/O	**P1.16 —** General purpose digital input/output pin.
	O	**SEG34 —** Segment 34 output for LCD.
		A13 — Address 13 for EBI.
P1.17/SEG35/A14	I/O	**P1.17 —** General purpose digital input/output pin.
	O	**SEG35 —** Segment 35 output for LCD.
		A14 — Address 14 for EBI.
P1.18/SEG36/A15	I/O	**P1.18 —** General purpose digital input/output pin.
	O	**SEG36 —** Segment 36 output for LCD.
		A15 — Address 15 for EBI.

P1.19/ALE	I/O	**P1.19 —** General purpose digital input/output pin.
	O	**ALE —** Address Latch output for EBI.
P2.0/AIN0/CM0N2	I/O	**P2.0 —** General purpose digital input/output pin.
	I	**AIN0 —** ADC channel input 0.
		CM0N2 — Negative input pin 2 of comparator 0.
P2.1/AIN1/SEG0/CM0P0	I/O	**P2.1 —** General purpose digital input/output pin.
	I	**AIN1 —** ADC channel input 1.
		CM0P0 — Positive input pin 0 of comparator 0.
	O	**SEG0 —** Segment 0 output for LCD.
P2.2/AIN2/SEG1/CM1N2	I/O	**P2.2 —** General purpose digital input/output pin.
	I	**AIN2 —** ADC channel input 2.
		CM1N2 — Negative input pin 2 of comparator 1.
	O	**SEG1 —** Segment 1 output for LCD.
P2.3/AIN3/SEG2/CM1P0	I/O	**P2.3 —** General purpose digital input/output pin.
	I	**AIN3 —** ADC channel input 3.
		CM1P0 — Positive input pin 0 of comparator 1.
	O	**SEG2 —** Segment 2 output for LCD.
P2.4/AIN4/CM1N0/AD10	I/O	**P2.4 —** General purpose digital input/output pin.
		AD10 — Address/Data 10 for EBI.
	I	**AIN4 —** ADC channel input 4.
		CM1N0 — Negative input pin 0 of comparator 1.
P2.5/AIN5/CM1N1/AD11	I/O	**P2.5 —** General purpose digital input/output pin.
		AD11 — Address/Data 11 for EBI.
	I	**AIN5 —** ADC channel input 5.
		CM1N1 — Negative input pin 1 of comparator 1.
P2.6/AIN6/SEG3/CM1P1/AD12	I/O	**P2.6 —** General purpose digital input/output pin.
		AD12 — Address/Data 12 for EBI.
	I	**AIN6 —** ADC channel input 6.
		CM1P1 — Positive input pin 1 of comparator 1.
	O	**SEG3 —** Segment 3 output for LCD.
	I/O	**P2.7 —** General purpose digital input/output pin.

P2.7/AIN7/SEG4/CM2N1/AD13		**AD13 —** Address/Data 13 for EBI.
	I	**AIN7 —** ADC channel input 7.
		CM2N1 — Negative input pin 1 of comparator 2.
	O	**SEG4 —** Segment 4 output for LCD.
P2.8/AIN8/SEG5/CM2P1/AD14	I/O	**P2.8 —** General purpose digital input/output pin.
		AD14 — Address/Data 14 for EBI.
	I	**AIN8 —** ADC channel input 8.
		CM2P1 — Positive input pin 1 of comparator 2.
	O	**SEG5 —** Segment 5 output for LCD.
P2.9/AIN9/SEG6/AD15	I/O	**P2.9 —** General purpose digital input/output pin.
		AD15 — Address/Data 15 for EBI.
	I	**AIN9 —** ADC channel input 9.
	O	**SEG6 —** Segment 6 output for LCD.
P2.10/AIN10/SEG18/CM0N0	I/O	**P2.10 —** General purpose digital input/output pin.
	I	**AIN10 —** ADC channel input 10.
		CM0N0 — Negative input pin 0 of comparator 0.
	O	**SEG18 —** Segment 18 output for LCD.
P2.11/AIN11/SEG19/CM0N1	I/O	**P2.11 —** General purpose digital input/output pin.
	I	**AIN11 —** ADC channel input 11.
		CM0N1 — Negative input pin 1 of comparator 0.
	O	**SEG19 —** Segment 19 output for LCD.
P2.12/AIN12/SEG20/CM2N0	I/O	**P2.12 —** General purpose digital input/output pin.
	I	**AIN12 —** ADC channel input 12.
		CM2N0 — Negative input pin 0 of comparator 1.
	O	**SEG20 —** Segment 20 output for LCD.
P2.13/AIN13/SEG21/CM2P0	I/O	**P2.13 —** General purpose digital input/output pin.
	I	**AIN13 —** ADC channel input 13.
		CM2P0 — Positive input pin 0 of comparator 2.
	O	**SEG21 —** Segment 21 output for LCD.
P2.14/AIN14/SEG22/CM0P1	I/O	**P2.14 —** General purpose digital input/output pin.
	I	**AIN14 —** ADC channel input 14.

		CM0P1 — Positive input pin 1 of comparator 0.
	O	**SEG22 —** Segment 22 output for LCD.
P2.15/AIN15/SEG23/CM0P2	I/O	**P2.15 —** General purpose digital input/output pin.
	I	**AIN15 —** ADC channel input 15.
		CM0P2 — Positive input pin 2 of comparator 0.
	O	**SEG23 —** Segment 23 output for LCD.
P3.0/COM0/A0/CLKOUT	I/O	**P3.0 —** General purpose digital input/output pin.
	O	**COM0 —** COM0 output for LCD.
		CLKOUT — Clockout pin
		A0 — Address 0 for EBI.
P3.1/COM1/A1	I/O	**P3.1 —** General purpose digital input/output pin.
	O	**COM1 —** COM1 output for LCD.
		A1 — Address 1 for EBI.
P3.2/COM2/A2	I/O	**P3.2 —** General purpose digital input/output pin.
	O	**COM2 —** COM2 output for LCD.
		A2 — Address 2 for EBI.
	O	**A4 —** Address 4 for EBI.
P3.5/SWDIO	I/O	**P3.5 —** General purpose digital input/output pin.
		SWDIO — Serial wire debug input/output.
P3.6/SWCLK	I/O	**P3.6 —** General purpose digital input/output pin.
	I	**SWCLK —** Serial wire clock.
P3.7/RESET	I/O	**P3.7 —** General purpose digital input/output pin.
	I	**RESET —** External Reset input.
P3.8/CT16B1_CAP0/CS0	I/O	**P3.8 —** General purpose digital input/output pin.
	I	**CT16B1_CAP0 —** Capture input 0 for CT16B1.
	O	**CS0 —** Chip Select 0 for EBI.
P3.9/CT16B0_CAP0/CS1	I/O	**P3.9 —** General purpose digital input/output pin.
	I	**CT16B0_CAP0 —** Capture input 0 for CT16B0.
	O	**CS1 —** Chip Select 0 for EBI.
P3.10/LXIN	I/O	**P3.10 —** General purpose digital input/output pin.
	I	**LXIN —** External low-speed X'tal input pin.

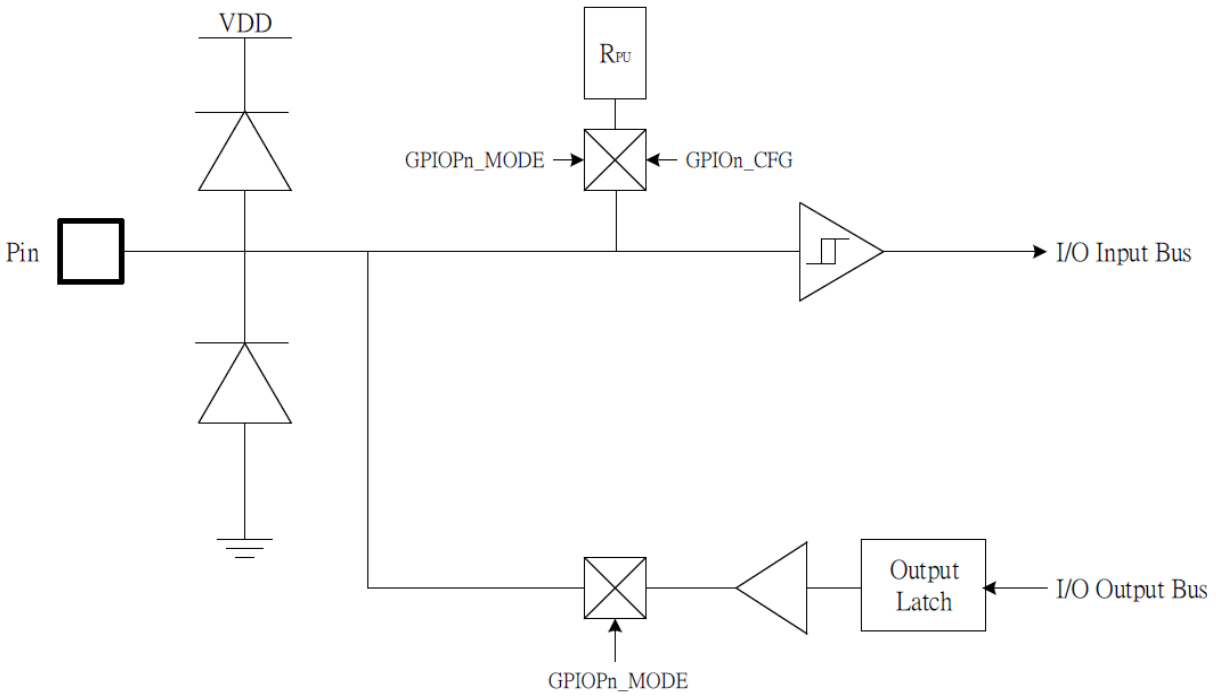
P3.11/LXOUT	I/O	**P3.11 —** General purpose digital input/output pin.
	O	**LXOUT —** External low-speed X'tal output pin.
P3.12/XIN/WE	I/O	**P3.12 —** General purpose digital input/output pin.
	I	**XIN —** External high-speed X'tal input pin.
	O	**WE —** Write enable pin of EBI.
P3.13/XOUT/OE	I/O	**P3.13 —** General purpose digital input/output pin.
	O	**XOUT —** External high-speed X'tal output pin.
		OE — Output enable pin of EBI.
P3.14/SEG32/A11	I/O	**P3.14 —** General purpose digital input/output pin.
	O	**SEG32 —** Segment 32 output for LCD.
		A11 — Address 11 for EBI.
P3.15/SEG33/A12	I/O	**P3.15 —** General purpose digital input/output pin.
	O	**SEG33 —** Segment 33 output for LCD.
		A12 — Address 12 for EBI.
P3.16/CS2	I/O	**P3.16 —** General purpose digital input/output pin.
	O	**CS2 —** Chip Select 2 for EBI.
P3.17/CS3	I/O	**P3.17 —** General purpose digital input/output pin.
	O	**CS3 —** Chip Select 3 for EBI.
P3.18/ARDY	I/O	**P3.18 —** General purpose digital input/output pin.
	I	**ARDY —** Ready/Busy pin of EBI.
P3.19	I/O	**P3.19 —** General purpose digital input/output pin.

Please refer to Peripheral Function Pin Assignment (PFPA) chapters for setting of each GPIOs.

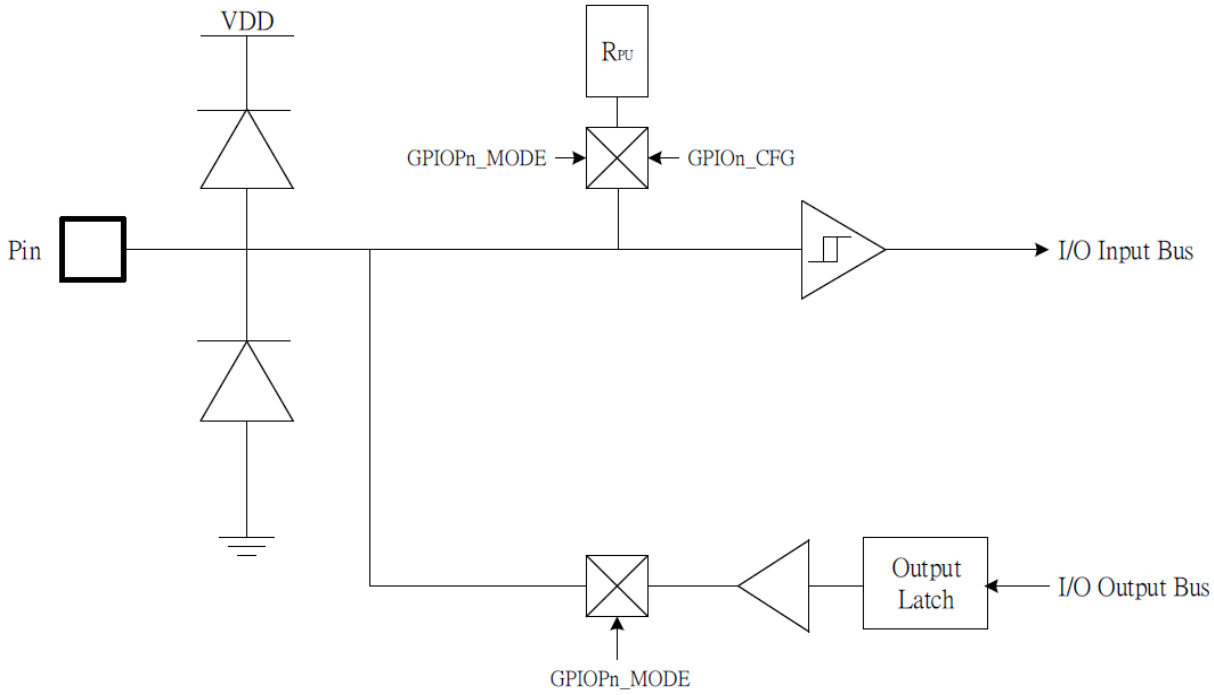
✷ ***Note: VDDIO1 is the I/O and LCD driver power input pin for P1.6~P1.15 and P3.0~P3.9. The voltage shall be less and equal to VLCD if VLCD is enabled. This power input shall not be floating.***

1.7 PIN CIRCUIT DIAGRAMS

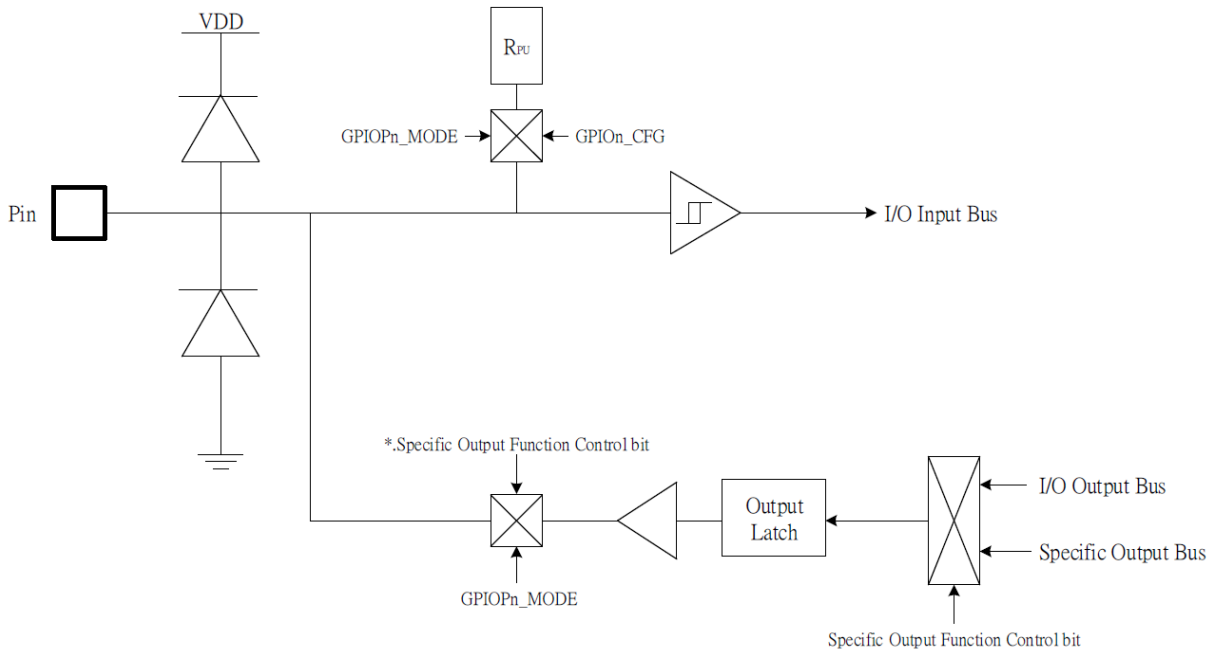
- **Normal Bi-direction I/O Pin.**



- **Bi-direction I/O Pin Shared with Specific Digital Input Function, e.g. SPI, I2C…**

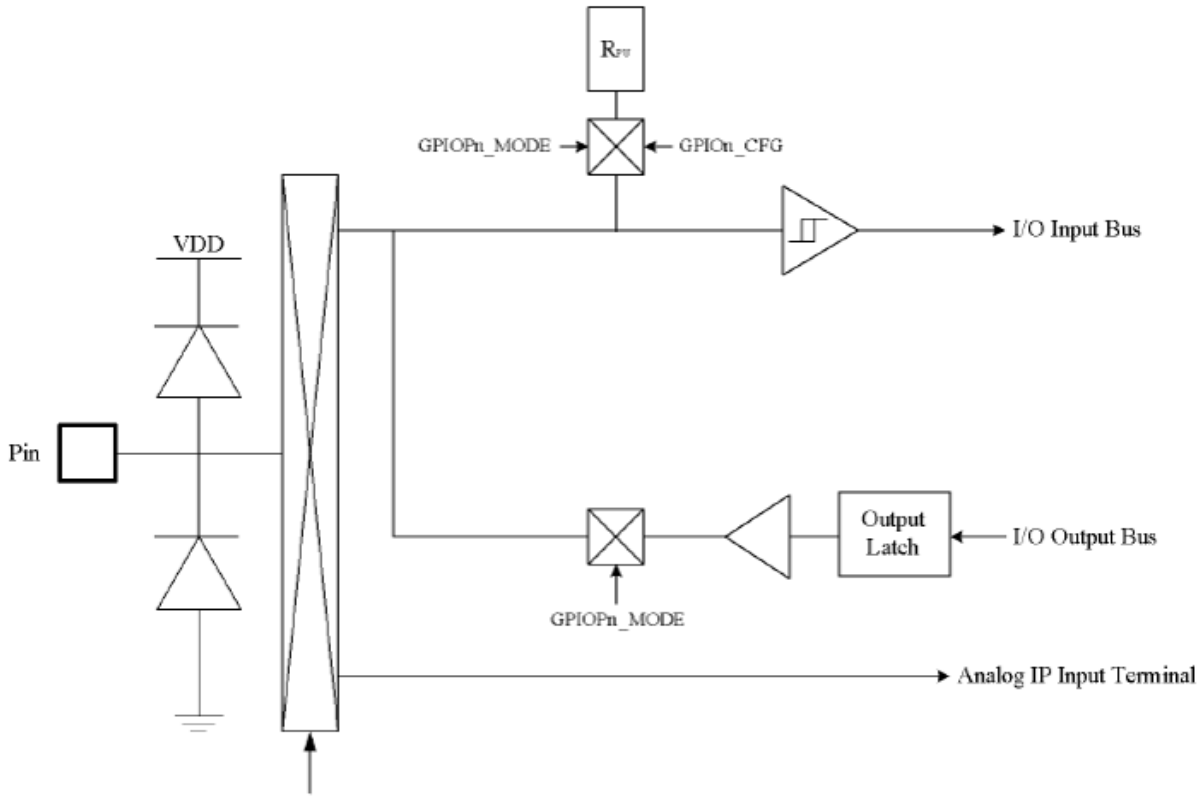


- **Bi-direction I/O Pin Shared with Specific Digital Output Function, e.g. SPI, I2C…**



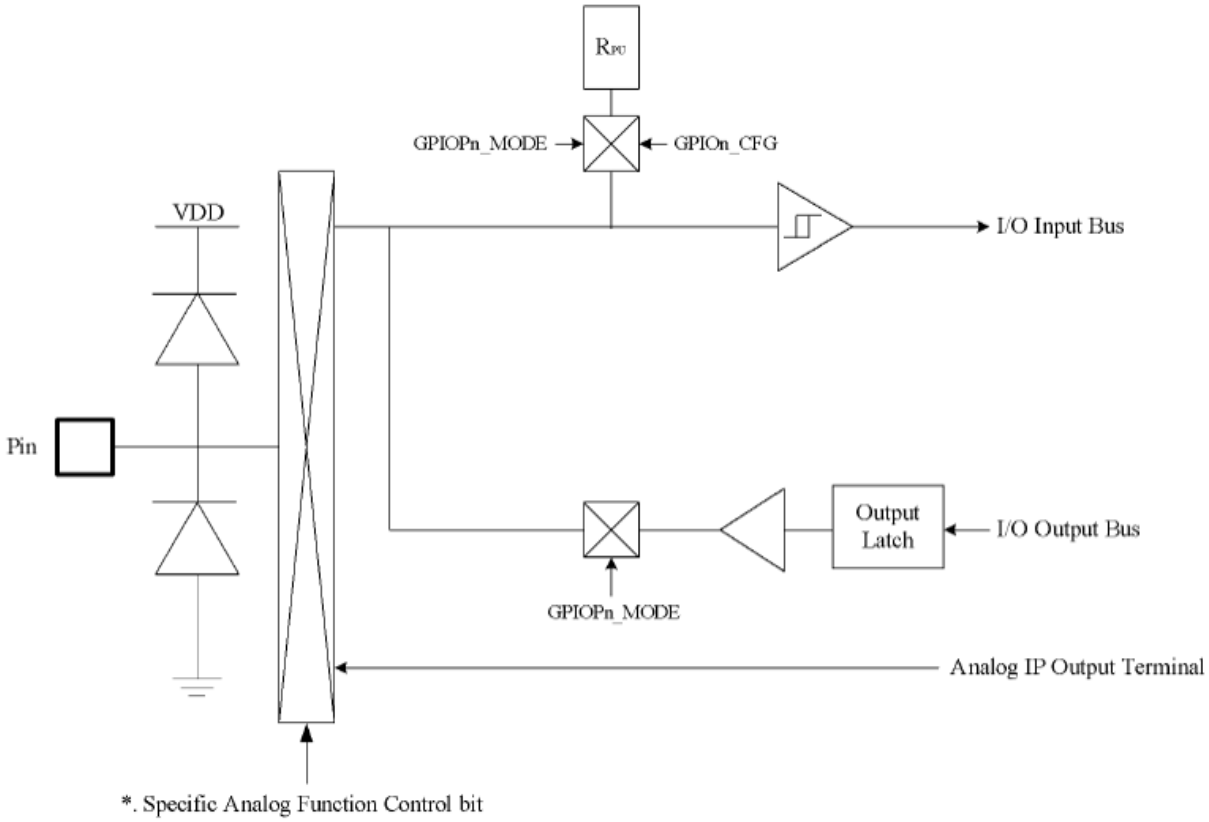
*. Some specific functions switch I/O direction directly, not through GPIOn_MODE register.

- **Bi-direction I/O Pin Shared with Specific Analog Input Function, e.g. XIN, ADC…**



*. Some specific functions switch I/O direction directly, not through GPIOn_MODE register.

- **Bi-direction I/O Pin Shared with Specific Analog Output Function, e.g. XOUT…**



***. Some specific functions switch I /O direction directly , not through GPIOn_MODE register.**

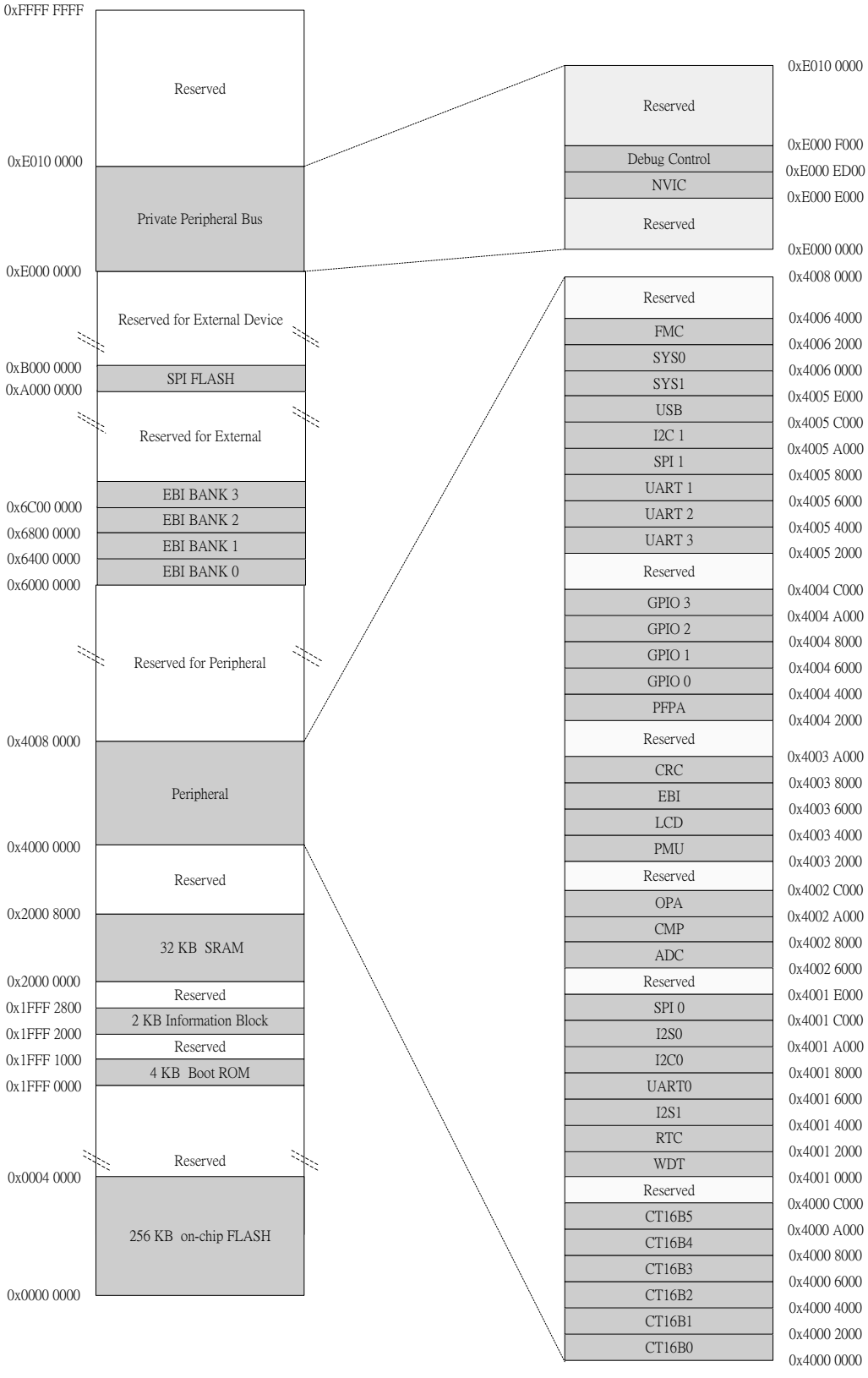
1.8 PIN CHARACTERISTICS

Port	Direction	ADC	CMP Input	OPA input/output	Open-Drain	Pull-up Resistor (75KΩ@3.3V)	Pull-down Resistor (75KΩ@3.3V)	Sink Current 100mA @VSS+1.5V	LCD
P0.0	I/O					V		V	
P0.1	I/O				V	V		V	V
P0.2	I/O				V	V		V	V
P0.3	I/O					V		V	
P0.4	I/O		V			V			
P0.5	I/O		V			V			
P0.6	I/O				V	V			
P0.7	I/O		V		V	V			
P0.8	I/O					V			
P0.9	I/O					V			
P0.10	I/O			V	V	V			V
P0.11	I/O			V	V	V			V
P0.12	I/O					V			V
P0.13	I/O					V			V
P0.14	I/O					V			V
P0.15	I/O					V			V
P0.16	I/O					V			
P0.17	I/O					V			
P0.18	I/O					V			
P0.19	I/O								
P1.0	I/O					V			V
P1.1	I/O				V	V			V
P1.2	I/O			V	V	V			V
P1.3	I/O			V		V			V
P1.4	I/O			V	V	V			V
P1.5	I/O			V	V	V			V
P1.6	I/O					V			V
P1.7	I/O					V			V
P1.8	I/O				V	V			V
P1.9	I/O				V	V			
P1.10	I/O				V	V			V
P1.11	I/O				V	V			V
P1.12	I/O					V		V	V
P1.13	I/O				V	V		V	V
P1.14	I/O				V	V			V
P1.15	I/O					V			V
P1.16	I/O					V			V
P1.17	I/O					V			V
P1.18	I/O					V			V
P1.19	I/O					V			
P2.0	I/O	V	V			V			
P2.1	I/O	V	V			V			V
P2.2	I/O	V	V			V			V
P2.3	I/O	V	V			V			V
P2.4	I/O	V	V			V			
P2.5	I/O	V	V			V			
P2.6	I/O	V	V			V			V
P2.7	I/O	V	V			V			V
P2.8	I/O	V	V			V			V
P2.9	I/O	V				V			V
P2.10	I/O	V	V			V			V
P2.11	I/O	V	V			V			V
P2.12	I/O	V	V			V			V
P2.13	I/O	V	V			V			V
P2.14	I/O	V	V			V			V
P2.15	I/O	V	V			V			V
P3.0	I/O					V			V
P3.1	I/O					V			V
P3.2	I/O					V			V

P3.5	I/O					V			
P3.6	I/O					V	V		
P3.7	I/O					V			
P3.8	I/O					V			
P3.9	I/O					V			
P3.10	I/O					V	V		
P3.11	I/O					V	V		
P3.12	I/O					V	V		
P3.13	I/O					V	V		
P3.14	I/O					V			V
P3.15	I/O					V			V
P3.16	I/O					V			
P3.17	I/O					V			
P3.18	I/O					V			
P3.19	I/O					V			

2 CENTRAL PROCESSOR UNIT (CPU)

2.1 MEMORY MAP



2.2 SYSTEM TICK TIMER

The SysTick timer is an integral part of the Cortex-M0. The SysTick timer is intended to generate a fixed 10-ms interrupt for use by an operating system or other system management software.

Since the SysTick timer is a part of the Cortex-M0, it facilitates porting of software by providing a standard timer that is available on Cortex-M0 based devices.

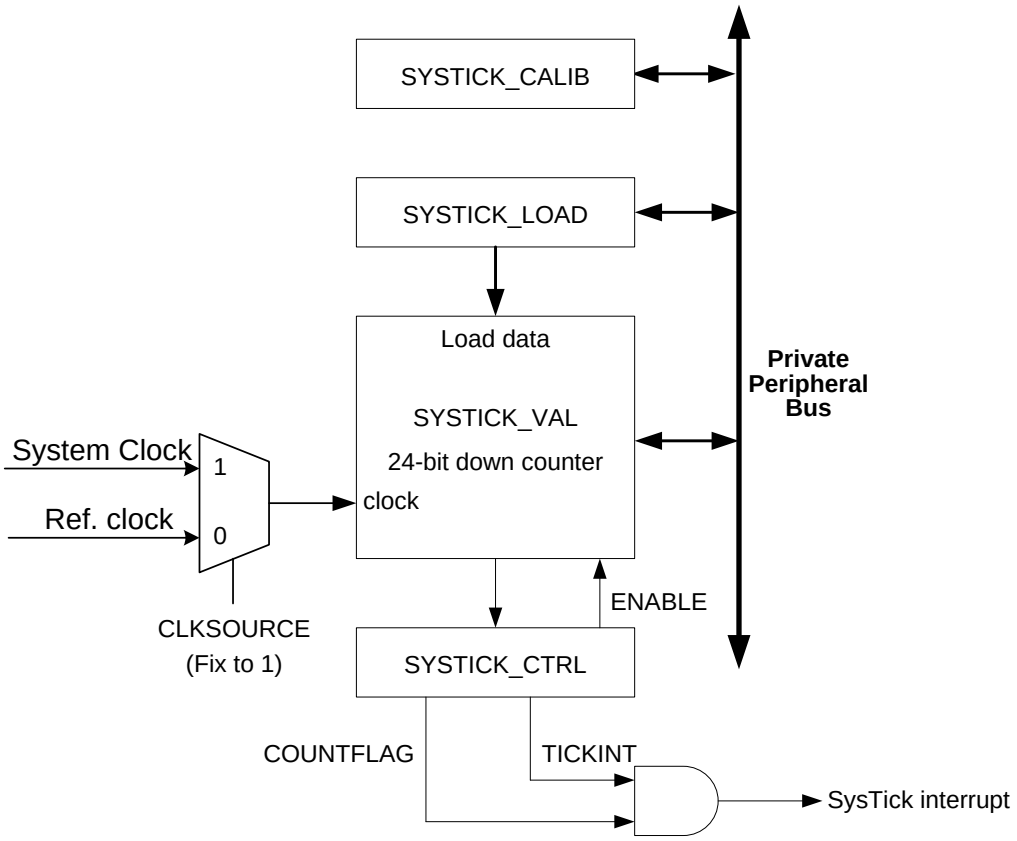
Refer to the *Cortex-M0 User Guide* for details.

2.2.1 OPERATION

The SysTick timer is a 24-bit timer that counts down to zero and generates an interrupt.

The intent is to provide a fixed 10-ms time interval between interrupts. The system tick timer is enabled through the SysTick control register. The system tick timer clock is fixed to the frequency of the system clock.

The block diagram of the SysTick timer:



When SysTick timer is enabled, the timer counts down from the current value (SYSTICK_VAL) to zero, reloads to the value in the SysTick Reload Value Register (SYSTICK_LOAD) on the next clock edge, then decrements on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set to 1. The COUNTFLAG bit clears on reads.

✸ ***Note: When the processor is halted for debugging the counter does not decrease.***

2.2.2 SYSTICK USAGE HINTS AND TIPS

The interrupt controller clock updates the SysTick counter. Some implementations stop this clock signal for low power mode. If this happens, the SysTick counter stops.

Ensure SW uses word accesses to access the SysTick registers.

The SysTick counter reload and current value are not initialized by HW. This means the correct initialization sequence for the SysTick counter is:

1. Program the reload value in SYSTICK_LOAD register.
2. Clear the current value by writing any value to SYSTICK_VAL register.
3. Program the Control and Status (SYSTICK_CTRL) register.

2.2.3 SYSTICK REGISTERS

2.2.3.1 System Tick Timer Control and Status register (SYSTICK_CTRL)

Address: 0xE000 E010 (Refer to Cortex-M0 Spec)

Bit	Name	Description	Attribute	Reset
31:17	Reserved		R	0
16	COUNTFLAG	This flag is set when the System Tick counter counts down to 0, and is cleared by reading this register.	R/W	0
15:3	Reserved		R	0
2	CLKSOURCE	Selects the SysTick timer clock source. 0: reference clock. 1: system clock. (Fixed)	R	1
1	TICKINT	System Tick interrupt enable. 0: Disable the System Tick interrupt 1: Enable the System Tick interrupt, the interrupt is generated when the System Tick counter counts down to 0.	R/W	0
0	ENABLE	System Tick counter enable. 0: Disable 1: Enable	R/W	0

2.2.3.2 System Tick Timer Reload value register (SYSTICK_LOAD)

Address: 0xE000 E014 (Refer to Cortex-M0 Spec)

The RELOAD register is set to the value that will be loaded into the SysTick timer whenever it counts down to zero. This register is set by software as part of timer initialization. The SYSTICK_CALIB register may be read and used as the value for RELOAD if the CPU or external clock is running at the frequency intended for use with the SYSTICK_CALIB value.

The following example illustrates selecting the SysTick timer reload value to obtain a 10 ms time interval with the system clock set to 50 MHz.

RELOAD = (system tick clock frequency × 10 ms) −1 = (50 MHz × 10 ms) −1
= 0x0007A11F.

Bit	Name	Description	Attribute	Reset
31:24	Reserved		R	0
23:0	RELOAD	Value to load into the SYSTICK_VAL when the counter is enabled and when it reaches 0.	R/W	0x5F7F9B

2.2.3.3 System Tick Timer Current Value register (SYSTICK_VAL)

Address: 0xE000 E018 (Refer to Cortex-M0 Spec)

Bit	Name	Description	Attribute	Reset
31:24	Reserved		R	0
23:0	CURRENT	Reading this register returns the current value of the System Tick counter. Writing any value clears the System Tick counter and the COUNTFLAG bit in SYSTICK_CTRL.	R/W	0x7E7F35

2.2.3.4 System Tick Timer Calibration Value register (SYSTICK_CALIB)

Address: 0xE000 E01C (Refer to Cortex-M0 Spec)

Bit	Name	Description	Attribute	Reset
31	NOREF	Indicates the reference clock to M0 is provided or not. 1: No reference clock provided.	R	1
30	SKEW	Indicates whether the TENMS value is exact, an inexact TENMS value can affect the suitability of SysTick as a software real time clock. 0: TENMS value is exact 1: TENMS value is inexact, or not given.	R	0
29:24	Reserved		R	0
23:0	TENMS	Reload value for 10ms timing, subject to system clock skew errors. If the value reads as zero, the calibration value is not known.	R/W	0xA71FF

2.3 NESTED VECTORED INTERRUPT CONTROLLER (NVIC)

All interrupts including the core exceptions are managed by the NVIC. NVIC has the following Features:

- The NVIC supports 32 vectored interrupts.
- 4 programmable interrupt priority levels with hardware priority level masking.
- Low-latency exception and interrupt handling.
- Efficient processing of late arriving interrupts.
- Implementation of System Control Registers
- Software interrupt generation.

2.3.1 INTERRUPT AND EXCEPTION VECTORS

Execution No.	Priority	Function	Description	Address Offset
0	-	-	Reserved	0x0000 0000
1	-3	Reset	Reset	0x0000 0004
2	-2	NMI_Handler	Non maskable interrupt.	0x0000 0008
3	-1	HardFault_Handler	All class of fault	0x0000 000C
4~10	Reserved	Reserved	Reserved	-
11	Settable	SVCCalll		0x0000 002C
12~13	Reserved	Reserved	Reserved	-
14	Settable	PendSV		0x0000 0038
15	Settable	SysTick		0x0000 003C
16	Settable	IRQ0/NDTIRQ	NDT	0x0000 0040
17	Settable	IRQ1/USBIRQ	USB	0x0000 0044
18	Settable	IRQ2/LCDIRQ	LCD	0x0000 0048
19	Settable	IRQ3/I2S0IRQ	I2S0	0x0000 004C
20	Settable	IRQ4/I2S1IRQ	I2S1	0x0000 0050
21	Settable	IRQ5/CMP3IRQ	CMP3	0x0000 0054
22	Settable	IRQ6/SPI0IRQ	SPI0	0x0000 0058
23	Settable	IRQ7/SPI1IRQ	SPI1	0x0000 005C
24	Settable	IRQ8/UART2IRQ	UART2	0x0000 0060
25	Settable	IRQ9/UART3IRQ	UART3	0x0000 0064
26	Settable	IRQ10/I2C0IRQ	I2C0	0x0000 0068
27	Settable	IRQ11/I2C1IRQ	I2C1	0x0000 006C
28	Settable	IRQ12/CMP2IRQ	CMP2	0x0000 0070
29	Settable	IRQ13/UART0IRQ	UART0	0x0000 0074
30	Settable	IRQ14/UART1IRQ	UART1	0x0000 0078

31	Settable	IRQ15/CT16B0IRQ	CT16B0	0x0000 007C
32	Settable	IRQ16/CT16B1IRQ	CT16B1	0x0000 0080
33	Settable	IRQ17/CT16B2IRQ	CT16B2	0x0000 0084
34	Settable	IRQ18/CMP1IRQ	CMP1	0x0000 0088
35	Settable	IRQ19/CT16B3IRQ	CT16B3	0x0000 008C
36	Settable	IRQ20/CT16B4IRQ	CT16B4	0x0000 0090
37	Settable	IRQ21/CT16B5IRQ	CT16B5	0x0000 0094
38	Settable	IRQ22/EBIIRQ	EBI	0x0000 0098
39	Settable	IRQ23/RTCIRQ	RTC	0x0000 009C
40	Settable	IRQ24/ADCIRQ	ADC	0x0000 00A0
41	Settable	IRQ25/WDTIRQ	WDT	0x0000 00A4
42	Settable	IRQ26/LVDIRQ	LVD	0x0000 00A8
43	Settable	IRQ27/CMP0IRQ	CMP0	0x0000 00AC
44	Settable	IRQ28/P3IRQ	GPIO interrupt status of port 3	0x0000 00B0
45	Settable	IRQ29/P2IRQ	GPIO interrupt status of port 2	0x0000 00B4
46	Settable	IRQ30/P1IRQ	GPIO interrupt status of port 1	0x0000 00B8
47	Settable	IRQ31/P0IRQ	GPIO interrupt status of port 0	0x0000 00BC

2.3.2 NVIC REGISTERS

2.3.2.1 IRQ0~31 Interrupt Set-Enable Register (NVIC_ISER)

Address: 0xE000 E100 (Refer to Cortex-M0 Spec.)

The ISER enables interrupts, and shows the interrupts that are enabled.

Bit	Name	Description	Attribute	Reset
31:0	SETENA[31:0]	Interrupt set-enable bits. Write→ 0: No effect 1: Enable interrupt. Read→ 0: Interrupt disabled 1: Interrupt enabled.	R/W	0

2.3.2.2 IRQ0~31 Interrupt Clear-Enable Register (NVIC_ICER)

Address: 0xE000 E180 (Refer to Cortex-M0 Spec.)

The ICER disables interrupts, and shows the interrupts that are enabled.

Bit	Name	Description	Attribute	Reset
31:0	CLRENA[31:0]	Interrupt clear-enable bits. Write→ 0: No effect 1: Disable interrupt.	R/W	0

		Read→ 0: Interrupt disabled 1: Interrupt enabled.		

2.3.2.3 IRQ0~31 Interrupt Set-Pending Register (NVIC_ISPR)

Address: 0xE000 E200 (Refer to Cortex-M0 Spec.)

The ISPR forces interrupts into the pending state, and shows the interrupts that are pending.

✸ ***Note: Writing 1 to the ISPR bit corresponding to***
1. an interrupt that is pending has no effect
2. a disabled interrupt sets the state of that interrupt to pending.

Bit	Name	Description	Attribute	Reset
31:0	SETPEND[31:0]	Interrupt set-pending bits. Write→ 0: No effect 1: Change interrupt state to pending Read→ 0: Interrupt is not pending 1: Interrupt is pending	R/W	0

2.3.2.4 IRQ0~31 Interrupt Clear-Pending Register (NVIC_ICPR)

Address: 0xE000 E280 (Refer to Cortex-M0 Spec.)

The ICPR removes the pending state from interrupts, and shows the interrupts that are pending.

✸ ***Note: Writing 1 to an ICPR bit does not affect the active state of the corresponding interrupt.***

Bit	Name	Description	Attribute	Reset
31:0	CLRPEND[31:0]	Interrupt clear-pending bits. Write→ 0: No effect 1: Removes pending state of an interrupt Read→ 0: Interrupt is not pending 1: Interrupt is pending	R/W	0

2.3.2.5 IRQ0~31 Interrupt Priority Register (NVIC_IPRn) (n=0~7)

Address: 0xE000 E400 + 0x4 * n (Refer to Cortex-M0 Spec.)

The interrupt priority registers provide an 8-bit priority field for each interrupt, and each register holds four priority fields. This means the number of registers is implementation-defined, and corresponds to the number of implemented interrupts.

Bit	Name	Description	Attribute	Reset
31:24	PRI_(4*n+3)	Each priority field holds a priority value, 0-192. The lower the value, the greater the priority of the corresponding interrupt. The processor implements only bits[31:30] of each field, bits [29:24] read as zero and ignore writes. This means writing 255 to a priority register saves value 192 to the register.	R/W	0
23:16	PRI_(4*n+2)	Each priority field holds a priority value, 0-192. The lower the value, the greater the priority of the corresponding interrupt. The processor implements only bits[23:22] of each field, bits [21:16] read as zero and ignore writes. This means writing 255 to a priority register saves value 192 to the register.	R/W	0

15:8	PRI_(4*n+1)	Each priority field holds a priority value, 0-192. The lower the value, the greater the priority of the corresponding interrupt. The processor implements only bits[15:14] of each field, bits [13:8] read as zero and ignore writes. This means writing 255 to a priority register saves value 192 to the register.	R/W	0
7:0	PRI_4*n	Each priority field holds a priority value, 0-192. The lower the value, the greater the priority of the corresponding interrupt. The processor implements only bits[7:6] of each field, bits [5:0] read as zero and ignore writes. This means writing 255 to a priority register saves value 192 to the register.	R/W	0

2.4 APPLICATION INTERRUPT AND RESET CONTROL (AIRC)

Address: 0xE000 ED0C (Refer to Cortex-M0 Spec)

The entire MCU, including the core, can be reset by SW by setting the SYSRESREQ bit in the AIRC register in Cortex-M0 spec.

✸ ***Note: To write to this register, user must write 0x05FA to the VECTKEY field at the same time, otherwise the processor ignores the write.***

Bit	Name	Description	Attribute	Reset
31:16	VECTKEY	Register key. Read as unknown. Write 0x05FA to VECTKEY, otherwise the write is ignored.	R/W	0
15	ENDIANESS	Data endianness implemented 0: Little-endian 1: Big-endian	R	0
14:3	Reserved		R	0
2	SYSRESETREQ	System reset request. This bit read as 0. 0: No effect 1: Requests a system level reset.	W	0
1	VECTCLRACTIVE	Reserved for debug use. This bit read as 0. When writing to the register you must write 0 to this bit, otherwise behavior is Unpredictable.	W	0
0	Reserved		R	0

2.5 CODE OPTION TABLE

Address: 0x1FFF 2000

Bit	Name	Description	Attribute	Reset
31:16	Code Security[15:0]	Code Security 0xFFFF: CS0 0x5A5A: CS1 0xA5A5: CS2 Others: CS2	R/W	FFFF
15:3	Reserved		R	All 1
2	BOOTPINEN	Boot Pin enable 0: Disable 1: Enable (default)	R/W	1
1	EXTRSTHWDIS	External reset HW disable bit 0: Enable (HW enables, FW can NOT control with SYS0_EXRSTCTRL) 1: Disable (default) (FW can control with SYS0_EXRSTCTRL)	R/W	1
0	BLEN	Boot loader enable 0: Disable 1: Enable (default)	R/W	1

2.6 UNIQUE NUMBER

The unique number is a 8-byte unique device serial number of each IC. In other words, the unique number is different and discontinuous for each IC. Users can use the unique number to pair in RF application, or use as USB string serial number.

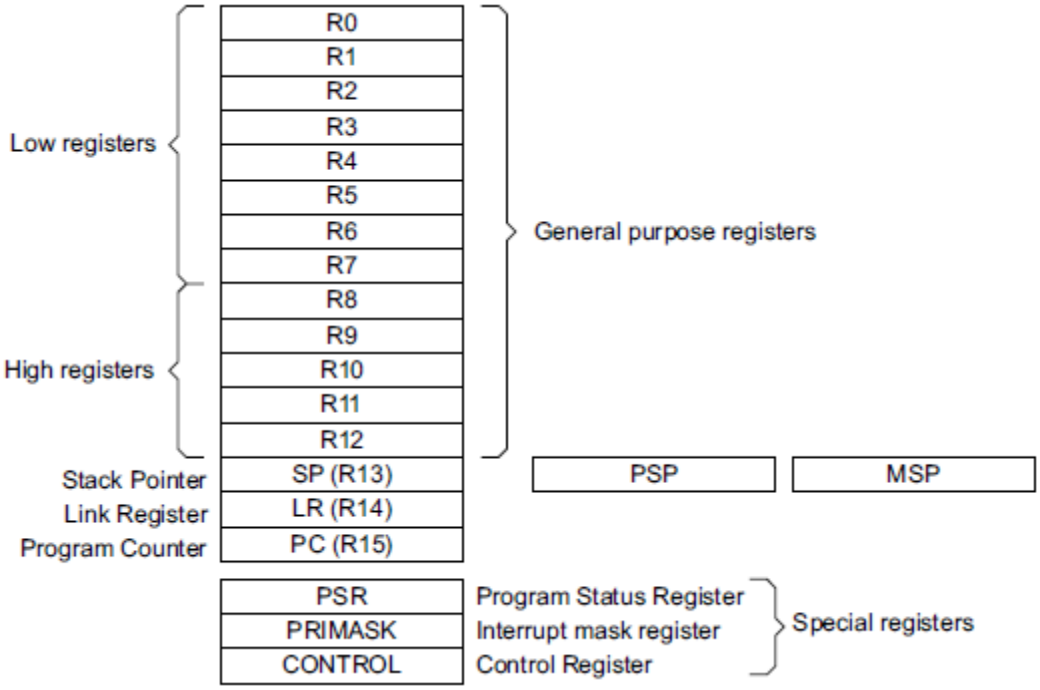
Address: 0x1FFF 2450

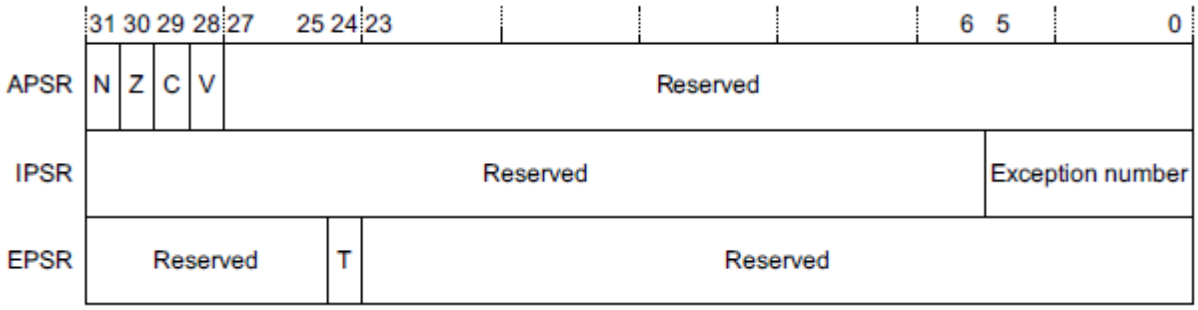
Bit	Name	Description	Attribute	Reset
31:0	L4BYTE[31:0]	Lower 4 bytes of Unique number	R	By Die

Address: 0x1FFF 2458

Bit	Name	Description	Attribute	Reset
31:0	H4BYTE[31:0]	High 4 bytes of Unique number	R	By Die

2.7 CORE REGISTER OVERVIEW



Register	Description (Refer to Cortex-M0 Spec)
R0~R12	General-purpose registers for data operations.
SP (R13)	The Stack Pointer (SP). In Thread mode, the CONTROL register indicates the stack pointer to use, Main Stack Pointer (MSP) or Process Stack Pointer (PSP) On reset, the processor loads the MSP with the value from address 0x00000000.
LR (R14)	The Link Register (LR). It stores the return information for subroutines, function calls, and exceptions.
PC (R15)	The Program Counter (PC). It contains the current program address. On reset, the processor loads the PC with the value of the reset vector, at address 0x00000004.
PSR	The Program Status Register (PSR) combines: • Application Program Status Register (APSR) • Interrupt Program Status Register (IPSR) • Execution Program Status Register (EPSR). These registers are mutually exclusive bit fields in the 32-bit PSR. 
PRIMASK	The PRIMASK register prevents activation of all exceptions with configurable priority.
CONTROL	The CONTROL register controls the stack used when the processor is in Thread mode.

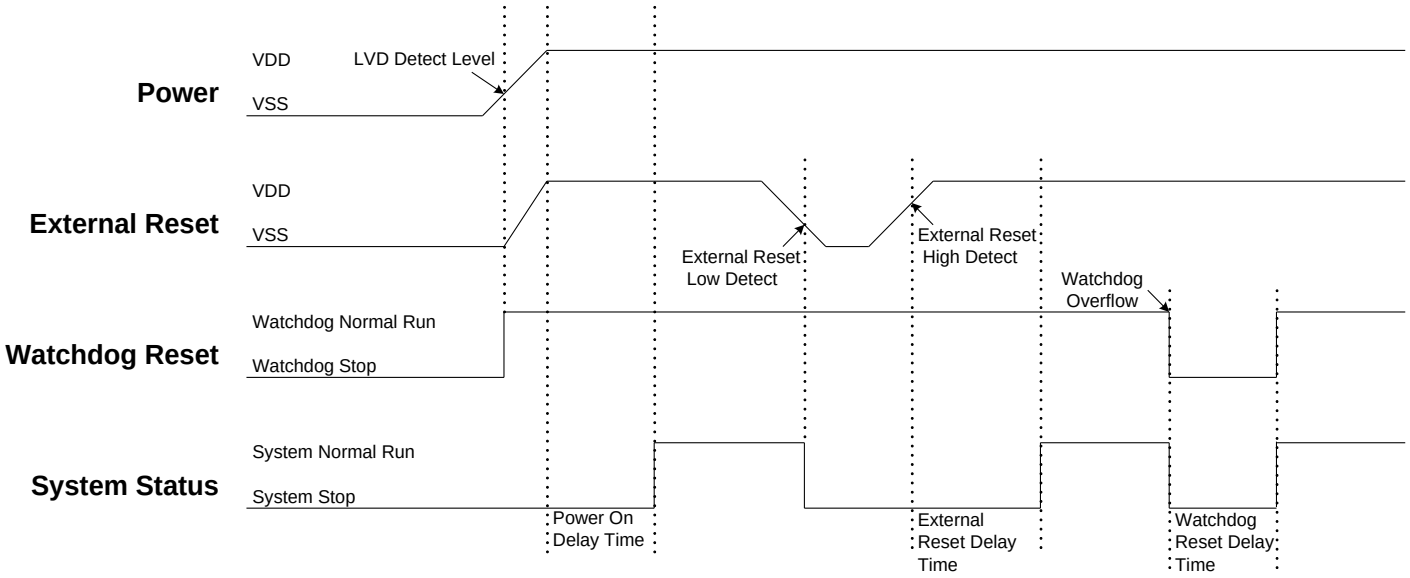
3 SYSTEM CONTROL

3.1 RESET

A system reset is generated when one of the following events occurs:
1. A low level on the RST pin (external reset).
2. Power-on reset (POR reset)
3. LVD reset
4. Watchdog Timer reset (WDT reset)
5. Software reset (SW reset)

The reset source can be identified by checking the reset flags in System Reset Status register (SYS0_RSTST). These sources act on the RST pin and it is always kept low during the delay phase. The RESET service routine vector is fixed at address 0x00000004 in the memory map. For more details, refer to Interrupt and Exception Vectors.

Finishing any reset sequence needs some time. The system provides complete procedures to make the power on reset successful. For different oscillator types, the reset time is different. That causes the VDD rise rate and start-up time of different oscillator is not fixed. RC type oscillator's start-up time is very short, but the crystal type is longer. Under client terminal application, users have to take care of the power on reset time for the master terminal requirement. The reset timing diagram is as following.



3.1.1 POWER-ON RESET (POR)

The power on reset depends on LVD operation for most power-up situations. The power supplying to system is a rising curve and needs some time to achieve the normal voltage. Power on reset sequence is as following:

- **Power-up:** System detects the power voltage up and waits for power stable.
- **External reset (only external reset pin enable):** System checks external reset pin status. If external reset pin is not high level, the system keeps reset status and waits external reset pin released.
- **System initialization:** All system registers is set as initial conditions and system is ready.
- **Oscillator warm up:** Oscillator operation is successfully and supply to system clock.
- **Program executing:** Power on sequence is finished and program executes from Boot loader if BLEN bit =1, or from 0x0 if BLEN bit =0.

3.1.2 WATCHDOG RESET (WDT RESET)

Watchdog reset is a system protection. In normal condition, system works well and clears watchdog timer by program. Under error condition, system is in unknown situation and watchdog can't be clear by program before watchdog timer overflow. Watchdog timer overflow occurs and the system is reset. After watchdog reset, the system restarts and returns normal mode. Watchdog reset sequence is as following.

- **Watchdog timer status:** System checks watchdog timer overflow status. If watchdog timer overflow occurs, the system is reset.
- **System initialization:** All system registers is set as initial conditions and system is ready.
- **Oscillator warm up:** Oscillator operation is successfully and supply to system clock.
- **Program executing:** Power on sequence is finished and program executes from Boot loader if BLEN bit =1, or from 0x0 if BLEN bit =0.

Watchdog timer application note is as following.

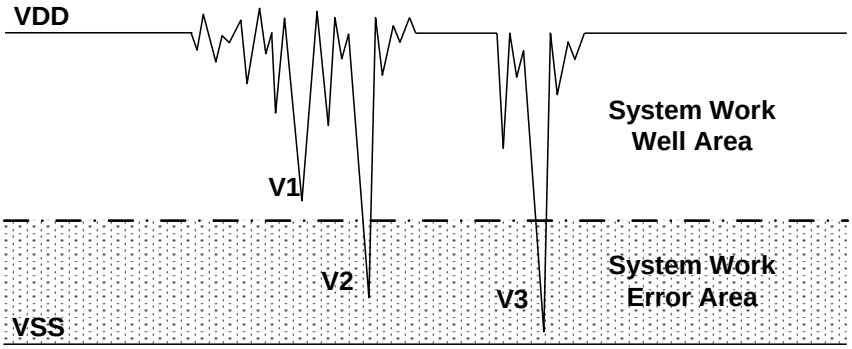
- Before clearing watchdog timer, check I/O status and check RAM contents can improve system error.
- Don't clear watchdog timer in interrupt vector and interrupt service routine. That can improve main routine fail.
- Clearing watchdog timer program is only at one part of the program. This way is the best structure to enhance the watchdog timer function.

✷ ***Note: Please refer to the "WATCHDOG TIMER" about watchdog timer detail information.***

3.1.3 BROWN-OUT RESET

3.1.3.1 BROWN OUT DESCRIPTION

The brown-out reset is a power dropping condition. The power drops from normal voltage to low voltage by external factors (e.g. EFT interference or external loading changed). The brown out reset would make the system not work well or executing program error.



Brown-Out Reset Diagram

The power dropping might through the voltage range that's the system dead-band. The dead-band means the power range can't offer the system minimum operation power requirement. The above diagram is a typical brown out reset diagram. There is a serious noise under the VDD, and VDD voltage drops very deep. There is a dotted line to separate the system working area. The above area is the system work well area. The below area is the system work error area called dead-band. V1 doesn't touch the below area and not affect the system operation. But the V2 and V3 is under the below area and may induce the system error occurrence. Let system under dead-band includes some conditions.

DC application:
The power source of DC application is usually using battery. When low battery condition and MCU drive any loading, the

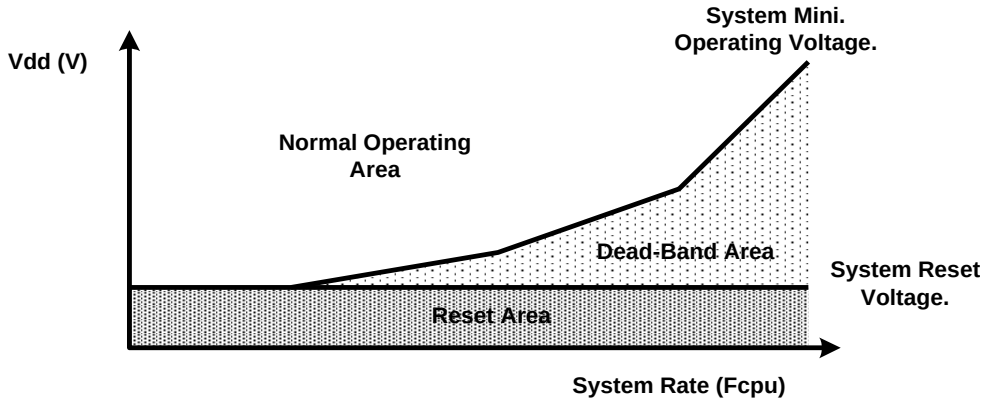
power drops and keeps in dead-band. Under the situation, the power won't drop deeper and not touch the system reset voltage. That makes the system under dead-band.

AC application:
In AC power application, the DC power is regulated from AC power source. This kind of power usually couples with AC noise that makes the DC power dirty. Or the external loading is very heavy, e.g. driving motor. The loading operating induces noise and overlaps with the DC power. VDD drops by the noise, and the system works under unstable power situation.

The power on duration and power down duration are longer in AC application. The system power on sequence protects the power on successful, but the power down situation is like DC low battery condition. When turn off the AC power, the VDD drops slowly and through the dead-band for a while.

3.1.3.2 THE SYSTEM OPERATING VOLTAGE DESCRIPTION

To improve the brown out reset needs to know the system minimum operating voltage which is depend on the system executing rate and power level. Different system executing rates have different system minimum operating voltage. The electrical characteristic section shows the system voltage to executing rate relationship.



Normally the system operation voltage area is higher than the system reset voltage to VDD, and the reset voltage is decided by LVD detect level. The system minimum operating voltage rises when the system executing rate upper even higher than system reset voltage. The dead-band definition is the system minimum operating voltage above the system reset voltage.

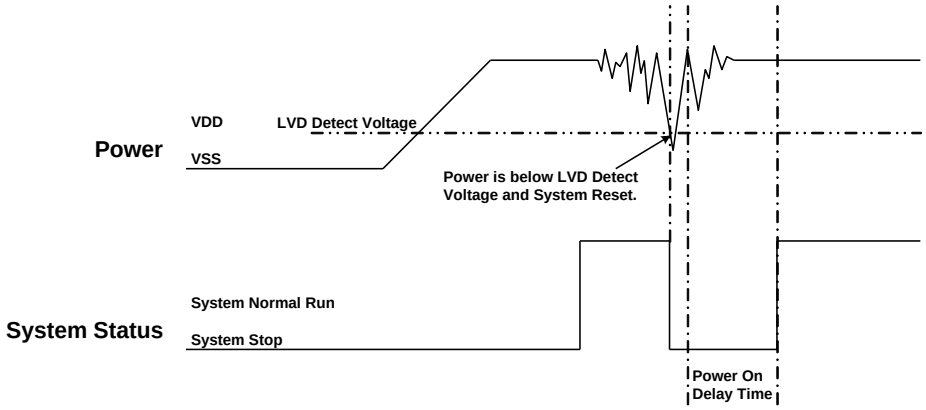
3.1.3.3 BROWN-OUT RESET IMPROVEMENT

How to improve the brown reset condition? There are some methods to improve brown out reset as following.

- **LVD reset**
- **Watchdog reset**
- **Reduce the system executing rate**
- **External reset circuit. (Zener diode reset circuit, Voltage bias reset circuit, External reset IC)**

✷ ***Note: The "Zener diode reset circuit", "Voltage bias reset circuit" and "External reset IC" can completely improve the brown out reset, DC low battery and AC slow power down conditions.***

LVD reset:



The LVD (low voltage detector) is built-in SONiX 32-bit MCU to be brown out reset protection. When the VDD drops and is below LVD detect voltage, the LVD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, SW can monitor the signal by reading a dedicated status register. An additional threshold level can be selected to cause a forced reset of the chip. The LVD detect level is different by each MCU. The LVD voltage level is a point of voltage and not easy to cover all dead-band range. Using LVD to improve brown out reset is dependent on application requirement and environment. If the power variation is very deep, violent and trigger the LVD, the LVD can be the protection. If the power variation can touch the LVD detect level and make system work error, the LVD can't be the protection and need to other reset methods. More detail LVD information is in the electrical characteristic section.

Watchdog reset:
The watchdog timer is a protection to make sure the system executes well. Normally the watchdog timer would be clear at one point of program. Don't clear the watchdog timer in several addresses. The system executes normally and the watchdog won't reset system. When the system is under dead-band and the execution error, the watchdog timer can't be clear by program. The watchdog is continuously counting until overflow occurrence. The overflow signal of watchdog timer triggers the system to reset and return to normal mode after reset sequence. This method also can improve brown out reset condition and make sure the system to return normal mode.
If the system reset by watchdog and the power is still in dead-band, the system reset sequence won't be successful and the system stays in reset status until the power return to normal range.

Reduce the system executing rate:
If the system rate is fast and the dead-band exists, to reduce the system executing rate can improve the dead-band. The lower system rate is with lower minimum operating voltage. Select the power voltage that's no dead-band issue and find out the mapping system rate. Adjust the system rate to the value and the system exits the dead-band issue. This way needs to modify whole program timing to fit the application requirement.

External reset circuit:
The external reset methods also can improve brown out reset and is the complete solution. There are three external reset circuits to improve brown out reset including "Zener diode reset circuit", "Voltage bias reset circuit" and "External reset IC". These three reset structures use external reset signal and control to make sure the MCU be reset under power dropping and under dead-band. The external reset information is described in the next section.

3.1.4 EXTERNAL RESET

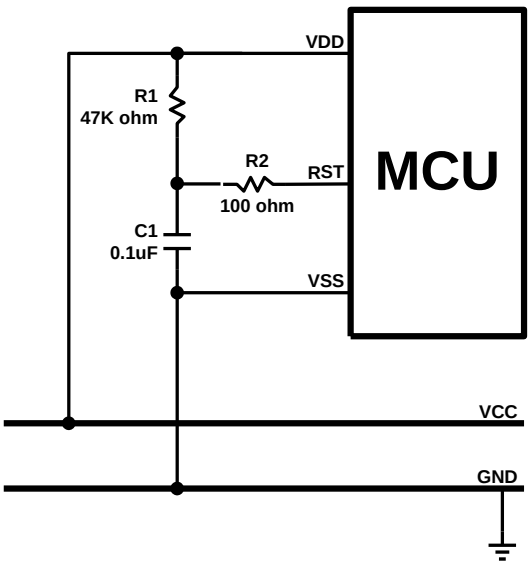
External reset function is controlled by External RESET pin control (SYS0_EXRSTCTRL) register. Default value is 1, which means external reset function is enabled. External reset pin is Schmitt Trigger structure and low level active. The system is running when reset pin is high level voltage input. The reset pin receives the low voltage and the system is reset. The external reset operation actives in power on and normal running mode. During system power-up, the external reset pin must be high level input, or the system keeps in reset status. External reset sequence is as following.

- **External reset (only external reset pin enable):** System checks external reset pin status. If external reset pin is not high level, the system keeps reset status and waits external reset pin released.

- **System initialization:** All system registers is set as initial conditions and system is ready.
- **Oscillator warm up:** Oscillator operation is successfully and supply to system clock.
- **Program executing:** Power on sequence is finished and program executes from Boot loader if BLEN bit =1, or from 0x0 if BLEN bit =0..

The external reset can reset the system during power on duration, and good external reset circuit can protect the system to avoid working at unusual power condition, e.g. brown out reset in AC power application.

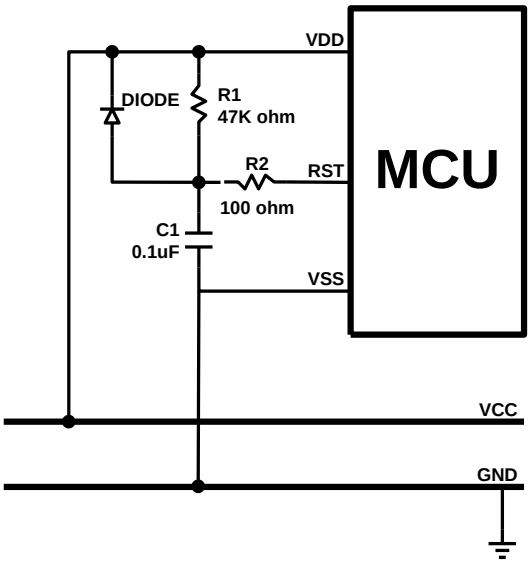
3.1.4.1 SIMPLY RC RESET CIRCUIT



This is the basic reset circuit, and only includes R1 and C1. The RC circuit operation makes a slow rising signal into reset pin as power up. The reset signal is slower than VDD power up timing, and system occurs a power on signal from the timing difference.

✷ ***Note: The reset circuit is no any protection against unusual power or brown out reset.***

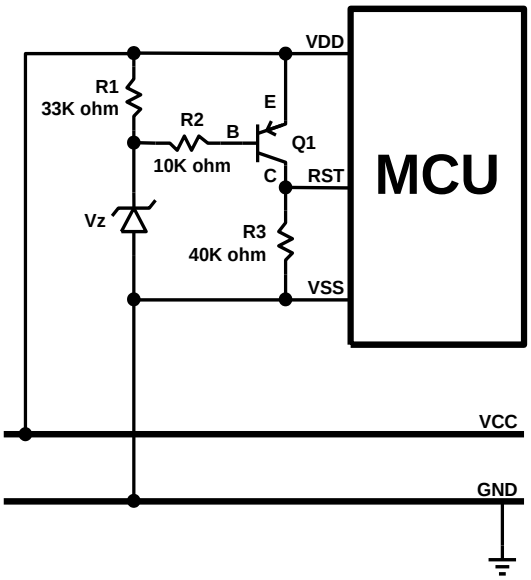
3.1.4.2 DIODE & RC RESET CIRCUIT



This is the better reset circuit. The R1 and C1 circuit operation is like the simply reset circuit to make a power on signal. The reset circuit has a simply protection against unusual power. The diode offers a power positive path to conduct higher power to VDD. It is can make reset pin voltage level to synchronize with VDD voltage. The structure can improve slight brown out reset condition.

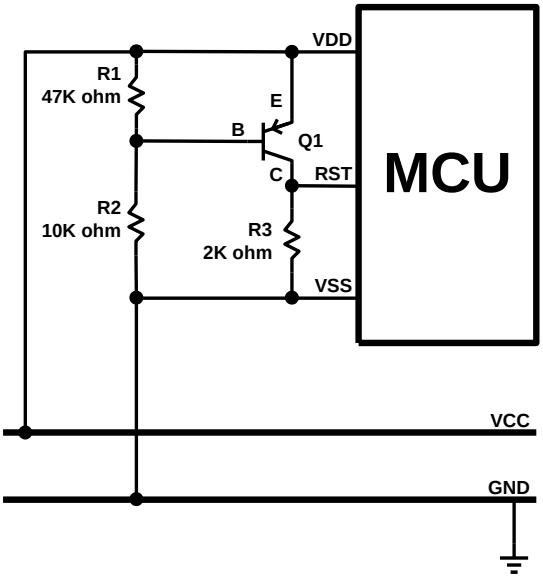
✸ ***Note: The R2 100 ohm resistor of "Simply reset circuit" and "Diode & RC reset circuit" is necessary to limit any current flowing into reset pin from external capacitor C in the event of reset pin breakdown due to Electrostatic Discharge (ESD) or Electrical Over-stress (EOS).***

3.1.4.3 ZENER DIODE RESET CIRCUIT



The Zener diode reset circuit is a simple low voltage detector and can **improve brown out reset condition completely**. Use Zener voltage to be the active level. When VDD voltage level is above "Vz + 0.7V", the C terminal of the PNP transistor outputs high voltage and MCU operates normally. When VDD is below "Vz + 0.7V", the C terminal of the PNP transistor outputs low voltage and MCU is in reset mode. Decide the reset detect voltage by Zener specification. Select the right Zener voltage to conform the application.

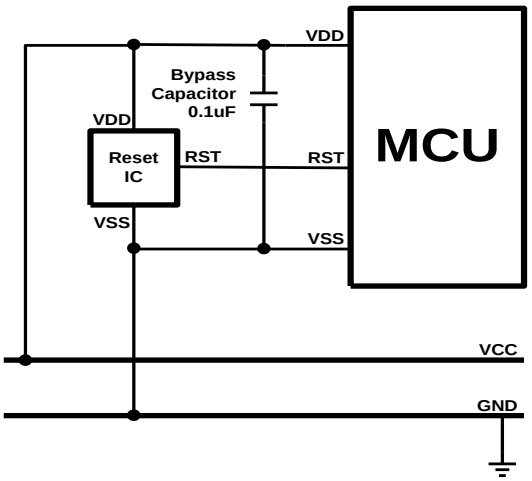
3.1.4.4 VOLTAGE BIAS RESET CIRCUIT



The voltage bias reset circuit is a low cost voltage detector and can **improve brown out reset condition completely**. The operating voltage is not accurate as Zener diode reset circuit. Use R1, R2 bias voltage to be the active level. When VDD voltage level is above or equal to “0.7V x (R1 + R2) / R1”, the C terminal of the PNP transistor outputs high voltage and MCU operates normally. When VDD is below “0.7V x (R1 + R2) / R1”, the C terminal of the PNP transistor outputs low voltage and MCU is in reset mode.
Decide the reset detect voltage by R1, R2 resistances. Select the right R1, R2 value to conform the application. In the circuit diagram condition, the MCU’s reset pin level varies with VDD voltage variation, and the differential voltage is 0.7V. If the VDD drops and the voltage lower than reset pin detect level, the system would be reset. If want to make the reset active earlier, set the R2 > R1 and the cap between VDD and C terminal voltage is larger than 0.7V. The external reset circuit is with a stable current through R1 and R2. For power consumption issue application, e.g. DC power system, the current must be considered to whole system power consumption.

✸ ***Note: Under unstable power condition as brown out reset, “Zener diode reset circuit” and “Voltage bias reset circuit” can protects system no any error occurrence as power dropping. When power drops below the reset detect voltage, the system reset would be triggered, and then system executes reset sequence. That makes sure the system work well under unstable power situation.***

3.1.4.5 EXTERNAL RESET IC



The external reset circuit also uses external reset IC to enhance MCU reset performance. This is a high cost and good effect solution. By different application and system requirement to select suitable reset IC. The reset circuit can improve all power variation.

3.1.5 SOFTWARE RESET

The entire MCU, including the core, can be reset by software by setting the SYSRESREQ bit in the AIRC (Application Interrupt and Reset Control) register in Cortex-M0 spec.

The software-initiated system reset sequence is as follows:

1. A software reset is initiated by setting the SYSRESREQ bit.
2. An internal reset is asserted.
3. The internal reset is deasserted and the MCU loads from memory the initial stack pointer, the initial program counter, and the first instruction designated by the program counter, and then begins execution.

3.2 SYSTEM CLOCK

Different clock sources can be used to drive the system clock (SYSCLK):

- 12 MHz internal high speed RC (IHRC)
- 32 KHz internal low speed RC (ILRC)
- PLL clock
- High speed external (EHS) crystal clock
- Low speed external (ELS) 32.768 KHz crystal

Each clock source can be switched on or off independently when it is not used, to optimize power consumption.

The micro-controller is a dual clock system. There are high-speed clock and low-speed clock. The high-speed clock is generated from the external oscillator & on-chip PLL circuit. The low-speed clock is generated from on-chip low-speed RC oscillator circuit (ILRC 16 KHz).

3.2.1 INTERNAL RC CLOCK SOURCE

3.2.1.1 Internal High-speed RC Oscillator (IHRC)

The internal high-speed oscillator is 12MHz RC type. The accuracy is ±0.2% under commercial condition.
The IHRC can be switched on and off using the IHRCEN bit in Analog Block Control register (SYS0_ANBCTRL).

3.2.1.2 Internal Low-speed RC Oscillator (ILRC)

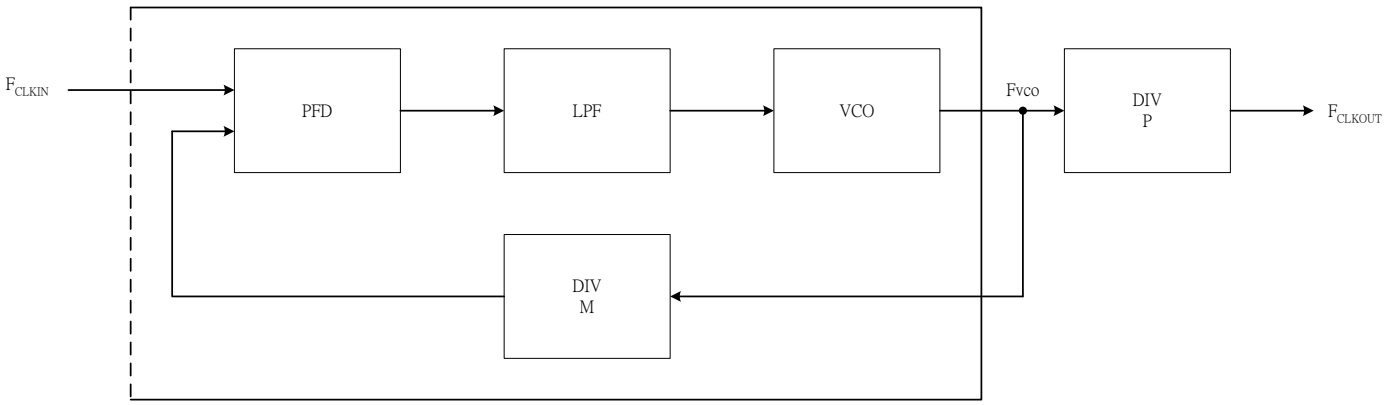
The system low clock source is the internal low-speed oscillator built in the micro-controller. The low-speed oscillator uses RC type oscillator circuit. The frequency is affected by the voltage and temperature of the system. In common condition, the frequency of the RC oscillator is about 32 KHz.

✷ ***Note: The ILRC can ONLY be switched on and off by HW.***

3.2.2 PLL

SONiX 32-bit MCU uses the PLL to create the clocks for the core and peripherals. The input frequency range is 10MHz to 25MHz. The input clock is divided down and fed to the Phase-Frequency Detector (PFD). This block compares the phase and frequency of its inputs, and generates a control signal when phase and/ or frequency do not match. The loop filter filters these control signals and drives the voltage controlled oscillator (VCO), which generates the main clock and optionally two additional phases. The VCO frequency range is 96MHz. These clocks are divided by P by the programmable post divider to create the output clock(s). The VCO output clock is then divided by M by the programmable feedback divider to generate the feedback clock. The output signal of the phase-frequency detector is also monitored by the lock detector, to signal when the PLL has locked on to the input clock.

The PLL settling time is 100 µs.



3.2.2.1 PLL Frequency selection

The PLL frequency equations:

$$F_{VCO} = F_{CLKIN} * M$$

$$F_{CLKOUT} = F_{VCO} / P$$

The PLL frequency is determined by the following parameters:

- F_{CLKIN}: Frequency from the PLLCLKSEL multiplexer.
- F_{VCO}: Frequency of the Voltage Controlled Oscillator (VCO); 96MHz.
- F_{CLKOUT}: Frequency of PLL output.
- P: System PLL post divider ratio, controlled by PSEL bits in PLL control register (SYS0_PLLCTRL).
- M: System PLL feedback divider ratio, controlled by MSEL bits in PLL control register (SYS0_PLLCTRL).

To select the appropriate values for M and P, it is recommended to follow these constraints:

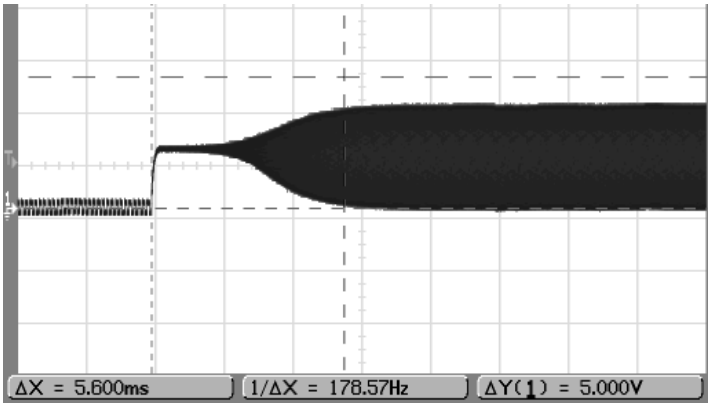
1. 10MHz ≤ F_{CLKIN} ≤ 25MHz
2. 96MHz
3. M = 4, 6, 8, 10, or 12
4. P = 2, or 4 (duty 50% +/- 2.5%)
5. F_{CLKOUT} = 30MHz, 50MHz, 60MHz, 24MHz, 36MHz, 48MHz, 72MHz, 64MHz
   with jitter < ±500 ps

3.2.3 EXTERNAL CLOCK SOURCE

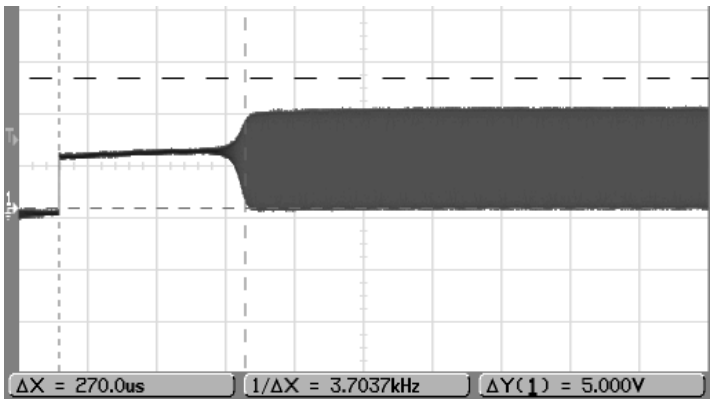
3.2.3.1 External High-speed (EHS) Clock

External high clock includes Crystal/Ceramic modules. The startup time of Crystal is longer. The oscillator start-up time decides reset time length.

4MHz Crystal

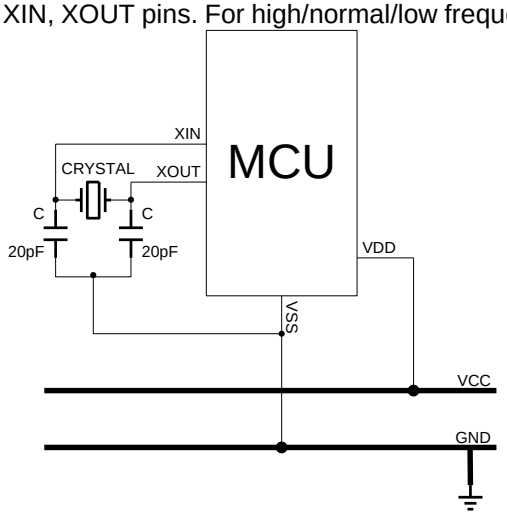


4MHz Ceramic



3.2.3.2 CRYSTAL/CERAMIC

Crystal/Ceramic devices are driven by XIN, XOUT pins. For high/normal/low frequency, the driving currents are different.



✷ ***Note: Connect the Crystal/Ceramic and C as near as possible to the XIN/XOUT/VSS pins of MCU.***

- **Structure:** 10MHz~25MHz EHS external crystal/ceramic resonator
- **Main Purpose:** System high clock source, RTC clock source, and PLL clock source.
- **Warm-up Time:** 2048*F_{EHS}
- **XIN/XOUT Shared Pin Selection:**

Oscillator Mode	XIN pin	XOUT pin
IHRC	GPIO	GPIO
EHS X'TAL	Crystal/Ceramic	Crystal/Ceramic

The resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

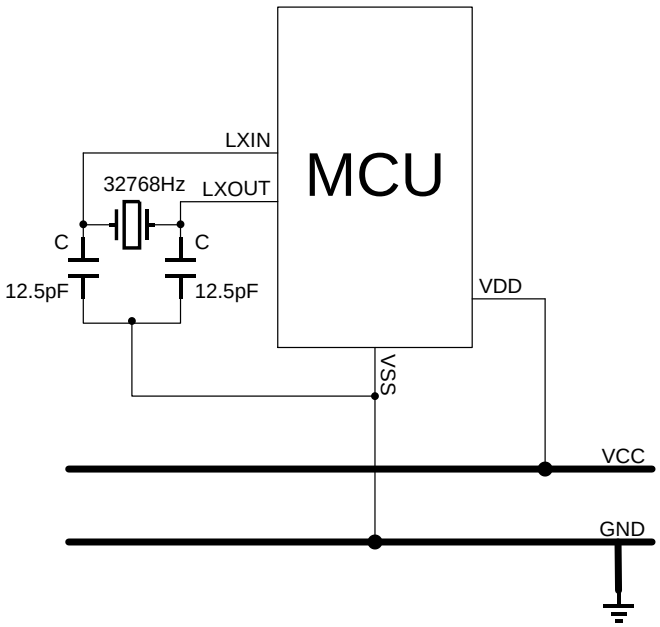
The EHS crystal is switched on and off using the EHSEN bit in Analog Block Control register (SYS0_ANBCTRL).

3.2.3.3 External Low-speed (ELS) Clock

The low-speed oscillator can use 32768 crystal oscillator circuit.

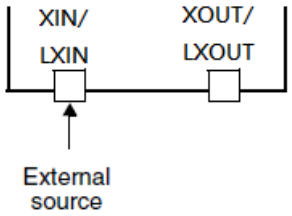
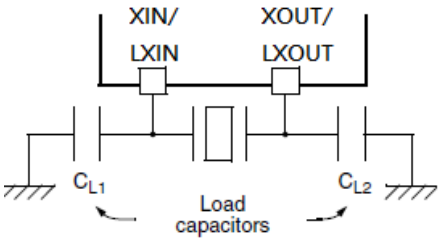
3.2.3.4 CRYSTAL

Crystal devices are driven by LXIN, LXOUT pins. The 32768 crystal and 10pF capacitor must be as near as possible to MCU. The ELS crystal is switched on and off using the ELSEN bit in Analog Block Control register (SYS0_ANBCTRL).



✷ ***Note: Connect the Crystal/Ceramic and C as near as possible to the LXIN/LXOUT/VSS pins of MCU.***

3.2.3.5 Bypass Mode

Clock Source	H/W Configuration	Description
External clock source (Bypass)		In Bypass mode, the external clock signal (square, sinus or triangle) with ~50% duty cycle must be provided to drive the XIN/LXIN pin while the XOUT/LXOUT pin should be the inverse of the input clock signal. EHS X'tal can have a frequency of up to 25 MHz. Select this mode by setting EHSEN bit in Analog Block Control register (SYS0_ANBCTRL). ELS X'TAL must have a frequency of 32.768 KHz. You select this mode by setting ELSEN bit in Analog Block Control register (SYS0_ANBCTRL).
External X'TAL (EHS/ELS X'TAL)		The 10 to 25 MHz EHS X'TAL has the advantage of producing a very accurate rate on the main clock ELS X'TAL must have a frequency of 32.768 KHz.

3.2.4 SYSTEM CLOCK (SYSCLK) SELECTION

After a system reset, the IHRC is selected as system clock. When a clock source is used directly or through the PLL as system clock, it is not possible to stop it.

A switch from one clock source to another occurs only if the target clock source is ready (clock stable after startup delay or PLL locked). If a clock source which is not yet ready is selected, the switch will occur when the clock source is ready.

Ready bits in SYS0_CSST register indicate which clock(s) is (are) ready and SYSCLKST bits in SYS0_CLKCFG register indicate which clock is currently used as system clock.

3.2.5 CLOCK-OUT CAPABILITY

The MCU clock output (CLKOUT) capability allows the clock to be output onto the external CLKOUT pin. The configuration registers of the corresponding GPIO port must be programmed in alternate function mode.

One of 6 clock signals can be selected as clock output:
1. HCLK
2. IHRC
3. ILRC
4. PLL clock output
5. ELS X'TAL
6. EHS X'TAL

The selection is controlled by the CLKOUTSEL bits in SYS1_AHBCLKEN register.

3.3 SYSTEM CONTROL REGISTERS 0

Base Address: 0x4006 0000

3.3.1 Analog Block Control register (SYS0_ANBCTRL)

Address Offset: 0x00

✷ ***Note: EHSEN / ELSEN / IHRCEN bit can NOT be cleared if the EHS X'tal / ELS X'tal / IHRC is selected as system clock or is selected to become the system clock.***

Bit	Name	Description	Attribute	Reset
31:6	Reserved		R	0
5	EHSFREQ	Frequency range (driving ability) of EHS X'TAL 0: <=12MHz 1: >12MHz	R/W	0
4	EHSEN	External high-speed clock enable 0: Disable EHS X'TAL. 1: Enable EHS X'TAL.	R/W	0
3	Reserved		R	0
2	ELSEN	External low-speed oscillator enable 0: Disable External 32.768 KHz oscillator 1: Enable External 32.768 KHz oscillator	R/W	0
1	Reserved		R	0
0	IHRCEN	Internal high-speed clock enable 0: Disable internal 12 MHz RC oscillator. 1: Enable internal 12 MHz RC oscillator.	R/W	1

3.3.2 PLL control register (SYS0_PLLCTRL)

Address Offset: 0x04

✷ ***Note: PLLEN bit can NOT be cleared if the PLL is selected as system clock or is selected to become the system clock.***

Bit	Name	Description	Attribute	Reset
31:16	Reserved		R	0
15	PLLEN	PLL enable 0: Disable 1: Enable	R/W	0
14:13	Reserved		R	0
12	PLLCLKSEL	System PLL clock source 0: IHRC 12 MHz oscillator 1: EHS X'TAL 10MHz ~25MHz	R/W	0
11:6	Reserved		R	0
5	PSEL	Post divider value. 0: P = 2 1: P = 4	R/W	0
4:3	Reserved		R	0

2:0	MSEL[2:0]	Feedback divider value. 000: M = 4 001: M = 6 010: M = 8 011: M = 10 100: M = 12 Other: Reserved	R/W	0

To select the appropriate values for M and P, it is recommended to follow these constraints:
1. 10MHz ≤ F_{CLKIN} ≤ 25MHz
2. 96MHz ≤ F_{VCO}
3. M = 4, 6, 8, 10, or 12
4. P = 2, or 4 (duty 50% +/- 2.5%)
5. F_{CLKOUT} = 30MHz, 50MHz, 60MHz, 24MHz, 36MHz, 48MHz, 72MHz, 64MHz
   with jitter < ±500 ps

3.3.2.1 RECOMMEND FREQUENCY SETTING

$F_{VCO} = F_{CLKIN} * M$
$F_{CLKOUT} = F_{VCO} / P$

F_{CLKIN}(MHz)	MSEL[2:0]	M	F_{VCO}(MHz)= F_{CLKIN} *M 96 MHz	PSEL	P	F_{CLKOUT}(MHz) = F_{VCO}/P
12	010b	**8**	**96**	0	**2**	48
16	001b	**6**	**96**	0	**2**	48

3.3.3 Clock Source Status register (SYS0_CSST)

Address Offset: 0x08

Bit	Name	Description	Attribute	Reset
31:7	Reserved		R	0
6	PLLRDY	PLL clock ready flag 0: PLL unlocked 1: PLL locked	R	0
5	Reserved		R	0
4	EHSRDY	External high-speed clock ready flag 0: EHS oscillator not ready 1: EHS oscillator ready	R	0
3	Reserved		R	0
2	ELSRDY	External low-speed clock ready flag 0: ELS oscillator not ready 1: ELS oscillator ready	R	0
1	Reserved		R	0
0	IHRCRDY	IHRC ready flag 0: IHRC not ready 1: IHRC ready	R	1

3.3.4 System Clock Configuration register (SYS0_CLKCFG)

Address Offset: 0x0C

Bit	Name	Description	Attribute	Reset
31:7	Reserved		R	0
6:4	SYSCLKST[2:0]	System clock switch status Set and cleared by HW to indicate which clock source is used as system clock. 000: IHRC is used as system clock 001: ILRC is used as system clock 010: EHS X'TAL is used as system clock 011: ELS X'TAL is used as system clock 100: PLL is used as system clock Other: Reserved	R	0
3	Reserved		R	0
2:0	SYSCLKSEL[2:0]	System clock switch Set and cleared by SW. 000: IHRC 001: ILRC 010: EHS X'TAL 011: ELS X'TAL 100: PLL output Other: Reserved	R/W	0

3.3.5 AHB Clock Prescale register (SYS0_AHBCP)

Address Offset: 0x10

Bit	Name	Description	Attribute	Reset
31:4	Reserved		R	0
3	DIV1P5	SYSCLK prescaler 0: SYSCLK = SYSCLK clock source / 1 1: SYSCLK = SYSCLK clock source / 1.5	R/W	0
2:0	AHBPRE[2:0]	AHB clock source prescaler 000: HCLK = SYSCLK / 1 001: HCLK = SYSCLK / 2 010: HCLK = SYSCLK / 4 011: HCLK = SYSCLK / 8 100: HCLK = SYSCLK / 16 101: HCLK = SYSCLK / 32 110: HCLK = SYSCLK / 64 111: HCLK = SYSCLK / 128	R/W	000b

3.3.6 System Reset Status register (SYS0_RSTST)

Address Offset: 0x14

Bit	Name	Description	Attribute	Reset
31:5	Reserved		R	0
4	PORRSTF	POR reset flag Set by HW when a POR reset occurs. 0: Read→No POR reset occurred Write→Clear this bit 1: POR reset occurred.	R/W	1
3	EXTRSTF	External reset flag Set by HW when a reset from the RESET pin occurs. 0: Read→No reset from RESET pin occurred Write→Clear this bit 1: Reset from RESET pin occurred.	R/W	0

2	LVDRSTF	LVD reset flag Set by HW when a LVD reset occurs. 0: Read→No LVD reset occurred Write→Clear this bit 1: LVD reset occurred.	R/W	0
1	WDTRSTF	WDT reset flag Set by HW when a WDT reset occurs. 0: Read→No watchdog reset occurred Write→Clear this bit 1: Watchdog reset occurred.	R/W	0
0	SWRSTF	Software reset flag Set by HW when a software reset occurs. 0: Read→No software reset occurred Write→Clear this bit 1: Software reset occurred.	R/W	1

3.3.7 LVD Control register (SYS0_LVDCTRL)

Address Offset: 0x18

The LVD control register selects four separate threshold values for generating a LVD interrupt to the NVIC or LVD reset.

Bit	Name	Description	Attribute	Reset
31:16	Reserved		R	0
15	LVDEN	LVD enable 0: Enable 1: Disable	R/W	0
14	LVDRSTEN	LVD Reset enable 0: Enable 1: Disable	R/W	0
13:7	Reserved		R	0
6:4	LVDINTLVL[2:0]	LVD interrupt level 100: 2.70V 101: 3.60V 011: Reserved for booting Other: Reserved	R/W	011b
3	Reserved		R	0
2:0	LVDRSTLVL[2:0]	LVD reset level 100: 2.70V 101: 3.60V 011: Reserved for booting Other: Reserved	R/W	011b

3.3.8 External RESET Pin Control register (SYS0_EXRSTCTRL)

Address Offset: 0x1C

✷ ***Note: FW can NOT change SYS0_EXRSTCTRL register if EXTRSTHWDIS bit in code option is 0.***

Bit	Name	Description	Attribute	Reset
31:1	Reserved		R	0

0	RESETDIS	External RESET pin disable bit. 0: Enable external RESET pin. (P3.7 acts as RESET pin) 1: Disable (P3.7 acts as GPIO pin)	R/W	By EXTRSTHWDIS bit in code option

3.3.9 SWD Pin Control register (SYS0_SWDCTRL)

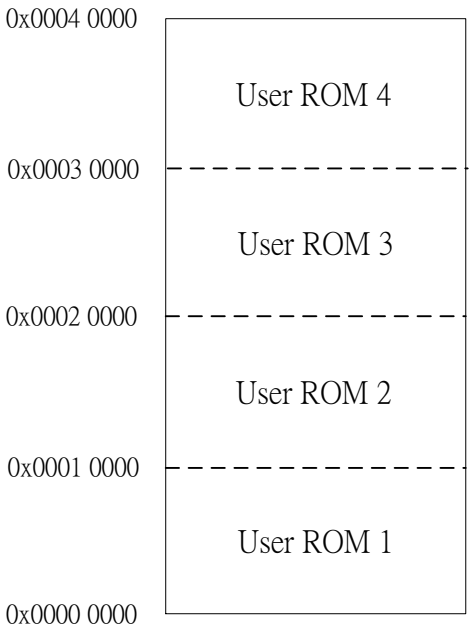
Address Offset: 0x20

Bit	Name	Description	Attribute	Reset
31:1	Reserved		R	0
0	SWDDIS	SWD pin disable bit. 0: Enable SWD pin. (P3.5 acts as SWDIO pin, P3.6 acts as SWCLK pin) 1: Disable. (P3.5 and P3.6 act as GPIO pins)	R/W	0

3.3.10 Interrupt Vector Table Mapping register (SYS0_IVTM)

Address Offset: 0x24

This register decides whether the ARM interrupt vector table is mapping to Boot ROM, User ROM, or SRAM.



Bit	Name	Description	Attribute	Reset
31:16	IVTMKEY[15:0]	IVTM register key. Read as 0. Behavior of writing to this register is ignored unless writing 0xA5A5 to IVTMKEY at the same time.	W	0
15:3	Reserved		R	0
2:0	IVTM[2:0]	Interrupt table mapping selection 000: Map to Boot ROM 001: Map to User ROM 1 011: Map to User ROM 2 100: Map to User ROM 3 101: Map to User ROM 4 Other: Reserved	R/W	By BLEN in code option

3.3.11 Noise Detect Control register (SYS0_NDTCTRL)

Address Offset: 0x28

Bit	Name	Description	Attribute	Reset
31:2	Reserved		R	0
1	NDT5V_IE	NDT0: Disable for VDD 5V interrupt enable bit. 0: Disable. 1: Enable. (The noise on IC VDD 5V domain detected by NDT5V IP will trigger.NDT interrupt IRQ0)	R/W	0
0	Reserved		R	0

3.3.12 Noise Detect Status register (SYS0_NDTSTS)

Address Offset: 0x2C

Bit	Name	Description	Attribute	Reset
31:2	Reserved		R	0
1	NDT5V_DET	Power noise status of NDT5V IP. 0: No power noise is detected. 1: Power noise is detected by NDT5V IP. *Cleared by write 1 to SYS0_NDTSTS[1]	R/W	0
0	Reserved		R	0

3.3.13 Anti-EFT Ability Control register (SYS0_ANTIEFT)

Address Offset: 0x30

This register decides the HW anti-EFT ability.

Bit	Name	Description	Attribute	Reset
31:3	Reserved		R	0
2:0	AEFT[2:0]	HW anti-EFT ability. 000: No 010: Low 011: Medium 100: Strong	R/W	000

3.3.14 IHRC Frequency Adjustment register (SYS0_IHRCADJ)

Address Offset: 0x34

Total 400 counts available for IHRC frequency adjusting, and each step varies between +/-0.2% from +/-0.3%.

Bit	Name	Description	Attribute	Reset
31:16	SYSKEY[15:0]	System register key Read as 0. Behavior of writing to this register is ignored unless writing 0xA5A5 to SYSKEY at the same time.	W	0
15:12	Reserved		R	0
11:4	ADJ[7:0]	IHRC frequency adjusting bits.	R/W	0

3:2	Reserved		R	0
1	DIR	IHRC frequency adjusting direction bit 0: Positive 1: Negative	R/W	0
0	ADJEN	IHRC frequency adjustment enable bit 0: Disable 1: Enable	R/W	0

3.4 SYSTEM CONTROL REGISTERS 1

Base Address: 0x4005 E000

3.4.1 AHB Clock Enable register (SYS1_AHBCLKEN)

Address Offset: 0x00

The SYS_AHBCLKEN register enables the AHB clock to individual system and peripheral blocks.

✸ ***Note:***
1. ***When the clock is disabled, the peripheral register values may not be readable by SW and the value returned is always 0x0.***
2. ***HW will replace GPIO with CLKOUT function directly if CLKOUTSEL is Not 0.***
3. ***User shall disable the AHB clock for individual peripheral to decrease power consumption by demand.***

Bit	Name	Description	Attribute	Reset
31	Reserved		R	0
30:28	CLKOUTSEL[2:0]	Clock output source 000: Disable 001: ILRC clock 010: ELS clock 100: HCLK 101: IHRC clock 110: EHS clock 111: PLL clock output Other: Disable	R/W	0
27	CRCCLKEN	Enable clock for CRC. 0: Disable 1: Enable	R/W	0
26	LCDCLKEN	Enable clock for LCD 0: Disable 1: Enable	R/W	0
25	I2S1CLKEN	Enable clock for I2S1. 0: Disable 1: Enable	R/W	0
24	WDTCLKEN	Enable clock for WDT. 0: Reserved 1: Enable	R/W	1
23	RTCCLKEN	Enable clock for RTC. 0: Disable 1: Enable	R/W	0
22	I2S0CLKEN	Enable clock for I2S0. 0: Disable 1: Enable	R/W	0
21	I2C0CLKEN	Enable clock for I2C0. 0: Disable 1: Enable	R/W	0
20	I2C1CLKEN	Enable clock for I2C1. 0: Disable 1: Enable	R/W	0
19	UART3CLKEN	Enable clock for UART3. 0: Disable 1: Enable	R/W	0
18	UART2CLKEN	Enable clock for UART2. 0: Disable 1: Enable	R/W	0
17	UART1CLKEN	Enable clock for UART1. 0: Disable 1: Enable	R/W	0

16	UART0CLKEN	Enable clock for UART0. 0: Disable 1: Enable	R/W	0
15	EBICLKEN	Enable clock for EBI. 0: Disable 1: Enable	R/W	0
14	CMPCLKEN	Enable clock for CMP. 0: Disable 1: Enable	R/W	0
13	SPI1CLKEN	Enable clock for SPI1. 0: Disable 1: Enable	R/W	0
12	SPI0CLKEN	Enable clock for SPI0. 0: Disable 1: Enable	R/W	0
11	ADCCLKEN	Enable clock for ADC. 0: Disable 1: Enable	R/W	0
10	CT16B5CLKEN	Enable clock for CT16B5. 0: Disable 1: Enable	R/W	0
9	CT16B4CLKEN	Enable clock for CT16B4. 0: Disable 1: Enable	R/W	0
8	CT16B3CLKEN	Enable clock for CT16B3. 0: Disable 1: Enable	R/W	0
7	CT16B2CLKEN	Enable clock for CT16B2. 0: Disable 1: Enable	R/W	0
6	CT16B1CLKEN	Enable clock for CT16B1. 0: Disable 1: Enable	R/W	0
5	CT16B0CLKEN	Enable clock for CT16B0. 0: Disable 1: Enable	R/W	0
4	USBCLKEN	Enable clock for USB. 0: Disable 1: Enable	R/W	0
3	OPACLKEN	Enable clock for OPA. 0: Disable 1: Enable	R/W	0
2:0	Reserved		R	0

3.4.2 APB Clock Prescale register 0 (SYS1_APBCP0)

Address Offset: 0x04

✸ ***Note: Must reset the corresponding peripheral with SYS1_PRST register after changing the prescale value.***

Bit	Name	Description	Attribute	Reset
31:19	Reserved		R	0
18:16	ADCPRE[2:0]	ADC clock source prescaler 000: HCLK / 1 001: HCLK / 2 010: HCLK / 4	R/W	0

		011: HCLK / 8 100: HCLK / 16 Other: Reserved		
15:0	Reserved		R	0

3.4.3 APB Clock Prescale register 1 (SYS1_APBCP1)

Address Offset: 0x08

✷ ***Note: Must reset the corresponding peripheral with SYS1_PRST register after changing the prescale value.***

Bit	Name	Description	Attribute	Reset
31	Reserved		R	0
30:28	CLKOUTPRE[2:0]	Clock-out source prescaler 000: Clock-out source / 1 001: Clock-out source / 2 010: Clock-out source / 4 011: Clock-out source / 8 100: Clock-out source / 16 101: Clock-out source / 32 110: Clock-out source / 64 111: Clock-out source / 128	R/W	0
27	Reserved		R	0
26:24	I2C1PRE[2:0]	I2C1 clock source prescaler 000: HCLK / 1 001: HCLK / 2 010: HCLK / 4 011: HCLK / 8 100: HCLK / 16 Other: Reserved	W	0
23	Reserved		R	0
22:20	WDTPRE[2:0]	WDT clock source prescaler 000: WDT_PCLK = WDT clock source / 1 001: WDT_PCLK = WDT clock source / 2 010: WDT_PCLK = WDT clock source / 4 011: WDT_PCLK = WDT clock source / 8 100: WDT_PCLK = WDT clock source / 16 101: WDT_PCLK = WDT clock source / 32 Other: Reserved	R/W	0
19:18	Reserved		R	0
17:15	I2S1PRE[2:0]	I2S1 clock source prescaler 000: HCLK / 1 001: HCLK / 2 010: HCLK / 4 011: HCLK / 8 100: HCLK / 16 111: HCLK / 3 Other: Reserved	R/W	0
14:12	I2S0PRE[2:0]	I2S0 clock source prescaler 000: HCLK / 1 001: HCLK / 2 010: HCLK / 4 011: HCLK / 8 100: HCLK / 16	R/W	0

		111: HCLK / 3 Other: Reserved		
11	Reserved		R	0
10:8	I2C0PRE[2:0]	I2C0 clock source prescaler 000: HCLK / 1 001: HCLK / 2 010: HCLK / 4 011: HCLK / 8 100: HCLK / 16 Other: Reserved	W	0
7:0	Reserved		R	0

3.4.4 Peripheral Reset register (SYS1_PRST)

Address Offset: 0x10

Bit	Name	Description	Attribute	Reset
31:29	Reserved		R	0
28	OPARST	OPA reset. 0: No effect 1: Reset OPA	R/W	0
27	Reserved		R	0
26	CRCRST	CRC reset 0: No effect 1: Reset CRC	R/W	0
25	I2S1RST	I2S1 reset 0: No effect 1: Reset I2S1	R/W	0
24	WDTRST	WDT reset 0: No effect 1: Reset WDT	R/W	0
23	RTCRST	RTC reset 0: No effect 1: Reset RTC	R/W	0
22	I2S0RST	I2S0 reset 0: No effect 1: Reset I2S0	R/W	0
21	I2C0RST	I2C0 reset 0: No effect 1: Reset I2C0	R/W	0
20	I2C1RST	I2C1 reset 0: No effect 1: Reset I2C1	R/W	0
19	UART3RST	UART3 reset 0: No effect 1: Reset UART3	R/W	0
18	UART2RST	UART2 reset 0: No effect 1: Reset UART2	R/W	0
17	UART1RST	UART1 reset 0: No effect 1: Reset UART1	R/W	0
16	UART0RST	UART0 reset 0: No effect 1: Reset UART0	R/W	0
15	LCDRST	LCD reset 0: No effect 1: Reset LCD	R/W	0

14	CMPRST	CMP reset 0: No effect 1: Reset CMP	R/W	0
13	SPI1RST	SPI1 reset 0: No effect 1: Reset SPI1	R/W	0
12	SPI0RST	SPI0 reset 0: No effect 1: Reset SPI0	R/W	0
11	ADCRST	ADC reset 0: No effect 1: Reset ADC	R/W	0
10	CT16B5RST	CT16B5 reset 0: No effect 1: Reset CT16B5	R/W	0
9	CT16B4RST	CT16B4 reset 0: No effect 1: Reset CT16B4	R/W	0
8	CT16B3RST	CT32B0 reset 0: No effect 1: Reset CT32B0	R/W	0
7	CT16B2RST	CT16B2 reset 0: No effect 1: Reset CT16B2	R/W	0
6	CT16B1RST	CT16B1 reset 0: No effect 1: Reset CT16B1	R/W	0
5	CT16B0RST	CT16B0 reset 0: No effect 1: Reset CT16B0	R/W	0
4	EBIRST	EBI reset 0: No effect 1: Reset EBI	R/W	0
3	GPIOP3RST	GPIO port 3 reset 0: No effect 1: Reset GPIO port 3	R/W	0
2	GPIOP2RST	GPIO port 2 reset 0: No effect 1: Reset GPIO port 2	R/W	0
1	GPIOP1RST	GPIO port 1 reset 0: No effect 1: Reset GPIO port 1	R/W	0
0	GPIOP0RST	GPIO port 0 reset 0: No effect 1: Reset GPIO port 0	R/W	0

4 SYSTEM OPERATION MODE

4.1 OVERVIEW

The chip builds in four operating mode for difference clock rate and power saving reason. These modes control oscillators, op-code operation and analog peripheral devices' operation.

- Normal mode
- Sleep mode
- Deep sleep mode

4.2 NORMAL MODE

In Normal mode, the ARM Cortex-M0 core, memories, and peripherals are clocked by the system clock. The SYS1_AHBCLKEN register controls which peripherals are running.

Selected peripherals have individual peripheral clocks with their own clock dividers in addition to the system clock. The peripheral clocks can be disabled respectively.

The power to various analog blocks (IHRC, EHS X'TAL, ELS X'TAL, PLL, Flash, LVD, ADC) can be controlled at any time individually through the enable bit of all blocks.

4.3 LOW-POWER MODES

There are three special modes of processor power reduction: Sleep mode, and Deep-sleep mode. The PMU_CTRL register controls which mode is desired.

The CPU clock rate may also be controlled as needed by changing clock sources, re-configuring PLL values, and/or altering the system clock divider value. This allows a trade-off of power versus processing speed based on application requirements.

Run-time power control allows disable the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider for power control.

✷ ***Note:***

1. ***The debug mode is not supported in Deep-sleep mode.***
2. ***The pins which are not pin-out shall be set correctly to decrease power consumption in low-power modes.*** **Strongly recommended to set these pins as input pull-up.**

4.3.1 SLEEP MODE

In Sleep mode, the system clock to the ARM Cortex-M0 core is stopped and execution of instructions is suspended.

Peripheral functions, if selected to be clocked in SYS1_AHBCLKEN register, continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

The power state of the analog blocks (IHRC, EHS X'TAL, ELS X'TAL, PLL, Flash, LVD, ADC) is determined by the enable bit of all blocks.

The processor state and registers, peripheral registers, and internal SRAM values are maintained and the logic levels of the pins remain static.

The pins of Port 2 configured as ADC input channel must be set as input mode, inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low) with GPIO2_MODE and GPIO2_CFG register by program to avoid current leakage.

Wake up the chip from Sleep mode by an interrupt occurs.

The RESET pin has keep functionality in Sleep mode.

The Sleep mode is entered by using the following steps:
1. Write 4 to PMU_CTRL register.
2. Execute ARM Cortex-M0 WFI instruction.

4.3.2 DEEP-SLEEP MODE

In Deep-sleep mode, the system clock to the ARM Cortex-M0 core is stopped, and execution of instructions is suspended.

The clock to the peripheral functions are stopped because the power state of oscillators are powered down, the clock source are stopped, except RTC or LCD low speed clock source (ELS X'TAL, ILRC) if used.

✸ ***Note: User SHALL decide to power down low speed clock source (ELS X'TAL, ILRC oscillator) or not if RTC or LCD is enabled.***

The processor state and registers, peripheral registers, and internal SRAM values are maintained and the logic levels of the pins remain static.

All GPIO pins are served as wakeup pins. The user must program the GPIO registers for each pin to set the appropriate edge polarity for the corresponding wakeup event, only edge sensitive is supported to wakeup MCU. The system will exit Deep-sleep mode when GPIO indicates a GPIO interrupt to the ARM core. Furthermore, the interrupts corresponding to each input must be enabled in the NVIC.

✸ ***Note: Strongly recommended to set the GPIO wake-up condition to both edge sensing.***

The RESET pin has keep functionality in Deep-sleep mode.

The Deep-sleep mode is entered by using the following steps:
1. Write 2 to PMU_CTRL register.
2. Execute ARM WFI instruction.

The advantage of the Deep-sleep mode is that can power down clock generating blocks such as oscillators and PLL, thereby gaining far greater dynamic power savings over Sleep mode. In addition, the Flash can be powered down in Deep-sleep mode resulting in savings in static leakage power, however at the expense of longer wake-up times for the Flash memory.

4.4 WAKEUP

4.4.1 OVERVIEW

Under low power mode, program doesn't execute. The wakeup trigger can wake the system up to normal mode. The wakeup function builds in interrupt operation and trigger system executing interrupt service routine as system wakeup occurrence.

- The wakeup trigger sources of the Sleep mode are all interrupts and the RESET pin.
- The wakeup trigger sources of the Deep-sleep mode are the GPIO interrupt, RTC interrupt, LCD interrupt, and the RESET pin.

4.4.2 WAKEUP TIME

When the system is in Sleep mode, the high clock is enabled or disabled by F/W. If the high clock stops and MCU is waken up from Sleep mode, MCU waits for 2048 external high-speed oscillator clocks and 32 internal high-speed oscillator clocks as the wakeup time to stable the oscillator circuit. After the wakeup time, the system goes into the normal mode.

✸ ***Note: Wakeup from Sleep mode spends NO wakeup time if the clock doesn't stop.***

When the system is in Deep-sleep mode, the high clock will stop. When MCU is waken up from Deep-sleep mode, MCU waits for 10us and IHRC/EHS warm up time (32T*IHRC/2048T*EHS). After the wakeup time, the system goes into the normal mode.

The value of the external high clock oscillator wakeup time from Deep sleep mode is as the following.

The total Wakeup time of EHS X'tal = 10us + 1/F_{EHS} * 2048 (sec) + high clock start-up time

- Example: F_{EHS}=20MHz, the wakeup time from Deep sleep mode is as the following.

  The total Wakeup time = 10us + 1/F_{EHS} * 2048 + oscillator start-up time

  = 112.4 us + oscillator start-up time (F_{EHS} = 20MHz)

The value of the IHRC wakeup time is as the following.

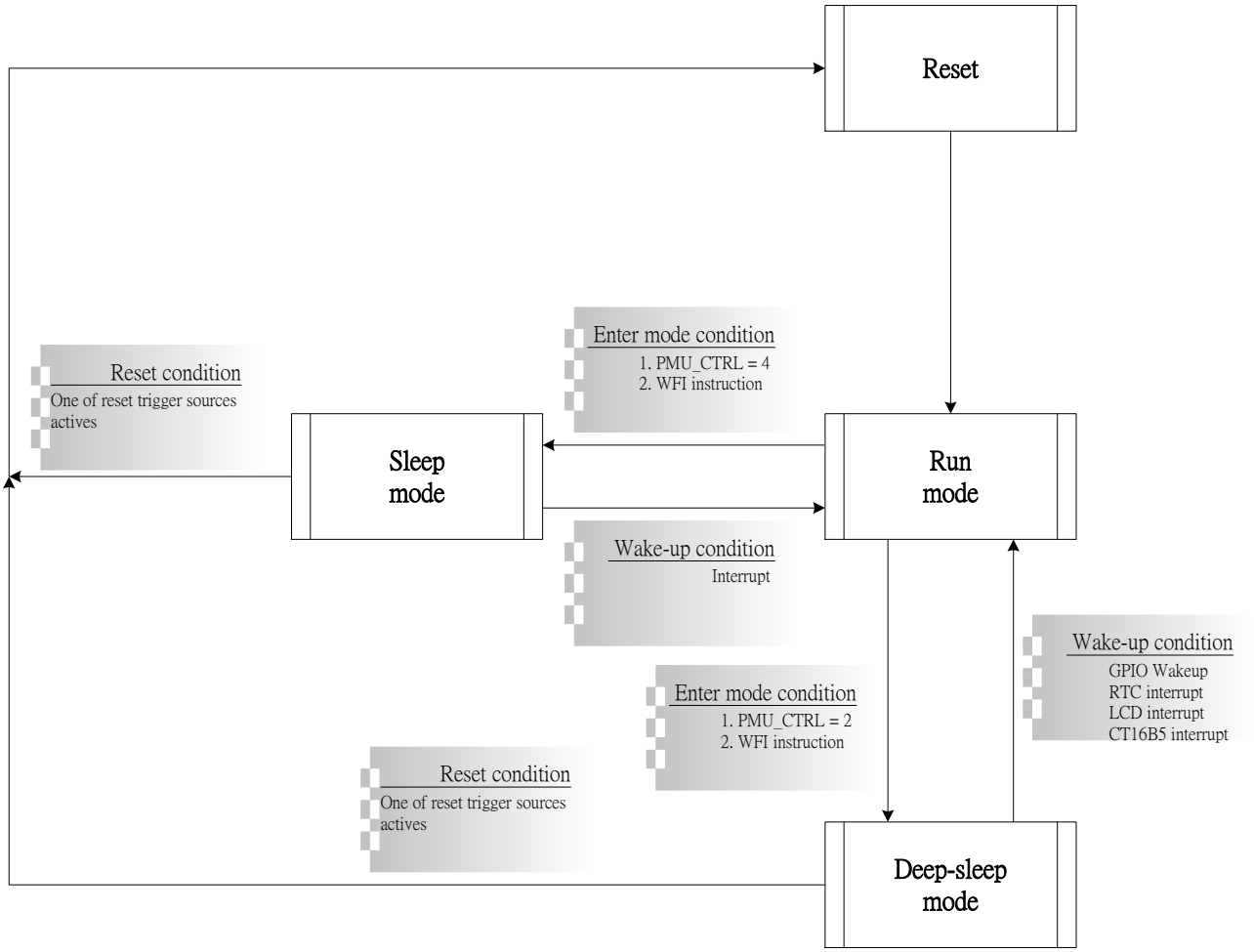
The total Wakeup time of IHRC = 10us + 1/F_{IHRC} * 32 (sec)

- Example: F_{IHRC}=12MHz, the wakeup time is as the following.

  The total Wakeup time = 10us + 1/F_{IHRC} * 32 = 12.67 us (F_{IHRC} = 12MHz)

✸ ***Note: The high clock start-up time is depended on the VDD and oscillator type of high clock.***

4.5 STATE MACHINE OF PMU



4.6 OPERATION MODE COMPARISON TABLE

Operation Mode	Normal Mode	Low-Power Mode	
		Sleep Mode	Deep-Sleep Mode
IHRC	By IHRCEN		Disable
ILRC	ON		Enable if used as clock source of LCD/RTC
EHS X'TAL	By EHSEN		Disable
ELS X'TAL	By ELSEN		Enable if used as clock source of LCD/RTC/CT16B5
PLL	By PLLEN		Disable
Cortex-M0	Running	Stop	Stop
Flash ROM	Enable	Disable	Disable
RAM	Enable	Maintain	Maintain
USB	By USBEN		Disable
ADC	By ADENB		Disable
LVD	By LVDEN		Disable
LCD	By LCDENB		By LCDENB
RTC	By RTCEN		By RTCEN
CMP	By CMnEN & CMnMODE		Disable
OPA	By OPnEN		Disable
Peripherals	By Enable bit of each peripherals		Disable HCLK
IO status	-	Maintained	Maintained
Wakeup Source	N/A	All interrupts, RESET pin	GPIO interrupt, CT16B5 interrupt, RTC interrupt, LCD interrupt, RESET pin

4.7 PMU REGISTERS

Base Address: 0x4003 2000

4.7.1 Power Control register (PMU_CTRL)

Address Offset: 0x40

The power control register selects whether one of the ARM Cortex-M0 controlled power-down modes (Sleep mode or Deep-sleep mode) and provides the flags respectively.

✸ ***Note: The pins which are not pin-out shall be set correctly to decrease power consumption in low-power modes.*** **Strongly recommended to set these pins as input pull-up.**

Bit	Name	Description	Attribute	Reset
31:3	Reserved		R	0
2:0	MODE[2:0]	Low power mode selection 000: Disable. 010: WFI instruction will make MCU enter Deep-sleep mode. 100: WFI instruction will make MCU enter Sleep mode. Other: Reserved	R/W	0

5 GENERAL PURPOSE I/O PORT (GPIO)

5.1 OVERVIEW

Digital ports can be configured input/output by SW.

- Each individual port pin can serve as external interrupt input pin.
- Interrupts can be configured on single falling or rising edges and on both edges.
- The I/O configuration registers control the electrical characteristics of the pads.
- Internal pull-up/pull-down resistor.
- Most of the I/O pins are mixed with analog pins and special function pins.

5.2 GPIO MODE

All GPIO pins are inputs and floating by default. The MODE bits in the GPIOn_CFG (n=0,1,2,3) register allow the selection of on-chip pull-up or pull-down resistors for each pin or select the repeater mode.

5.3 GPIO REGISTERS

Base Address: 0x4004 4000 (GPIO 0)
0x4004 6000 (GPIO 1)
0x4004 8000 (GPIO 2)
0x4004 A000 (GPIO 3)

5.3.1 GPIO Port n Data register (GPIOn_DATA) (n=0,1,2,3)

Address offset: 0x00

Bit	Name	Description	Attribute	Reset
31:20	Reserved		R	0
19:0	DATA[19:0]	Input data (read) or output data (write) for Pn.0 to Pn.19	R/W	0

5.3.2 GPIO Port n Mode register (GPIOn_MODE) (n=0,1,2,3)

Address offset: 0x04

✷ ***Note: HW will switch I/O Mode directly when Specific function (Peripheral, ADC) is enabled, not through GPIOn_MODE register.***

Bit	Name	Description	Attribute	Reset
31:20	Reserved		R	0
19:0	MODE[19:0]	Select pin x as input or output (x = 0 to 19) 0: Pn.x is configured as input 1: Pn.x is configured as output.	R/W	0

5.3.3 GPIO Port n Configuration register (GPIOn_CFG) (n=0,1,2,3)

Address offset: 0x08

Reset value: 0xAAAAAAAA

✷ ***Note: HW will switch I/O Mode directly when Specific function (Peripheral, ADC) is enabled, not through GPIOn_MODE register.***

Bit	Name	Description	Attribute	Reset
31:30	CFG15[1:0]	Configuration of Pn.15 00: Pull-up resistor enabled. 01: Reserved 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)	R/W	10b
29:28	CFG14[1:0]	Configuration of Pn.14 00: Pull-up resistor enabled. 01: Reserved 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger	R/W	10b

		enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)		
27:26	CFG13[1:0]	Configuration of Pn.13 00: Pull-up resistor enabled. 01: Reserved (n=0,1,2) / Pull-down resistor enabled (n=3) 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)	R/W	10b
25:24	CFG12[1:0]	Configuration of Pn.12 00: Pull-up resistor enabled. 01: Reserved (n=0,1,2) / Pull-down resistor enabled (n=3) 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)	R/W	10b
23:22	CFG11[1:0]	Configuration of Pn.11 00: Pull-up resistor enabled. 01: Reserved (n=0,1,2) / Pull-down resistor enabled (n=3) 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)	R/W	10b
21:20	CFG10[1:0]	Configuration of Pn.10 00: Pull-up resistor enabled. 01: Reserved (n=0,1,2) / Pull-down resistor enabled (n=3) 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)	R/W	10b
19:18	CFG9[1:0]	Configuration of Pn.9 00: Pull-up resistor enabled. 01: Reserved 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)	R/W	10b
17:16	CFG8[1:0]	Configuration of Pn.8 00: Pull-up resistor enabled. 01: Reserved 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)	R/W	10b
15:14	CFG7[1:0]	Configuration of Pn.7 00: Pull-up resistor enabled. 01: Reserved 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)	R/W	10b
13:12	CFG6[1:0]	Configuration of Pn.6 00: Pull-up resistor enabled. 01: Reserved 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)	R/W	10b
11:10	CFG5[1:0]	Configuration of Pn.5 00: Pull-up resistor enabled. 01: Reserved 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)	R/W	10b

9:8	CFG4[1:0]	Configuration of Pn.4 00: Pull-up resistor enabled. 01: Reserved 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)	R/W	10b
7:6	CFG3[1:0]	Configuration of Pn.3 00: Pull-up resistor enabled. 01: Reserved 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)	R/W	10b
5:4	CFG2[1:0]	Configuration of Pn.2 00: Pull-up resistor enabled. 01: Reserved 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)	R/W	10b
3:2	CFG1[1:0]	Configuration of Pn.1 00: Pull-up resistor enabled. 01: Reserved 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)	R/W	10b
1:0	CFG0[1:0]	Configuration of Pn.0 00: Pull-up resistor enabled. 01: Reserved 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)	R/W	10b

5.3.4 GPIO Port n Interrupt Sense register (GPIOn_IS) (n=0,1,2,3)

Address offset: 0x0C

Bit	Name	Description	Attribute	Reset
31:20	Reserved		R	0
19:0	IS[19:0]	Select the interrupt on pin x as level or edge sensitive (x = 0 to 19). 0: Interrupt on Pn.x is configured as edge sensitive. 1: Interrupt on Pn.x is configured as event sensitive.	R/W	0

5.3.5 GPIO Port n Interrupt Both-edge Sense register (GPIOn_IBS) (n=0,1,2,3)

Address offset: 0x10

Bit	Name	Description	Attribute	Reset
31:20	Reserved		R	0
19:0	IBS[19:0]	Select the interrupt on Pn.x to be triggered on both edges (x = 0 to 19). 0: Interrupt on Pn.x is controlled through register GPIOn_IEV. 1: Both edges on Pn.x trigger an interrupt.	R/W	0

5.3.6 GPIO Port n Interrupt Event register (GPIOn_IEV) (n=0,1,2,3)

Address offset: 0x14

Bit	Name	Description	Attribute	Reset
31:20	Reserved		R	0
19:0	IEV[19:0]	Select the interrupt on pin x to be triggered rising or falling edges (x = 0 to 19). 0: Depending on setting in register GPIOn_IS, Rising edges or HIGH level on Pn.x trigger an interrupt. 1: Depending on setting in register GPIOn_IS, Falling edges or LOW level on Pn.x trigger an interrupt.	R/W	0

5.3.7 GPIO Port n Interrupt Enable register (GPIOn_IE) (n=0,1,2,3)

Address offset: 0x18

Bits set to HIGH in the GPIOn_IE register allow the corresponding pins to trigger their individual interrupts. Clearing a bit disables interrupt triggering on that pin.

Bit	Name	Description	Attribute	Reset
31:20	Reserved		R	0
19:0	IE[19:0]	Select the interrupt on pin x to be enabled (x = 0 to 19). 0: Disable Interrupt on Pn.x 1: Enable Interrupt on Pn.x	R/W	0

5.3.8 GPIO Port n Raw Interrupt Status register (GPIOn_RIS) (n=0,1,2,3)

Address offset: 0x1C

This register indicates the status for GPIO control raw interrupts. A GPIO interrupt is sent to the interrupt controller if the corresponding bit in GPIOn_IE register is set.

Bit	Name	Description	Attribute	Reset
31:20	Reserved		R	0
19:0	IF[19:0]	GPIO raw interrupt flag (x = 0 to 19). 0: No interrupt on Pn.x 1: Interrupt requirements met on Pn.x.	R	0

5.3.9 GPIO Port n Interrupt Clear register (GPIOn_IC) (n=0,1,2,3)

Address offset: 0x20

Bit	Name	Description	Attribute	Reset
31:20	Reserved		R	0
19:0	IC[19:0]	Select the interrupt flag on pin x to be cleared (x = 0 to 19). 0: No effect 1: Clear interrupt flag on Pn.x	W	0

5.3.10 GPIO Port n Bits Set Operation register (GPIOn_BSET) (n=0,1,2,3)

Address offset: 0x24

In order for SW to set GPIO bits without affecting any other pins in a single write operation, the GPIO bit is set if the corresponding bit in the GPIOn_BSET register is set.

Bit	Name	Description	Attribute	Reset
31:20	Reserved		R	0
19:0	BSET[19:0]	Bit Set enable (x = 0 to 19) 0: No effect on Pn.x 1: Set Pn.x to "1"	W	0

5.3.11 Port n Bits Clear Operation register (GPIOn_BCLR) (n=0,1,2,3)

Address offset: 0x28

In order for SW to clear GPIO bits without affecting any other pins in a single write operation, the GPIO bit is cleared if the corresponding bit in this register is set.

Bit	Name	Description	Attribute	Reset
31:20	Reserved		R	0
19:0	BCLR[19:0]	Bit clear enable (x = 0 to 19) 0: No effect on Pn.x 1: Clear Pn.x.	W	0

5.3.12 GPIO Port n Configuration register 1 (GPIOn_CFG1) (n=0,1,3)

Address offset: 0x30

Reset value: 0x000000AA

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7:6	CFG19[1:0]	Configuration of Pn.19 00: Pull-up resistor enabled. 01: Reserved 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)	R/W	10b
5:4	CFG18[1:0]	Configuration of Pn.18 00: Pull-up resistor enabled. 01: Reserved 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)	R/W	10b
3:2	CFG17[1:0]	Configuration of Pn.17 00: Pull-up resistor enabled. 01: Reserved 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)	R/W	10b
1:0	CFG16[1:0]	Configuration of Pn.16 00: Pull-up resistor enabled. 01: Reserved 10: Inactive (no pull-down/up resistor enabled, Schmitt trigger enabled). 11: Inactive (no pull-down/up resistor enabled, Schmitt trigger disabled, Data register keep low)	R/W	10b

6 PERIPHERAL FUNCTION PIN ASSIGNMENT (PFPA)

6.1 OVERVIEW

PFPA registers are used to provide flexible assignment of digital peripheral functions to desired external pins of different packages.

6.2 FEATURES

- Flexible assignment of digital peripheral functions to desired pins.
- Supported functions are UART, I2C, SPI, I2S, Capture, and PWM.

6.3 PIN ASSIGNMENT LIST

Peripheral	Pin Name	PA0	PA1	PA2	PA3
UART0	URXD0	P0.11	P2.0	P3.2	
	UTXD0	P0.10	P2.1	P3.1	
UART1	URXD1	P1.8	P2.3	P1.17	
	UTXD1	P1.9	P2.2	P1.16	P3.6
UART2	URXD2	P0.2	P1.3	P2.15	P1.6
	UTXD2	P0.1	P1.4	P2.14	P1.7
UART3	URXD3	P3.13	P1.6	P2.1	
	UTXD3	P3.12	P1.7	P2.0	
SPI0	SCK0	P0.0	P2.5	P1.0	P3.0
	SEL0	P0.1	P2.4	P1.8	P1.7
	MISO0	P0.2	P2.6	P1.1	P3.1
	MOSI0	P0.3	P2.7	P1.2	P3.2
SPI1	SCK1	P1.13	P1.8	P0.1	P0.12
	SEL1	P1.12	P1.9	P1.5	P0.13
	MISO1	P1.14	P1.10	P2.12	P3.14
	MOSI1	P1.15	P1.11	P2.13	P3.15
I2C0	SCL0	P0.6	P1.4	P0.10	P1.1
	SDA0	P0.7	P1.5	P0.11	P1.2
I2C1	SCL1	P1.10	P1.13	P0.1	P1.8
	SDA1	P1.11	P1.14	P0.2	P1.9
I2S0	MCLK0	P3.0	P2.6	P1.1	
	BCLK0	P3.1	P2.5	P1.0	
	WS0	P3.2	P2.4	P1.8	
	DOUT0		P2.7	P1.2	
	DIN0		P2.8	P1.3	

I2S1	MCLK1	P3.14	P1.7	P1.14	P2.12
	BCLK1	P3.17	P1.6	P1.13	P0.1
	WS1	P3.16	P1.5	P1.12	P1.9
	DOUT1	P3.15	P1.2	P1.15	P2.13
	DIN1	P3.18	P1.1	P1.19	P1.10
CT16B0	PWM0	P0.2	P3.0	P2.6	P1.12
	PWM0N	P0.3	P1.13	P2.7	P0.12
	PWM1	P2.9	P3.1	P0.1	P2.5
	PWM1N	P1.14	P0.0	P2.8	P2.4
	PWM2	P2.7	P3.2	P0.0	P2.8
	PWM2N	P1.15	P2.6	P2.9	P0.1
	PWM3	P0.1		P0.3	P2.14
	PWM3N	P0.0	P1.16	P0.2	P2.15
CT16B1	PWM0	P0.0	P1.8		
	PWM1	P0.1	P1.9		
	PWM2	P0.2	P1.10		
	PWM3	P0.3	P1.11		
	PWM4	P0.4	P1.12		
	PWM5	P0.5	P1.13		
	PWM6	P0.6	P1.14		
	PWM7	P0.7	P1.15		
	PWM8	P0.8	P2.0		
	PWM9	P0.9	P2.4		
	PWM10	P0.10	P2.7		
	PWM11	P0.11	P2.9		
CT16B2	PWM0	P2.0	P2.5	P1.8	P0.0
	PWM1	P2.1	P1.0	P1.7	P0.3
	PWM2	P2.2	P0.1	P1.6	P1.18
	PWM3	P2.3	P0.2	P1.10	P1.17
CT16B3	PWM0	P1.14	P2.2	P2.6	P1.4
	PWM0N	P1.15	P2.1	P0.10	P1.3
	PWM1	P2.3	P1.15	P1.12	P1.5
	PWM1N	P2.4	P0.11	P1.13	P0.8
CT16B4	PWM0	P2.7	P1.5	P0.10	P0.9
	PWM0N	P0.11	P2.6	P1.2	P0.8
	PWM1	P2.6	P1.4	P2.5	P1.12
	PWM1N	P0.10	P1.3	P2.4	P1.13
CT16B5	PWM0	P2.6	P0.15	P1.1	P3.16
	PWM1	P2.7	P0.14	P1.2	P3.17
	PWM2	P2.8	P0.13	P1.0	P3.18

	PWM3	P2.9	P0.12	P1.18	P3.19

6.4 PFPA REGISTERS

Base Address: 0x4004 2000

6.4.1 PFPA for CT16B0 register (PFPA_CT16B0)

Address offset: 0x00

Bit	Name	Description	Attribute	Reset
31:16	Reserved		R	0
15:14	PWM3N[1:0]	Pin to be assigned as CT16B0_PWM3N 00: P0.0 01: P1.16 10: P0.2 11: P2.15	R/W	0
13:12	PWM3[1:0]	Pin to be assigned as CT16B0_PWM3. 00: P0.1 01: Reserved 10: P0.3 11: P2.14	R/W	0
11:10	PWM2N[1:0]	Pin to be assigned as CT16B0_PWM2N 00: P1.15 01: P2.6 10: P2.9 11: P0.1	R/W	0
9:8	PWM2[1:0]	Pin to be assigned as CT16B0_PWM2. 00: P2.7 01: P3.2 10: P0.0 11: P2.8	R/W	0
7:6	PWM1N[1:0]	Pin to be assigned as CT16B0_PWM1N. 00: P1.14 01: P0.0 10: P2.8 11: P2.4	R/W	0
5:4	PWM1[1:0]	Pin to be assigned as CT16B0_PWM1. 00: P2.9 01: P3.1 10: P0.1 11: P2.5	R/W	0
3:2	PWM0N[1:0]	Pin to be assigned as CT16B0_PWM0N. 00: P0.3 01: P1.13 10: P2.7 11: P0.12	R/W	0
1:0	PWM0[1:0]	Pin to be assigned as CT16B0_PWM0. 00: P0.2 01: P3.0 10: P2.6 11: P1.12	R/W	0

6.4.2 PFPA for CT16B1 register (PFPA_CT16B1)

Address offset: 0x04

Bit	Name	Description	Attribute	Reset
31:12	Reserved		R	0

11	PWM11	Pin to be assigned as CT16B1_PWM11. 0: P0.11 1: P2.9	R/W	0
10	PWM10	Pin to be assigned as CT16B1_PWM10. 0: P0.10 1: P2.7	R/W	0
9	PWM09	Pin to be assigned as CT16B1_PWM09. 0: P0.9 1: P2.4	R/W	0
8	PWM08	Pin to be assigned as CT16B1_PWM08. 0: P0.8 1: P2.0	R/W	0
7	PWM07	Pin to be assigned as CT16B1_PWM07. 0: P0.7 1: P1.15	R/W	0
6	PWM06	Pin to be assigned as CT16B1_PWM06. 0: P0.6 1: P1.14	R/W	0
5	PWM05	Pin to be assigned as CT16B1_PWM05. 0: P0.5 1: P1.13	R/W	0
4	PWM04	Pin to be assigned as CT16B1_PWM04. 0: P0.4 1: P1.12	R/W	0
3	PWM03	Pin to be assigned as CT16B1_PWM03. 0: P0.3 1: P1.11	R/W	0
2	PWM02	Pin to be assigned as CT16B1_PWM02. 0: P0.2 1: P1.10	R/W	0
1	PWM01	Pin to be assigned as CT16B1_PWM01. 0: P0.1 1: P1.9	R/W	0
0	PWM00	Pin to be assigned as CT16B1_PWM00. 0: P0.0 1: P1.8	R/W	0

6.4.3 PFPA for UART register (PFPA_UART)

Address offset: 0x08

Bit	Name	Description	Attribute	Reset
31:16	Reserved		R	0
15:14	URXD3[1:0]	Pin to be assigned as URXD3. 00: P3.13 01: P1.6 10: P2.1 11: Reserved	R/W	0
13:12	UTXD3[1:0]	Pin to be assigned as UTXD3. 00: P3.12 01: P1.7 10: P2.0 11: Reserved	R/W	0
11:10	URXD2[1:0]	Pin to be assigned as URXD2. 00: P0.2 01: P1.3 10: P2.15 11: P1.6	R/W	0
9:8	UTXD2[1:0]	Pin to be assigned as UTXD2. 00: P0.1 10: P1.4 10: P2.14	R/W	0

		11: P1.7		
7:6	URXD1[1:0]	Pin to be assigned as URXD1. 00: P1.8 01: P2.3 10: P1.17 11: Reserved	R/W	0
5:4	UTXD1[1:0]	Pin to be assigned as UTXD1. 00: P1.9 01: P2.2 10: P1.16 11: P3.6	R/W	0
3:2	URXD0[1:0]	Pin to be assigned as URXD0. 00: P0.11 01: P2.0 10: P3.2 11: Reserved	R/W	0
1:0	UTXD0[1:0]	Pin to be assigned as UTXD0. 00: P0.10 01: P2.1 10: P3.1 11: Reserved	R/W	0

6.4.4 PFPA for I2C register (PFPA_I2C)

Address offset: 0x0C

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7:6	SCL1[1:0]	Pin to be assigned as SCL1. 00: P1.10 01: P1.13 10: P0.1 11: P1.8	R/W	0
5:4	SDA1[1:0]	Pin to be assigned as SDA1. 00: P1.11 01: P1.14 10: P0.2 11: P1.9	R/W	0
3:2	SCL0[1:0]	Pin to be assigned as SCL0. 00: P0.6 01: P1.4 10: P0.10 11: P1.1	R/W	0
1:0	SDA0[1:0]	Pin to be assigned as SDA0. 00: P0.7 01: P1.5 10: P0.11 11: P1.2	R/W	0

6.4.5 PFPA for SPI register (PFPA_SPI)

Address offset: 0x10

Bit	Name	Description	Attribute	Reset
31:16	Reserved		R	0
15:14	SEL1[1:0]	Pin to be assigned as SEL1. 00: P1.12 01: P1.9 10: P1.5	R/W	0

		11: P0.13		
13:12	SCK1[1:0]	Pin to be assigned as SCK1. 00: P1.13 01: P1.8 10: P0.1 11: P0.12	R/W	0
11:10	MOSI1[1:0]	Pin to be assigned as MOSI1. 00: P1.15 01: P1.11 10: P2.13 11: P3.15	R/W	0
9:8	MISO1[1:0]	Pin to be assigned as MISO1. 00: P1.14 01: P1.10 10: P2.12 11: P3.14	R/W	0
7:6	SEL0[1:0]	Pin to be assigned as SEL0. 00: P0.1 01: P2.4 10: P1.8 11: P1.7	R/W	0
5:4	SCK0[1:0]	Pin to be assigned as SCK0. 00: P0.0 01: P2.5 10: P1.0 11: P3.0	R/W	0
3:2	MOSI0[1:0]	Pin to be assigned as MOSI0. 00: P0.3 01: P2.7 10: P1.2 11: P3.2	R/W	0
1:0	MISO0[1:0]	Pin to be assigned as MISO0. 00: P0.2 01: P2.6 10: P1.1 11: P3.1	R/W	0

6.4.6 PFPA for I2S register (PFPA_I2S)

Address offset: 0x14

Bit	Name	Description	Attribute	Reset
31:20	Reserved		R	0
19:18	DIN1[1:0]	Pin to be assigned as DIN1. 00: P3.18 01: P1.1 10: P1.19 11: P1.10	R/W	0
17:16	DOUT1[1:0]	Pin to be assigned as DOUT1. 00: P3.15 01: P1.2 10: P1.15 11: P2.13	R/W	0
15:14	WS1[1:0]	Pin to be assigned as WS1. 00: P3.16 01: P1.5 10: P1.12 11: P1.9	R/W	0
13:12	BCLK1[1:0]	Pin to be assigned as BCLK1. 00: P3.17 01: P1.6 10: P1.13 11: P0.1	R/W	0

11:10	MCLK1[1:0]	Pin to be assigned as MCLK1. 00: P3.14 01: P1.7 10: P1.14 11: P2.12	R/W	0
9:8	DIN0[1:0]	Pin to be assigned as DIN0. 00: Reserved 01: P2.8 10: P1.3 11: Reserved	R/W	0
7:6	DOUT0[1:0]	Pin to be assigned as DOUT0. 00: Reserved 01: P2.7 10: P1.2 11: Reserved	R/W	0
5:4	WS0[1:0]	Pin to be assigned as WS0. 00: P3.2 01: P2.4 10: P1.8 11: Reserved	R/W	0
3:2	BCLK0[1:0]	Pin to be assigned as BCLK0. 00: P3.1 01: P2.5 10: P1.0 11: Reserved	R/W	0
1:0	MCLK0[1:0]	Pin to be assigned as MCLK0. 00: P3.0 01: P2.6 10: P1.1 11: Reserved	R/W	0

6.4.7 PFPA for CT16B2 register (PFPA_CT16B2)

Address offset: 0x18

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7:6	PWM3[1:0]	Pin to be assigned as CT16B2_PWM3. 00: P2.3 01: P0.2 10: P1.10 11: P1.17	R/W	0
5:4	PWM2[1:0]	Pin to be assigned as CT16B2_PWM2. 00: P2.2 01: P0.1 10: P1.6 11: P1.18	R/W	0
3:2	PWM1[1:0]	Pin to be assigned as CT16B2_PWM1. 00: P2.1 01: P1.0 10: P1.7 11: P0.3	R/W	0
1:0	PWM0[1:0]	Pin to be assigned as CT16B2_PWM0. 00: P2.0 01: P2.5 10: P1.8 11: P0.0	R/W	0

6.4.8 PFPA for CT16B3 register (PFPA_CT16B3)

Address offset: 0x1C

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7:6	PWM1N[1:0]	Pin to be assigned as CT16B3_PWM1N. 00: P2.4 01: P0.11 10: P1.13 11: P0.8	R/W	0
5:4	PWM1[1:0]	Pin to be assigned as CT16B3_PWM1. 00: P2.3 01: P1.15 10: P1.12 11: P1.5	R/W	0
3:2	PWM0N[1:0]	Pin to be assigned as CT16B3_PWM0N. 00: P1.15 01: P2.1 10: P0.10 11: P1.3	R/W	0
1:0	PWM0[1:0]	Pin to be assigned as CT16B3_PWM0. 00: P1.14 01: P2.2 10: P2.6 11: P1.4	R/W	0

6.4.9 PFPA for CT16B4 register (PFPA_CT16B4)

Address offset: 0x20

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7:6	PWM1N[1:0]	Pin to be assigned as CT16B4_PWM1N. 00: P0.10 01: P1.3 10: P2.4 11: P1.13	R/W	0
5:4	PWM1[1:0]	Pin to be assigned as CT16B4_PWM1. 00: P2.6 01: P1.4 10: P2.5 11: P1.12	R/W	0
3:2	PWM0N[1:0]	Pin to be assigned as CT16B4_PWM0N. 00: P0.11 01: P2.6 10: P1.2 11: P0.8	R/W	0
1:0	PWM0[1:0]	Pin to be assigned as CT16B4_PWM0. 00: P2.7 01: P1.5 10: P0.10 11: P0.9	R/W	0

6.4.10 PFPA for CT16B5 register (PFPA_CT16B5)

Address offset: 0x24

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7:6	PWM3[1:0]	Pin to be assigned as CT16B5_PWM3. 00: P2.9 01: P0.12 10: P1.18 11: P3.19	R/W	0
5:4	PWM2[1:0]	Pin to be assigned as CT16B5_PWM2. 00: P2.8 01: P0.13 10: P1.0 11: P3.18	R/W	0
3:2	PWM1[1:0]	Pin to be assigned as CT16B5_PWM1. 00: P2.7 01: P0.14 10: P1.2 11: P3.17	R/W	0
1:0	PWM0[1:0]	Pin to be assigned as CT16B5_PWM0. 00: P2.6 01: P0.15 10: P1.1 11: P3.16	R/W	0

7 16+3 CHANNEL ANALOG TO DIGITAL CONVERTOR (ADC)

7.1 OVERVIEW

This analog to digital converter (ADC) has 16 external input sources, one internal channel to internal voltage source (2V/3V/4.5V), one internal channel to OPA0 output, and one internal channel to OPA1 output, with up to 4096-step resolution to transfer analog signal into 12-bits digital data. The sequence of ADC operation is to select input source (AIN0 ~ AIN15) at first, then set GCHS and ADS bit to “1” to start conversion. When the conversion is complete, the ADC circuit will set EOC bit to “1” and final value output in ADB register.

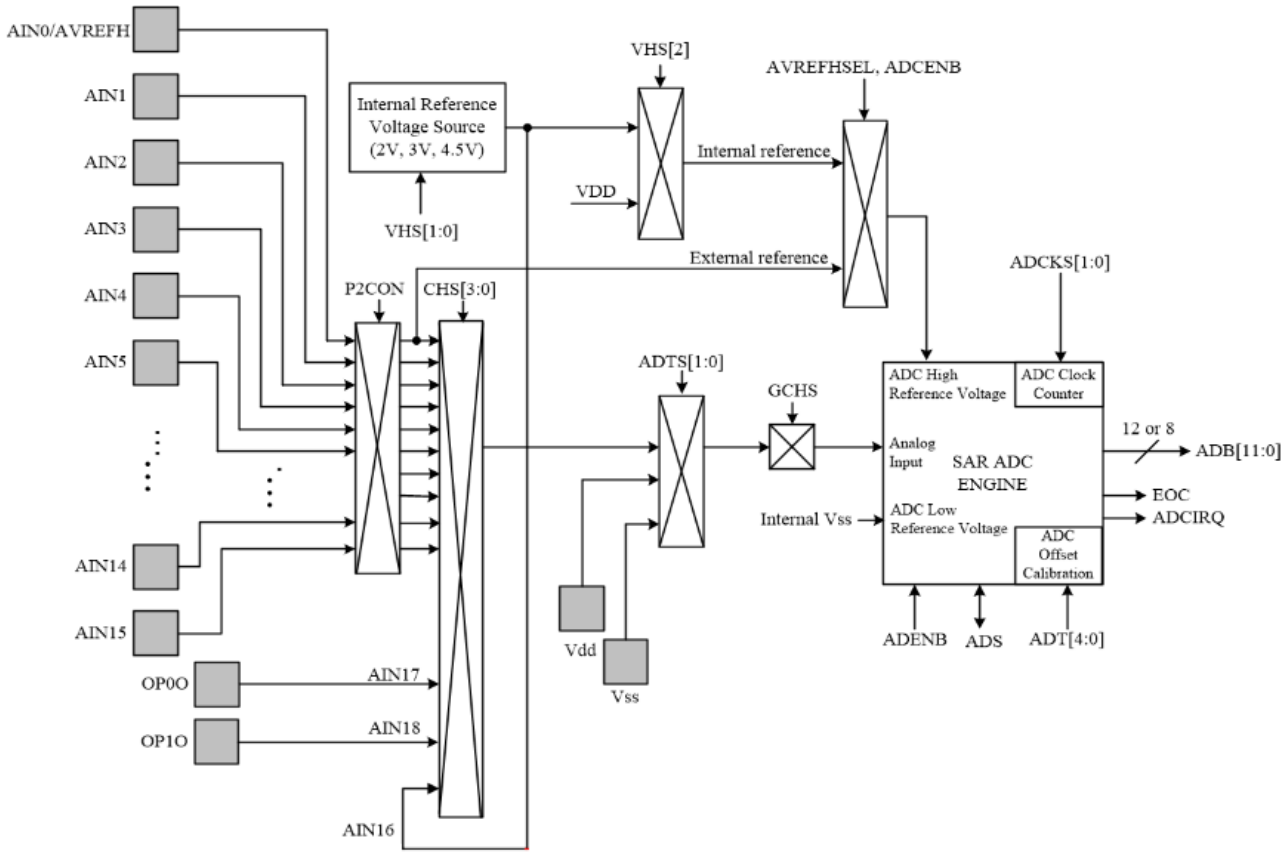
When ADC is enabled (ADENB=1) and global channel is enabled (GCHS=1), the ADC shared pins transfers to ADC purpose and disable GPIO function and disable pull-up/pull-down resistor by HW automatically. When ADC is disabled or global channel is disabled, the ADC pins returns to GPIO last status including pull-up/pull-down resistor. Use CHS[4:0] to select AIN pin and GCHS enables global ADC channel, the analog signal inputs to ADC engine.

The ADC resolution can be selected 8-bit or 12-bit through ADLEN bit in ADR register. The ADC converting rate can be selected by ADCKS[1:0] bits. These two parameters decide the ADC converting time.

The AIN16 is internal 2V or 3V or 4.5V input channel, there is no any input pin from outside. In this time ADC reference voltage must be internal VDD and External voltage, not internal 2V or 3V or 4.5V. AIN16 can be a good battery detector for battery system. To select appropriate internal AVREFH level and compare value, a high performance and cheaper low battery detector is built in the system.

The ADC reference high voltage includes two source, one is internal Vdd (AVREFHSEL=0), and the other one is external reference voltage input pin from P2.0 pin (AVREFHSEL=1).

The ADC resolution can be selected 8-bit or 12-bit through ADLEN bit in ADR register. The ADC converting rate can be selected by ADCKS[1:0] bits. The two parameters decide ADC converting time.



✷ ***Note:***

1. ***For 8-bit resolution the conversion time is 12 steps. For 12-bit resolution the conversion time is 16 steps***
2. ***ADC_PCLK shall be less than 16MHz.***
3. ***The analog input level must be between the AVREFH and AVREFL.***
4. ***The AVREFH level must be between the AVDD and AVREFL + 2.0V.***
5. ***ADC programming notice***
   - ***Disable ADC (set ADENB = "0") before enter low-power (Sleep/Deep-sleep) mode to save power consumption.***
   - ***Delay 100us after enable ADC (set ADENB = "1") to wait ADC circuit ready for conversion.***

7.2 ADC CONVERTING TIME

The ADC converting time is from ADS=1 (Start to ADC convert) to EOC=1 (End of ADC convert). The converting time duration is depend on ADC resolution and ADC clock rate.

ADC clock source is controlled by ADCKS[2:0] bits. The ADC converting time affects ADC performance. If input high rate analog signal, it is necessary to select a high ADC converting rate. If the ADC converting time is slower than analog signal variation rate, the ADC result would be error. So to select a correct ADC clock rate and ADC resolution to decide a right ADC converting rate is very important.

12-bit ADC conversion time = 1/(ADC clock /4)*16 sec

ADLEN	ADCKS [2:0]	ADC Clock	ADC_PCLK = 4 MHz		ADC_PCLK = 12 MHz		ADC_PCLK = 16 MHz	
			ADC Conversion Time (us)	ADC Conversion Rate (KHz)	ADC Conversion Time (us)	ADC Conversion Rate (KHz)	ADC Conversion Time (us)	ADC Conversion Rate (KHz)
1	000	ADC_PCLK	16	62.5	5.33	187.5	4	250
	001	ADC_PCLK/2	32	31.25	10.67	93.75	8	125
	010	ADC_PCLK/4	64	15.625	21.33	46.875	16	62.5
	011	ADC_PCLK/8	128	7.813	42.67	23.437	32	31.25
	100	ADC_PCLK/16	256	3.906	85.3	11.718	64	15.625
	101	ADC_PCLK/32	512	1.953	170.67	5.859	128	7.813

8-bit ADC conversion time = 1/(ADC clock /4)*12 sec

ADLEN	ADCKS [2:0]	ADC Clock	ADC_PCLK = 4 MHz		ADC_PCLK = 12 MHz		ADC_PCLK = 16 MHz	
			ADC Conversion Time (us)	ADC Conversion Rate (KHz)	ADC Conversion Time (us)	ADC Conversion Rate (KHz)	ADC Conversion Time (us)	ADC Conversion Rate (KHz)
0	000	ADC_PCLK	12	83.333	4	250	3	333.333
	001	ADC_PCLK/2	24	41.667	8	125	6	166.667
	010	ADC_PCLK/4	48	20.83	16	62.5	12	83.333
	011	ADC_PCLK/8	96	10.416	32	31.25	24	41.667
	100	ADC_PCLK/16	192	5.208	64	15.625	48	20.83
	101	ADC_PCLK/32	384	2.604	128	7.813	96	10.416

7.3 ADC CONTROL NOTICE

7.3.1 ADC SIGNAL

The ADC high reference voltage includes internal VDD/4V/3V/2V and external reference voltage source from P2.0/AVREFH pin controlled by AVREFHSEL bit. If AVREFHSEL=0, ADC reference voltage is from internal voltage source; if EVHENB=1, ADC reference voltage is from external voltage source (P2.0/AVREFH).
ADC reference voltage range limitation is **"(ADC high reference voltage – low reference voltage) ≧ 2V"**. ADC low reference voltage is Vss = 0V. So **ADC high reference voltage range is 2V~Vdd**. The range is ADC external high reference voltage range.

- **ADC Internal Low Reference Voltage = 0V**
- **ADC Internal High Reference Voltage = VDD/4.5V/3V/2V (AVREFHSEL = 0)**
- **ADC External High Reference Voltage = 2V~VDD (AVREFHSEL = 1)**

ADC sampled input signal voltage must be from ADC low reference voltage to ADC high reference. If the ADC input signal voltage is over the range, the ADC converting result is error (full scale or zero).

- **ADC Low Reference Voltage (VSS) ≦ ADC Sampled Input Voltage ≦ ADC High Reference Voltage**

7.3.2 ADC PROGRAM

The first step of ADC execution is to setup ADC configuration. The ADC program setup sequence and notices are as following.

- **Step 1:** Enable ADC. ADENB is ADC control bit to control. ADENB = 1 is to enable ADC. ADENB = 0 is to disable ADC. ***When ADENB is enabled, the system must be delay 100us to be the ADC warm-up time by program, and then set ADS to do ADC converting. The 100us delay time is necessary after ADENB setting (not ADS setting), or the ADC converting result would be error.*** Normally, the ADENB is set one time when the system under normal run condition, and do the delay time only one time.

- **Step 2:** If the ADC high reference voltage is from external voltage source, set the AVREFHSEL = 1. The ADC external high reference voltage inputs from P2.0 pin. ***It is necessary to set P2.0 as input mode without pull-up resistor.***

- **Step 3:** Select the ADC input pin by CHS[3:0], and enable ADC global input. **When one AIN pin is selected to be analog signal input pin, it is necessary to setup the pin as input mode and disable the pull-up resistor by program.**

- **Step 4:** Start to execute ADC conversion by setting ADS = 1.

- **Step 5:** Wait the end of ADC converting through checking EOC = 1 or ADCIF = 1. If ADC interrupt function is enabled, the program executes ADC interrupt service when ADC interrupt occurrence. ***ADS is cleared when the end of ADC converting automatically. EOC bit indicates ADC processing status immediately and is cleared when ADS = 1. Users needn't to clear it by program.***

7.3.3 ADC PIN CONFIGURATION

ADC input pins are shared with Port 2 digital I/O pins. ADC channel selection is through CHS[4:0] bits in ADC_ADM register. CHS[4:0] value points to the ADC input channel directly, CHS[4:0]=0000b selects AIN0, CHS[4:0]=0001b selects AIN1, etc.

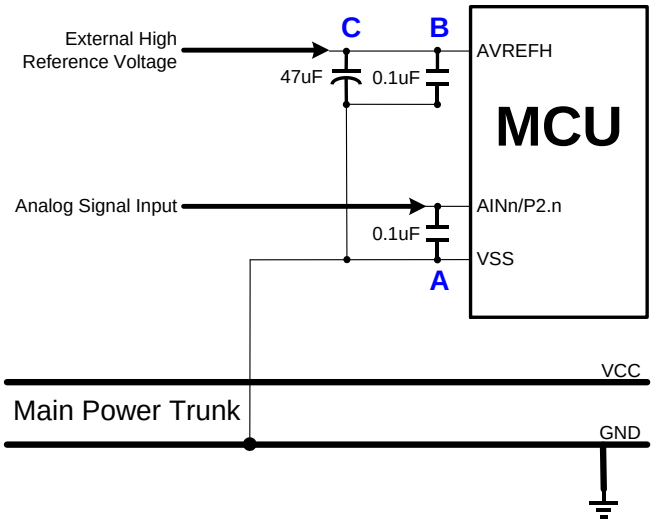
Connect an analog signal to COMS digital input pin, especially, the analog signal level is about 1/2 VDD will cause extra current leakage. In the power down mode, the above leakage current will be a big problem. Unfortunately, if users connect more than one analog input signal to Port 2 will encounter above current leakage situation.

The P2.0/AIN0 can be ADC external high reference voltage input pin when AVREFHSEL =1. In the condition, P2.0 GPIO mode must be set as input mode and inactive (no pull-down/up resistor enabled, Schmitt trigger disabled) with GPIO2_MODE and GPIO2_CFG register by program.

Only one pin of Port 2 can be configured as ADC input in the same time. The pins of Port 2 configured as ADC input channel must be set as input mode, inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low) with GPIO2_MODE and GPIO2_CFG register by program to avoid current leakage.

✸ ***Note: The GPIO mode of ADC input channels used must be set as input mode and inactive (no pull-down/pull-up resistor enabled, Schmitt trigger disabled, Data register keep low) with GPIO2_MODE and GPIO2_CFG register by program.***

7.4 ADC CIRCUIT



The analog signal is inputted to ADC input pin “AINn/P2.n”. The ADC input signal must be through a 0.1uF capacitor “A”. The 0.1uF capacitor is set between ADC input pin and VSS pin, and must be on the side of the ADC input pin as possible. Don’t connect the capacitor’s ground pin to ground plain directly, and must be through VSS pin. The capacitor can reduce the power noise effective coupled with the analog signal.

If the ADC high reference voltage is from external voltage source, the external high reference is connected to AVREFH pin (P2.0). The external high reference source must be through a 47uF ”C” capacitor first, and then 0.1uF capacitor “B”. These capacitors are set between AVREFH pin and VSS pin, and must be on the side of the AVREFH pin as possible. Don’t connect the capacitor’s ground pin to ground plain directly, and must be through VSS pin.

7.5 ADC REGISTERS

Base Address: 0x4002 6000

7.5.1 ADC Management register (ADC_ADM)

Address Offset: 0x00

✷ ***Note:***

1. ***When ADC is enabled (ADENB=1) and global channel is enabled (GCHS=1), the ADC shared pins transfers to ADC purpose and disable GPIO function and disable pull-up/pull-down resistor by HW automatically, the P2.n/AINn's digital I/O function including pull-up is isolated.***
2. ***When ADC is disabled (ADENB=0) or global channel is disabled (GCHS=0) , the ADC pins returns to last GPIO status.***
3. ***If P2.0 is used as external reference voltage input pin, users should set P2.0 as input mode inactive (no pull-down/up resistor enabled, Schmitt trigger disabled.***
4. ***If AIN16 channel is selected as internal 2V/3V/4.5V input channel, there is no any input pin from outside. In this time ADC reference voltage must be internal VDD and External voltage, Not internal 2V/3V/4.5V.***
5. ***The GPIO mode of ADC input channels used must be set as input mode and inactive (no pull-down/ pull-up resistor enabled, Schmitt trigger disabled, Data register keep low) with GPIO2_MODE and GPIO2_CFG register by program.***

Bit	Name	Description	Attribute	Reset
31:17	Reserved		R	0
16:14	VHS[2:0]	Internal reference voltage level selection. 000: Internal 2.0V as ADC internal reference high voltage 001: Internal 3.0V as ADC internal reference high voltage 010: Internal 4.5V as ADC internal reference high voltage 011: Reserved 100: VDD as ADC internal reference high voltage, Internal 2.0V as AIN16 101: VDD as ADC internal reference high voltage, Internal 3.0V as AIN16 110: VDD as ADC internal reference high voltage, Internal 4.5V as AIN16 111: VDD as ADC internal reference high voltage	R/W	000b
13	AVREFHSEL	ADC high reference voltage source select bit 0: Internal reference voltage. (P2.0 is GPIO or AIN0 pin) 1: Enable external reference voltage from P2.0	R/W	0
12	ADENB	ADC Enable bit. In power saving mode, disable ADC to reduce power consumption. 0: Disable 1: Enable	R/W	0
11:9	ADCKS[2:0]	ADC Clock source divider 000: ADC_PCLK / 1 001: ADC_PCLK / 2 010: ADC_PCLK / 4 011: ADC_PCLK / 8 101: ADC_PCLK / 16 110: ADC_PCLK / 32 Other: Reversed	R/W	0
8	ADLEN	ADC resolution control bit. 0: 8-bit ADC. 1:12-bit ADC.	R/W	0
7	ADS	ADC start control bit. 0: ADC converting stops. 1: Start to execute ADC converting. ADS is cleared when the end of ADC converting automatically.	R/W	0
6	EOC	ADC status bit. Indicates ADC processing status immediately and is cleared when ADS = 1. 0: ADC progressing.	R/W	0

		1: End of converting and reset ADS bit.		
5	GCHS	ADC global channel select bit. 0: Disable AIN channel 1: Enable AIN channel	R/W	0
4:0	CHS[4:0]	ADC input channels select bit. 00000: AIN0 00001: AIN1 00010: AIN2 00011: AIN3 00100: AIN4 00101: AIN5 00110: AIN6 00111: AIN7 01000: AIN8 01001: AIN9 01010: AIN10 01011: AIN11 01100: AIN12 01101: AIN13 01110: AIN14 01111: AIN15 10000: AIN16 (Internal reference voltage) 10001: AIN17 (OP0O) 10010: AIN18 (OP1O) Other: Reserved	R/W	0

7.5.2 ADC Data register (ADC_ADB)

Address Offset: 0x04

ADB is ADC data buffer to store AD converter result.

✸ ***Note: The initial value of ADC buffer (ADB) after reset is unknown.***

Bit	Name	Description	Attribute	Reset
31:12	Reserved		R	0
11:0	ADB[11:0]	ADB11~ADB4 bits for 8-bit ADC ADB11~ADB0 bits for 12-bit ADC	R	0

The AIN's input voltage vs. ADB's output data

AIN n	ADB11	ADB10	ADB9	ADB8	ADB7	ADB6	ADB5	ADB4	ADB3	ADB2	ADB1	ADB0
0/4096*VREFH	0	0	0	0	0	0	0	0	0	0	0	0
1/4096*VREFH	0	0	0	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
4094/4096*VREFH	1	1	1	1	1	1	1	1	1	1	1	0
4095/4096*VREFH	1	1	1	1	1	1	1	1	1	1	1	1

For different applications, users maybe need more than 8-bit resolution but less than 12-bit ADC converter. First, the AD resolution must be set 12-bit mode and then to execute ADC converter routine. Then delete the LSB of ADC data and get the new resolution result. The table is as following.

	ADB11	ADB10	ADB9	ADB8	ADB7	ADB6	ADB5	ADB4	ADB3	ADB2	ADB1	ADB0
8-bit	O	O	O	O	O	O	O	O	X	X	X	X
9-bit	O	O	O	O	O	O	O	O	O	X	X	X
10-bit	O	O	O	O	O	O	O	O	O	O	X	X
11-bit	O	O	O	O	O	O	O	O	O	O	O	X
12-bit.	O	O	O	O	O	O	O	O	O	O	O	O
O = Selected, X = Delete												

7.5.3 ADC Interrupt Enable register (ADC_IE)

Address offset: 0x0C

This register allows control over which A/D channels generate an interrupt when a conversion is complete. For example, it may be desirable to use some A/D channels to monitor sensors by continuously performing conversions on them. The most recent results are read by the application program whenever they are needed. In this case, an interrupt is not desirable at the end of each conversion for some A/D channels.

Bit	Name	Description	Attribute	Reset
31:19	Reserved		R	0
18:0	IE[18:0]	These bits allow control over which A/D channels generate interrupts for conversion completion. When bit x is one, completion of a conversion on AIN x will generate an interrupt.	R/W	0

7.5.4 ADC Raw Interrupt Status register (ADC_RIS)

Address offset: 0x10

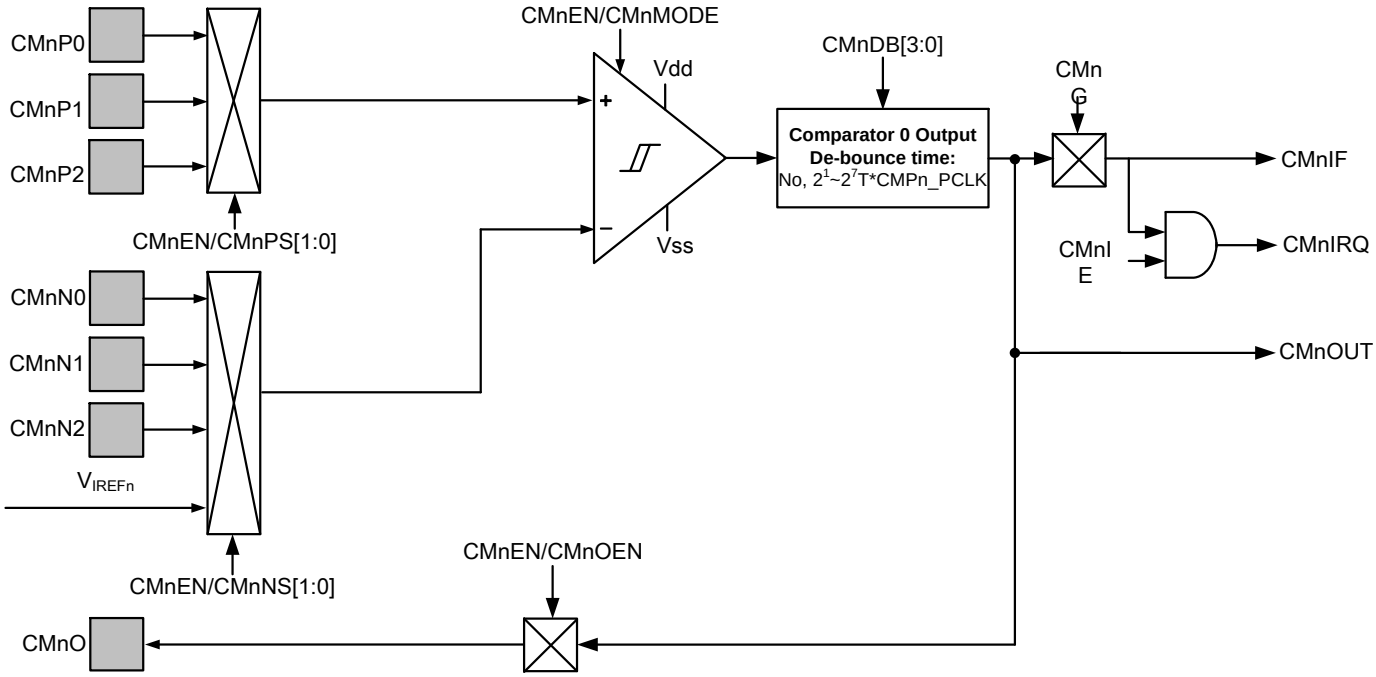
Bit	Name	Description	Attribute	Reset
31:19	Reserved		R	0
18:0	EOCIF[18:0]	ADC raw interrupt flag. (x = 0 to 18). 0: Read→No interrupt on AINx Write→Write “0” to the corresponding bit will clear the bit and reset the Interrupt if the corresponding IE bit is set. 1: Interrupt requirements (AINx finishes conversion) met on AINx.	R/W	0

8 RAIL TO RAIL ANALOG COMPARATOR

8.1 OVERVIEW

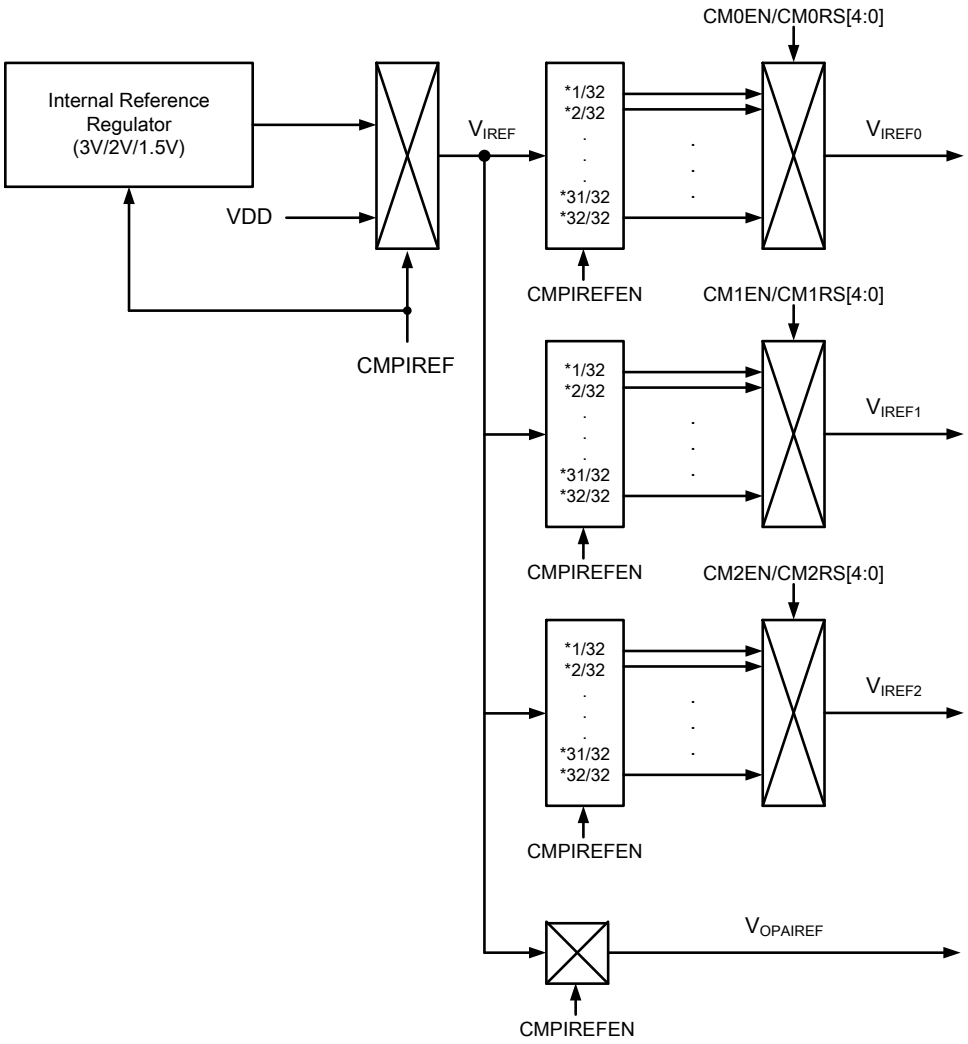
The micro-controller builds in 3 sets comparators (CMP0/1/2). The comparators are Rail-to-Rail structure. That means the input/output voltage is real from Vdd~Vss. When the positive input voltage is greater than the negative input voltage, the comparator output is high. When the positive input voltage is smaller than the negative input voltage, the comparator output is low.

The CMnOUT and CMnIRQ bits indicate the comparator result. The CMnOUT shows the comparator result immediately, but the CMnIRQ only indicates the event of the comparator result. The event condition is controlled by CMnG bit and includes rising edge (CMnOUT changes from low to high), falling edge (CMnOUT changes from high to low). The CMnIRQ = 1 condition makes the comparator interrupt service executed when CMnIE bit is set.



The comparator builds in internal reference to replace comparator external negative input voltage source and controlled by CMPIREF[1:0] and CMPIREFEN bits. The internal reference voltage is 3V/2V/1.5V from internal LDO, or VDD. When CMnNS[1:0] = 00b~10b, the comparator negative input is from external voltage source through CMnN0, CMnN1, or CMnN2 pin. When CMnNS[1:0] = 11b, the comparator negative voltage source is from internal reference and CMnN0/1/2 pins are GPIO function.

The comparator positive input terminal is controlled by CMnPS[1:0]. When CMnPS[1:0] = 01b~11b, the comparator positive input is from CMnP0, CMnP1, or CMnP2 pin. When CMnPS[1:0] = 00b, CMnP0/1/2 pins are GPIO function.
Besides, the comparator output signal is through a de-bounce circuit to filter comparator transient status. The de-bounce time is controlled by CMnDB[2:0] bits.



The main purposes of comparator are as following.

- **Normal comparator function:** General comparator mode compares the two tensions of positive input terminal and negative input terminal.
- **Interrupt function:** When comparator output edge direction equals to edge selection, the CMnIRQ actives and the system points program counter to interrupt vector to do interrupt sequence when CMnIE (comparator interrupt enable control bit) is set.

8.2 NORMAL COMPARATOR MODE

8.2.1 COMPARATOR ENABLE

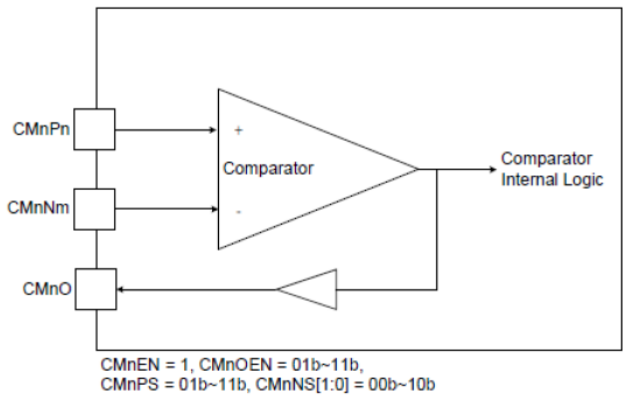
The comparator pins are shared with GPIO controlled by CMnEN bit.

When CM0EN=1 and CM0NS[1:0] = 00b~10b, the comparator negative voltage source is from external voltage source through CM0N0, CM0N1, or CM0N2 pin. When CM0NS[1:0] = 11b, the comparator negative positive voltage is from internal reference and CM0N0/1/2 pins are GPIO function. When CM0PS[1:0] = 01b~11b, the comparator positive input is from CM0P0, CM0P1, or CM0P2 pin. When CM0PS[1:0] = 00b, CM0P0/1/2 pins are GPIO function.

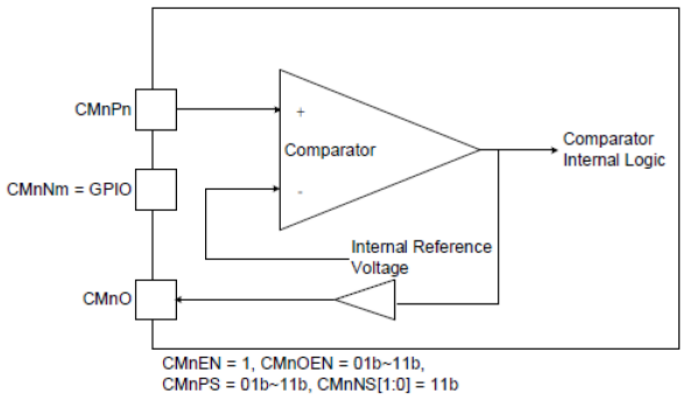
When CM1EN=1 and CM1NS[1:0] = 00b~10b, the comparator negative voltage source is from external voltage source through CM1N0, CM1N1, or CM1N2 pin. When CM1NS[1:0] = 11b, the comparator negative positive voltage is from internal reference and CM1N0/1/2 pins are GPIO function. When CM1PS[1:0] = 01b~11b, the comparator positive input is from CM1P0, CM1P1, or CM1P2 pin. When CM1PS[1:0] = 00b, CM1P0/1/2 pins are GPIO function.

When CM2EN=1 and CM2NS[1:0] = 00b~10b, the comparator negative voltage source is from external voltage source through CM2N0, CM2N1, or CM2N2 pin. When CM2NS[1:0] = 11b, the comparator negative positive voltage is from internal reference and CM2N0/1/2 pins are GPIO function. When CM2PS[1:0] = 01b~11b, the comparator positive input is from CM2P0, CM2P1, or CM2P2 pin. When CM2PS[1:0] = 00b, CM2P0/1/2 pins are GPIO function.

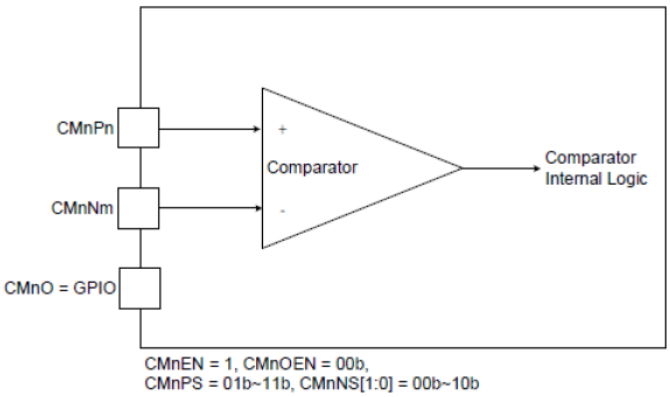
CMnOEN controls Comparator output connected to GPIO or not. When CMnOEN=1, Comparator output terminal is connected to GPIO pins and isolate GPIO function. When CMnOEN=0, comparator output status can be read through CMnOUT flag and CmnO pin is GPIO mode.



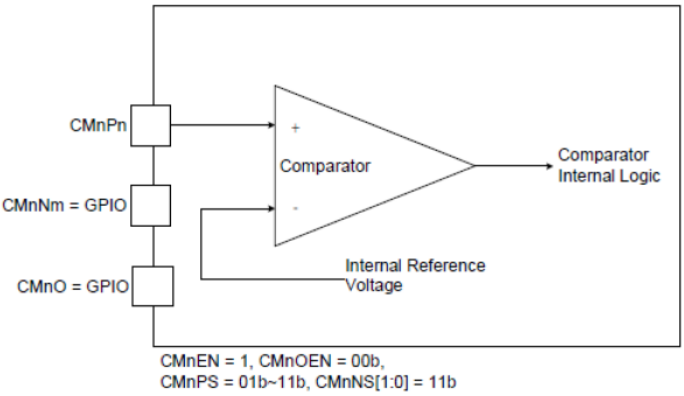
CMnEN = 1, CMnOEN = 01b~11b,
CMnPS = 01b~11b, CMnNS[1:0] = 00b~10b



CMnEN = 1, CMnOEN = 01b~11b,
CMnPS = 01b~11b, CMnNS[1:0] = 11b



CMnEN = 1, CMnOEN = 00b,
CMnPS = 01b~11b, CMnNS[1:0] = 00b~10b



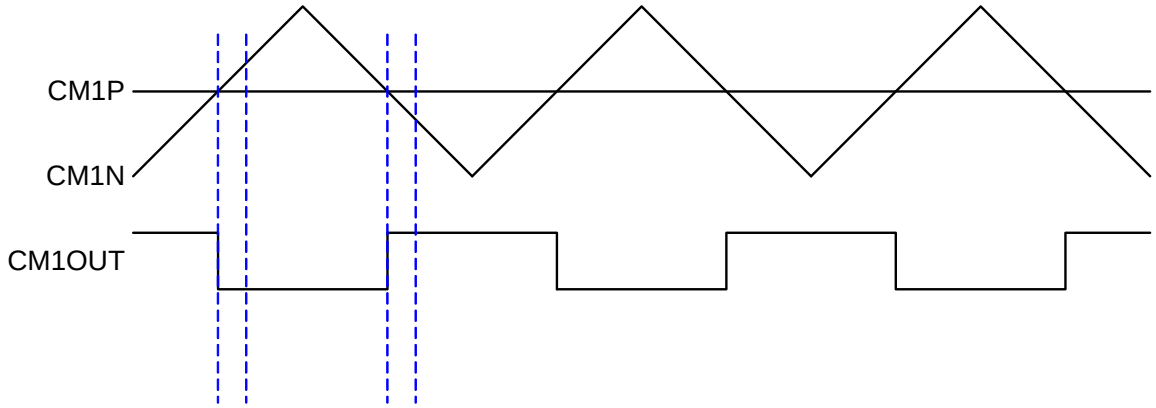
CMnEN = 1, CMnOEN = 00b,
CMnPS = 01b~11b, CMnNS[1:0] = 11b

8.2.2 CMnOUT, CMnG AND CMnIF

The CMnOUT and CMnIF bits indicate the comparator result. The CMnOUT shows the comparator result immediately, but the CMnIF only indicates the event condition of the comparator result.

Comparator n compares positive terminal's voltage and negative terminal's voltage, and then output result to output pin. When V+ > V-, comparator outputs high status. When V+ < V-, comparator outputs low status.

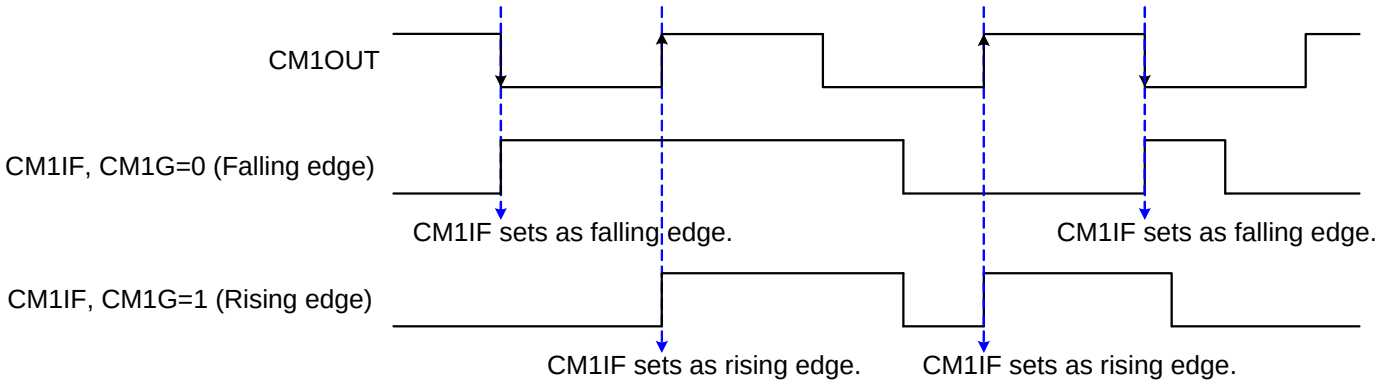
Take Comparator 1 as example,



The event condition is controlled by register and includes rising edge (CMnOUT changes from low to high), or falling edge (CMnOUT changes from high to low), controlled by CMnG bit. When CMnG= 0, the comparator n interrupt trigger direction is falling edge. When CMnG= 1, the comparator n interrupt trigger direction is rising edge. When comparator output edge event occurs and equal CMnG condition, CMnIF flag is issued. If CMnIE= 1, program counter points to interrupt vector to execute interrupt service routine.

✷ ***Note: CMnOUT is comparator raw output without latch. It varies depend on the comparator process result. But the CMnIF is latch comparator output result. It must be cleared by program.***

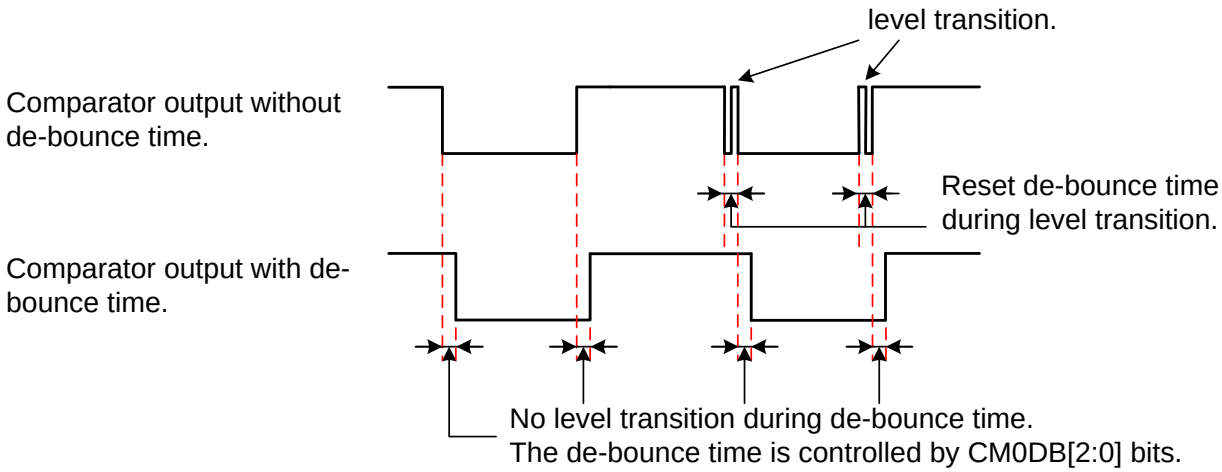
Take Comparator 1 as example,



***. CM1IF is cleared by program.**

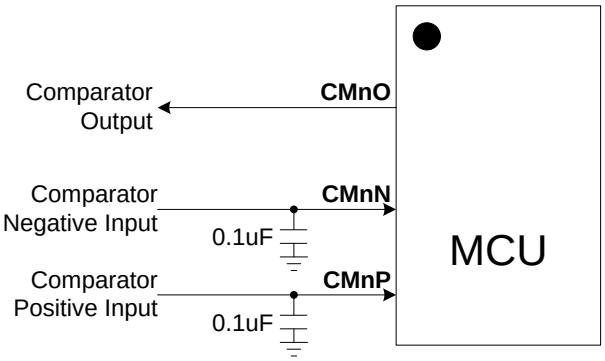
8.2.3 COMPARATOR OUTPUT DEBOUNCE TIME CONTROL

The critical condition is comparator positive voltage equal to comparator negative voltage, and the voltage range is decided comparator offset parameter of input common mode. In the voltage range, the comparator output signal is unstable and keeps oscillating until the differential voltage exits the range. In the condition, the comparator flag (CM0IF) latches the first exchanging and issue the status, but the status is a transient, not a stable condition. So the comparator builds in a filter to de-bounce the transient condition. The comparator output signal is through a de-bounce circuit to filter comparator transient status. The de-bounce time is controlled by CM0DB[2:0] bits that means the comparator minimum response time is 2*CMP_PCLK, 4*CMP_PCLK, 8*CMP_PCLK, …, 128*CMP_PCLK, or no de-bounce. The de-bounce time depends on the signal slew rate and selected by program.



8.3 COMPARATOR APPLICATION NOTICE

The comparator is to compares the positive voltage and negative voltage to output result. The positive and negative sources are analog signal. In hardware application circuit, the comparator input pins must be connected a 0.1uF comparator to reduce power noise and make the input signal more stable. The application circuit is as following.



8.4 CMP REGISTERS

Base Address: 0x4002 8000 (CMP)

8.4.1 CMP Control register (CMP_CTRL)

Address Offset: 0x00

Bit	Name	Description	Attribute	Reset
31:29	Reserved		R	0
28	CM1G	CMP1 interrupt trigger direction control bit. 0: Falling edge trigger (CMP1 output status is from high to low as V_+ < V-) 1: Rising edge trigger (CMP1 output status is from low to high as V+ > V-)	R/W	0
27:26	CM1OEN[1:0]	CMP1 output pin control bit. 00: Disable (CM1O is GPIO mode) 01: P2.2 is CM1O and isolate GPIO function. 10: P2.7 is CM1O and isolate GPIO function. 11: Reserved	R/W	0
25:21	CM1RS[4:0]	CMP1 internal reference voltage (V_{IREF1}) selection bits. 0000: $V_{IREF1} = V_{IREF}$ 00001~11111: $V_{IREF1} = V_{IREF} * CM1RS[4:0] / 32$	R/W	00000b
20:19	CM1NS[1:0]	CMP1 negative input pin selection bit 00: CM1N0 is comparator negative input pin, and isolate GPIO function 01: CM1N1 is comparator negative input pin, and isolate GPIO function 10: CM1N2 is comparator negative input pin, and isolate GPIO function 11: V_{IREF1}. CM1N0/CM1N1/CM1N2 pins are GPIO mode.	R/W	00b
18:17	CM1PS[1:0]	CMP1 positive input pin selection bit 00: Reserved. CM1P0/CM1P1/CM1P2 pins are GPIO mode. 01: CM1P0 is comparator positive input pin, and isolate GPIO function 10: CM1P1 is comparator positive input pin, and isolate GPIO function 11: CM1P2 is comparator positive input pin, and isolate GPIO function	R/W	01b
16	CM1EN	CMP1 enable bit. 0: Disable (CM1P0/1/2, CM1N0/1/2, CM1O are GPIO mode) 1: Enable	R/W	0
15:13	Reserved		R	0
12	CM0G	CMP0 interrupt trigger direction control bit. 0: Falling edge trigger (CMP0 output status is from high to low as V+ < V-) 1: Rising edge trigger (CMP0 output status is from low to high as V+ > V-)	R/W	0
11:10	CM0OEN[1:0]	CMP0 output pin control bits 00: Disable (CM0O is GPIO mode) 01: P2.0 is CM0O and isolate GPIO function. 10: P2.6 is CM0O and isolate GPIO function. 11: Reserved	R/W	0
9:5	CM0RS[4:0]	CMP0 internal reference voltage (V_{IREF0}) selection bits. 00000: $V_{IREF0} = V_{IREF}$ 00001~11111: $V_{IREF0} = V_{IREF} * CM0RS[4:0] / 32$	R/W	00000b
4:3	CM0NS[1:0]	CMP0 negative input selection bits 00: CM0N0 is comparator negative input pin, and isolate GPIO function 01: CM0N1 is comparator negative input pin, and isolate GPIO function 10: CM0N2 is comparator negative input pin, and isolate GPIO function 11: V_{IREF0}. CM0N0/CM0N1/CM0N2 pins are GPIO mode.	R/W	00b
2:1	CM0PS[1:0]	CMP0 positive input selection bits 00: ReservedCM0P0/CM0P1/CM0P2 pins are GPIO mode. 01: CM0P0 is comparator positive input pin, and isolate GPIO function 10: CM0P1 is comparator positive input pin, and isolate GPIO function 11: CM0P2 is comparator positive input pin, and isolate GPIO function	R/W	01b
0	CM0EN	CMP0 enable bit. 0: Disable (CM0P0/1/2, CM0N0/1/2, CM0O are GPIO mode) 1: Enable	R/W	0

8.4.2 CMP Control register 1 (CMP_CTRL1)

Address Offset: 0x04

Bit	Name	Description	Attribute	Reset
31:13	Reserved		R	0
12	CM2G	CMP2 interrupt trigger direction control bit. 0: Falling edge trigger (CMP2 output status is from high to low as V+ < V-) 1: Rising edge trigger (CMP2 output status is from low to high as V+ > V-)	R/W	0
11:10	CM2OEN[1:0]	CMP2 output pin control bit. 00: Disable (CM2O is GPIO mode) 01: P0.12 is CM2O and isolate GPIO function. 10: P0.3 is CM2O and isolate GPIO function. 11: P3.8 is CM2O and isolate GPIO function.	R/W	0
9:5	CM2RS[4:0]	CMP2 internal reference voltage (V_{IREF2}) selection bits. 00000: $V_{IREF2} = V_{IREF}$ 00001~11111: $V_{IREF2} = V_{IREF} * CM2RS[4:0] / 32$	R/W	00000b
4:3	CM2NS[1:0]	CMP2 negative input pin selection bit 00: CM2N0 is comparator negative input pin, and isolate GPIO function 01: CM2N1 is comparator negative input pin, and isolate GPIO function 10: CM2N2 is comparator negative input pin, and isolate GPIO function 11: V_{IREF2}. CM2N0/CM2N1/CM2N2 pins are GPIO mode.	R/W	00b
2:1	CM2PS[1:0]	CMP2 positive input pin selection bit 00: Reserved. CM2P0/CM2P1/CM2P2 pins are GPIO mode. 01: CM2P0 is comparator positive input pin, and isolate GPIO function 10: CM2P1 is comparator positive input pin, and isolate GPIO function 11: CM2P2 is comparator positive input pin, and isolate GPIO function	R/W	01b
0	CM2EN	CMP2 enable bit. 0: Disable (CM2P0/1/2, CM2N0/1/2, CM2O are GPIO mode) 1: Enable	R/W	0

8.4.3 CMP Internal Reference Voltage Source register (CMP_VIREF)

Address Offset: 0x08

Bit	Name	Description	Attribute	Reset
31:3	Reserved		R	0
2:1	CMPIREF[1:0]	Comparator internal reference voltage (V_{IREF}) source 00: VDD 01: internal 1.5V 10: internal 2V 11: Internal 3V	R/W	0
0	CMPIREFEN	Comparator internal reference voltage (V_{IREF}) enable bit. 0: Disable 1: Enable	R/W	0

8.4.4 CMP Output Status register (CMP_OS)

Address Offset: 0x0C

✷ ***Note: CMnOUT is comparator raw output without latch. It varies depend on the comparator process result. But the CMnIF is latch comparator output result. It must be cleared by program.***

Bit	Name	Description	Attribute	Reset
31:3	Reserved		R	0
2	CM2OUT	CMP2 output flag bit. 0: $V_{2+} < V_{2-}$ 1: $V_{2+} > V_{2-}$	R	0
1	CM1OUT	CMP1 output flag bit. 0: $V_{1+} < V_{1-}$ 1: $V_{1+} > V_{1-}$	R	0
0	CM0OUT	CMP0 output flag bit. 0: $V_{0+} < V_{0-}$ 1: $V_{0+} > V_{0-}$	R	0

8.4.5 CMP Interrupt Enable register (CMP_IE)

Address Offset: 0x10

Bit	Name	Description	Attribute	Reset
31:3	Reserved		R	0
2	CM2IE	CMP2 interrupt enable control bit. 0: Disable 1: Enable	R/W	0
1	CM1IE	CMP1 interrupt enable control bit. 0: Disable 1: Enable	R/W	0
0	CM0IE	CMP0 interrupt enable control bit. 0: Disable 1: Enable	R/W	0

8.4.6 CMP Raw Interrupt Status register (CMP_RIS)

Address offset: 0x14

This register indicates the status for comparator raw interrupts. A CMP0/1/2 interrupt is sent to the interrupt controller if the corresponding CMnIE bit is set.

✸ ***Note: CMnOUT is comparator raw output without latch. It varies depend on the comparator process result. But the CMnIF is latch comparator output result. It must be cleared by program.***

Bit	Name	Description	Attribute	Reset
31:3	Reserved		R	0
2	CM2IF	CMP2 raw interrupt flag 0: No interrupt on CMP2 1: Interrupt requirements met on CMP2	R	0
1	CM1IF	CMP1 raw interrupt flag 0: No interrupt on CMP1 1: Interrupt requirements met on CMP1	R	0
0	CM0IF	CMP0 raw interrupt flag 0: No interrupt on CMP0 1: Interrupt requirements met on CMP0	R	0

8.4.7 CMP Interrupt Clear register (CMP_IC)

Address offset: 0x18

Bit	Name	Description	Attribute	Reset
31:3	Reserved		R	0
2	CM2IC	Select the interrupt flag on CMP2 to be cleared 0: No effect 1: Clear CM2IF bit	W	0
1	CM1IC	Select the interrupt flag on CMP1 to be cleared 0: No effect 1: Clear CM1IF bit	W	0
0	CM0IC	Select the interrupt flag on CMP0 to be cleared 0: No effect 1: Clear CM0IF bit	W	0

8.4.8 CMP Output Debounce register (CMP_DB)

Address offset: 0x1C

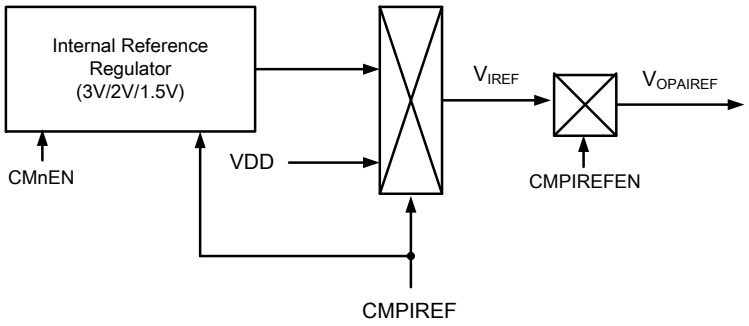
Bit	Name	Description	Attribute	Reset
31:11	Reserved		R	0
10:8	CM2DB[2:0]	Count for CMP2 output debounce time 000: No CMP2 output debounce time 001~111: CMP2 output debounce time = $2^{CM2DB[2:0]}$ * CMP2_PCLK cycle	W/R	000b
7	Reserved		R	0
6:4	CM1DB[2:0]	Count for CMP1 output debounce time 000: No CMP1 output debounce time 001~111: CMP1 output debounce time = $2^{CM1DB[2:0]}$ * CMP1_PCLK cycle	W/R	000b
3	Reserved		R	0
2:0	CM0DB[2:0]	Count for CMP0 output debounce time 000: No CMP0 output debounce time 001~111: CMP0 output debounce time = $2^{CM0DB[2:0]}$ * CMP0_PCLK cycle	W/R	000b

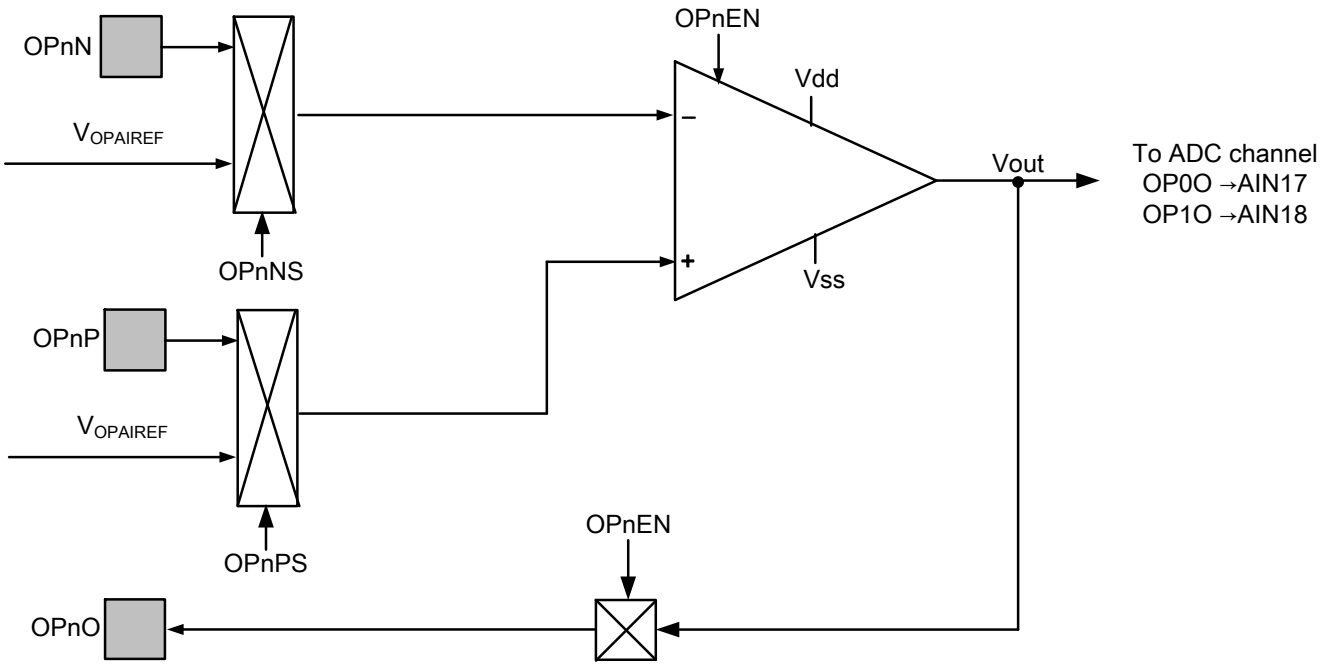
9 OPERATIONAL-AMPLIFIER (OPA)

9.1 OVERVIEW

The microcontroller builds in two operational amplifiers (OP0 and OP1). The OP-Amp power range is VSS~VDD. OP-Amp input signal and output voltage are within the voltage range. The OP-Amp output pin is programmable to connect with ADC input channel (AIN17 and AIN18) for voltage measurement.

The internal reference regulator of the comparator is also shared with OPA.





9.2 CONFIGURATION OF OPERATION

The OP-AMP pins are shared with GPIO controlled by OP0EN/OP1EN bit. When OPEN=0, OP AMP pins are GPIO mode. When OPEN=1, GPIO pins switch to OP-AMP and isolate GPIO path. OP-AMP pins selection table is as following.

OPA#	OPnEN	OP Positive Pin (V+)	OP Negative Pin (V-)	OP Output Pin
OPA0	0	All shared pins are GPIO mode.		
	1	OP0P if OP0PS = 1 $V_{OPAIREF}$ if OP0PS = 0	OP0N if OP0NS = 1 $V_{OPAIREF}$ if OP0NS = 0	OP0O
OPA1	0	All shared pins are GPIO mode.		
	1	OP1P if OP1PS = 1 $V_{OPAIREF}$ if OP1PS = 0	OP1N if OP1NS = 1 $V_{OPAIREF}$ if OP1NS = 0	OP1O

9.3 OPA REGISTERS

Base Address: 0x4002 8000 (CMP)

9.3.1 OPA Control register (OPA_CTRL)

Address Offset: 0x00

Bit	Name	Description	Attribute	Reset
31:13	Reserved		R	0
12	OP1NS	OP-Amp 1 negative input selection bit 0: $V_{OPAIREF}$. OP1N pin is GPIO mode. 1: OP1N. OP1N is OPA1 negative input pin, and isolate GPIO function.	R/W	0
11	OP1PS	OP-Amp 1 positive input selection bit 0: $V_{OPAIREF}$. OP1P pin is GPIO mode. 1: OP1P. OP1P is OPA1 positive input pin, and isolate GPIO function.	R/W	0
10:9	Reserved		R	0
8	OP1EN	OP-Amp 1 enable bit. 0: Disable. OP1O/OP1P/OP1N pins are GPIO mode. 1: Enable. OP1O is OP-Amp 1 output pin.	R/W	0
7:5	Reserved		R	0
4	OP0NS	OP-Amp 0 negative input selection bit 0: $V_{OPAIREF}$. OP0N pin is GPIO mode. 1: OP0N. OP0N is OPA0 negative input pin, and isolate GPIO function.	R/W	0
3	OP0PS	OP-Amp 0 positive input selection bit 0: $V_{OPAIREF}$. OP0P is GPIO mode 1: OP0P. OP0P is OPA0 positive input pin, and isolate GPIO function.	R/W	0
2:1	Reserved		R	0
0	OP0EN	OP-Amp 0 enable bit. 0: Disable. OP0O/OP0P/OP0N pins are GPIO mode. 1: Enable. OP0O is OP-Amp 0 output pin.	R/W	0

10 16-BIT TIMER WITH CAPTURE FUNCTION

10.1 OVERVIEW

The microcontroller builds in six 16-bit timers (CT16B0~CT16B5). Each Counter/timer is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and can optionally generate interrupts or perform other actions at specified timer values based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

In PWM mode, up to 12 match and a global match registers can be used to provide a single-edge controlled PWM output on the match output pins.

	CT16B0	CT16B1	CT16B2	CT16B3	CT16B4	CT16B5
Clock Source	HCLK PLL_VCO			HCLK PLL_VCO ELS		
Counter Mode	Up/Down/ Center-aligned counting	Up-counting	Up/Down/ Center-aligned counting	Up-counting	Up-counting	Up/Down/ Center-aligned counting
PWM	PWM0/1/2/3+ PWM0N/1N/2N/3N	PWM0/1/…/11	PWM0/1/2/3	PWM0/1+ PWM0N/1N	PWM0/1+ PWM0N/1N	PWM0/1/2/3
PCLK	max 96MHz	max 96MHz	max 96MHz	max 96MHz	max 96MHz	max 96MHz

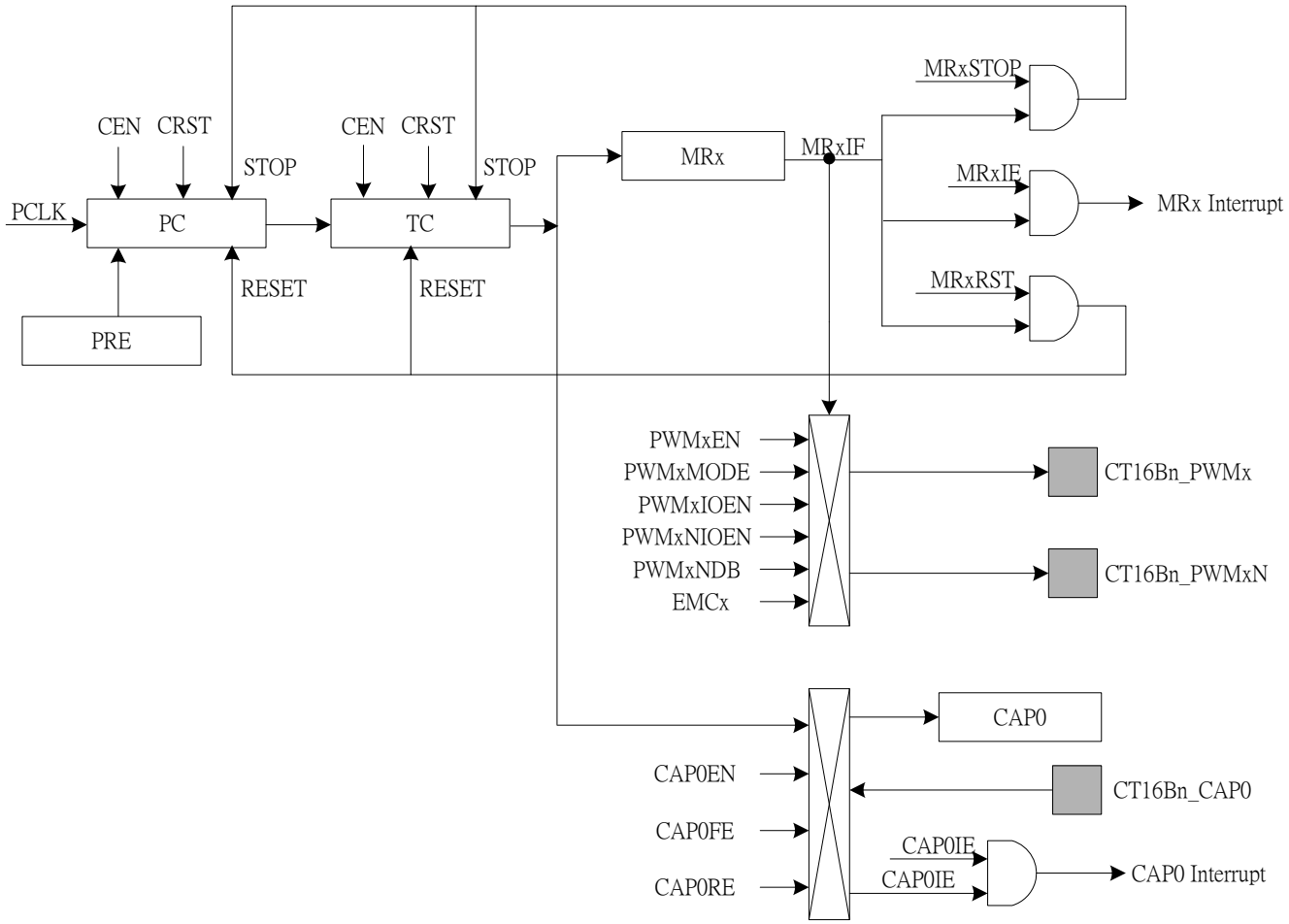
10.2 FEATURES

- Six 16-bit counter/timers with a programmable 8-bit prescaler.
- Counter or timer operation
- Six 16-bit capture channels that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Six 16-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to 4 (CT16B0, CT16B2, CT16B5), 12 (CT16B1), or 2 (CT16B3, CT16B4) PWM outputs corresponding to match registers with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- For CT16B0, up to 4 complete inverse waveform of the PWM signals, and builds in programmable dead-band function.
- For CT16B3 and CT16B4, up to 2 complete inverse waveform of the PWM signals, and builds in programmable dead-band function.

10.3 PIN DESCRIPTION

Pin Name	Type	Description	GPIO Configuration
CT16Bn_CAP0	I	Capture channel input 0	Depends on GPIOn_CFG
CT16Bn_PWMx	O	Output channel x of Match/PWM output.	
CT16Bn_PWMxN	O	Inverse Output channel of Match/PWMx output.	

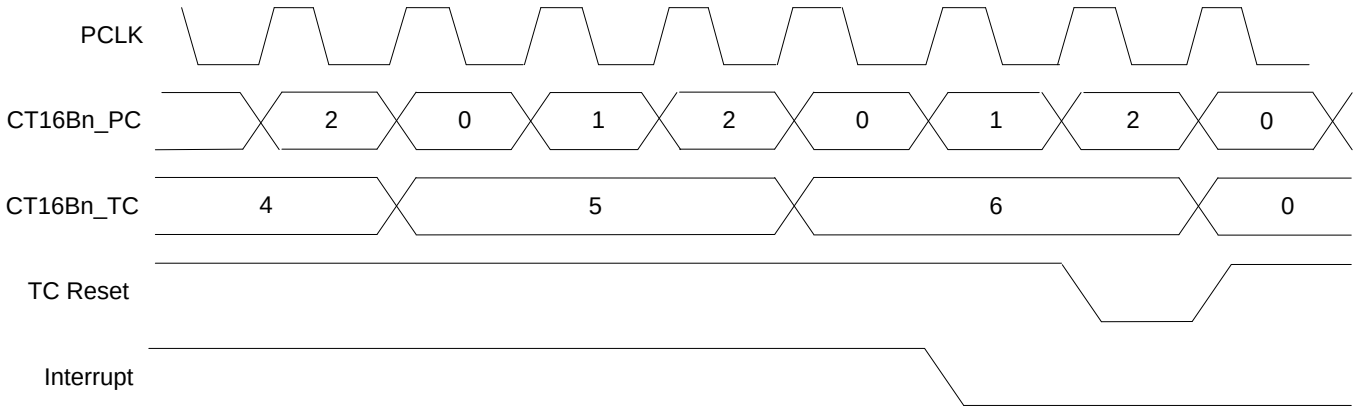
10.4 BLOCK DIAGRAM



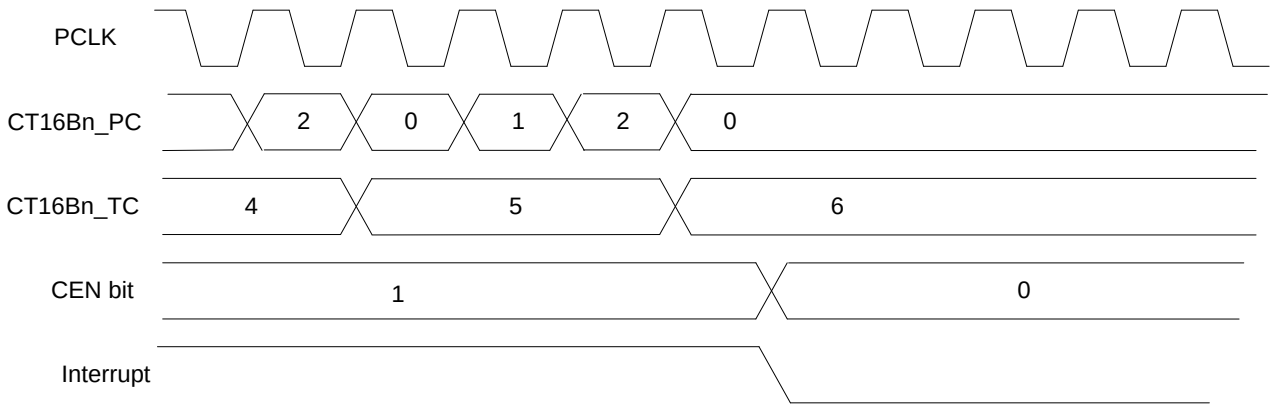
10.5 TIMER OPERATION

10.5.1 Edge-aligned Up-counting Mode

The following figure shows a timer configured to reset the count (TC) and generate an interrupt on match in Edge-aligned up-counting mode. The CT16Bn_PRE register is set to 2, and the CT16Bn_MRx register is set to 6. At the end of the timer cycle where the match occurs, the timer count is reset. This gives a full length cycle to the match value. The interrupt indicating that a match occurred is generated in the next clock after the timer reached the match value.



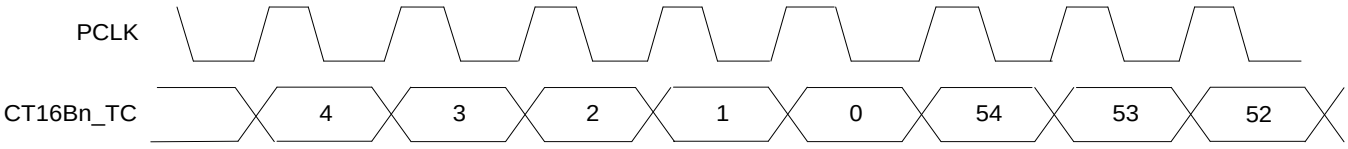
The following figure shows a timer configured to stop and generate an interrupt on match in Edge-aligned up-counting mode. The CT16Bn_PRE register is set to 2, and the CT16Bn_MRx register is set to 6. In the next clock after the timer reaches the match value, the CEN bit in CT16Bn_TMRCTRL register is cleared, and the interrupt indicating that a match occurred is generated.



10.5.2 Edge-aligned Down-counting Mode

The timer count TC[15:0] will be reset to the value of CT16Bn_MR3 after resetting counter or TC reaches 0. Besides, TC is blocked while the value of CT16Bn_MR9 is zero.

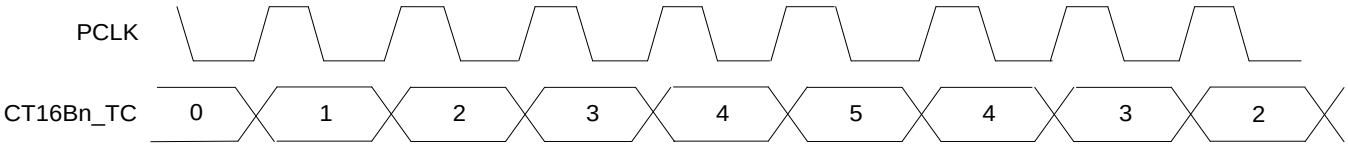
The following figure shows a timer configured to reset the count in Edge-aligned down-counting mode. The CT16Bn_PRE register is set to 0, and the CT16Bn_MR9 register is set to 54. After TC reaches 0, the timer count is reset and loaded from the value of CT16Bn_MR9.



10.5.3 Center-aligned Counting Mode

In Center-aligned counting mode, TC counts up from 0 to the value of CT16Bn_MR9, and then counts down to 0 alternatively. Besides, TC is blocked while the value of CT16Bn_MR9 is zero.

The following figure shows a timer in Center-aligned counting mode. The CT16Bn_PRE register is set to 0, and the CT16Bn_MR9 register is set to 5.



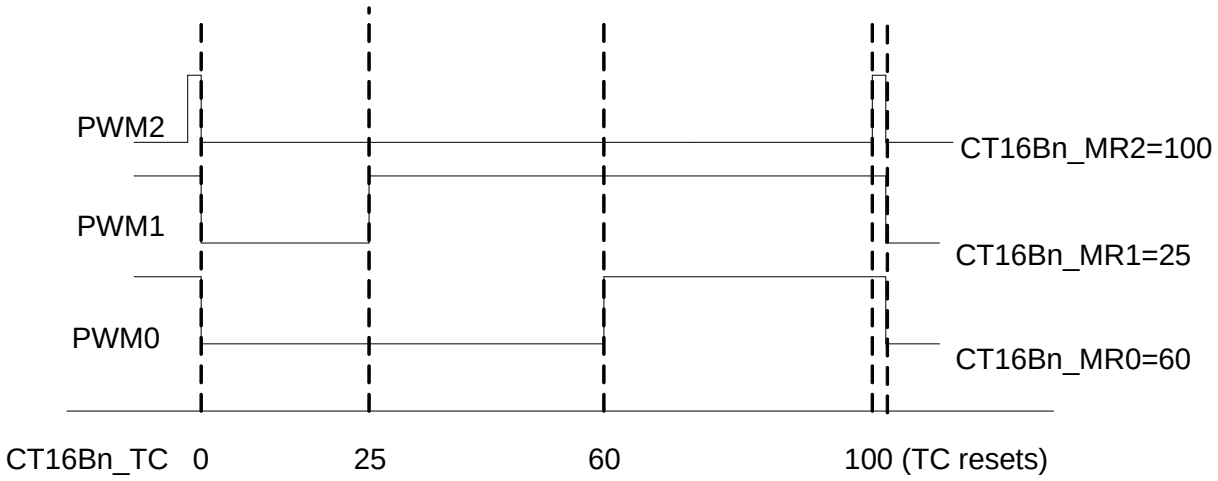
10.6 PWM

10.6.1 PWM Mode 1

- PWMn is 0 when TC<MRn during Up-counting period
- PWMn is 0 when TC≤MRn during Down-counting period

Take Edge-aligned up-counting Mode as example,

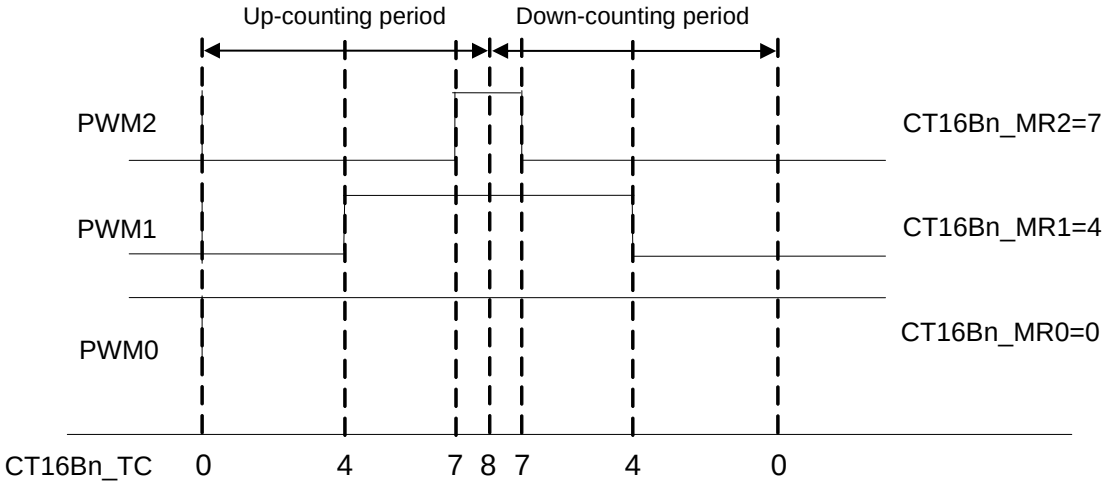
1. All single edge controlled PWM outputs go LOW at the beginning of each PWM cycle (timer is set to zero) unless their match value in CT16Bn_MR0~3 registers is equal to zero.
2. Each PWM output will go HIGH when its match value is reached. If no match occurs, the PWM output remains continuously LOW.
3. If a match value larger than the PWM cycle length is written to the CT16Bn_MR0~3 registers, and the PWM signal is HIGH already, then the PWM signal will be cleared on the next start of the next PWM cycle.
4. If a match register contains the same value as the timer reset value (the PWM cycle length), then the PWM output will be reset to LOW on the next clock tick. Therefore, the PWM output will always consist of a one clock tick wide positive pulse with a period determined by the PWM cycle length.
5. If a match register is set to zero, then the PWM output will go HIGH the first time the timer goes back to zero and will stay HIGH continuously.



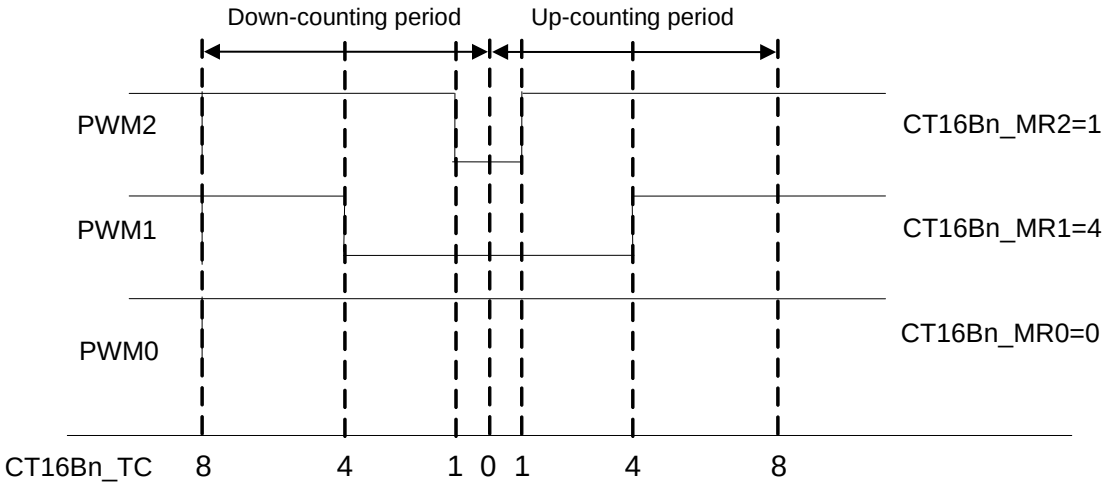
- ***Note: When the match outputs are selected to perform as PWM outputs, the timer reset (MRnRST) and timer stop (MRnSTOP) bits in CT16Bn_MCTRL register must be set to zero except for the match register setting the PWM cycle length. For this register, set the MRnR bit to one to enable the timer reset when the timer value matches the value of the corresponding match register.***

The following figure shows the PWM mode 1 wave form in Center-aligned counting mode.

Case1: The CT16Bn_PRE register is set to 0, the CT16Bn_MR9 register is set to 8, the CT16Bn_MR2 register is set to 7, the CT16Bn_MR1 register is set to 4, and the CT16Bn_MR0 register is set to 0.



Case 2: The CT16Bn_PRE register is set to 0, the CT16Bn_MR9 register is set to 8, the CT16Bn_MR2 register is set to 1, the CT16Bn_MR1 register is set to 4, and the CT16Bn_MR0 register is set to 0.



10.6.2 PWM Mode 2

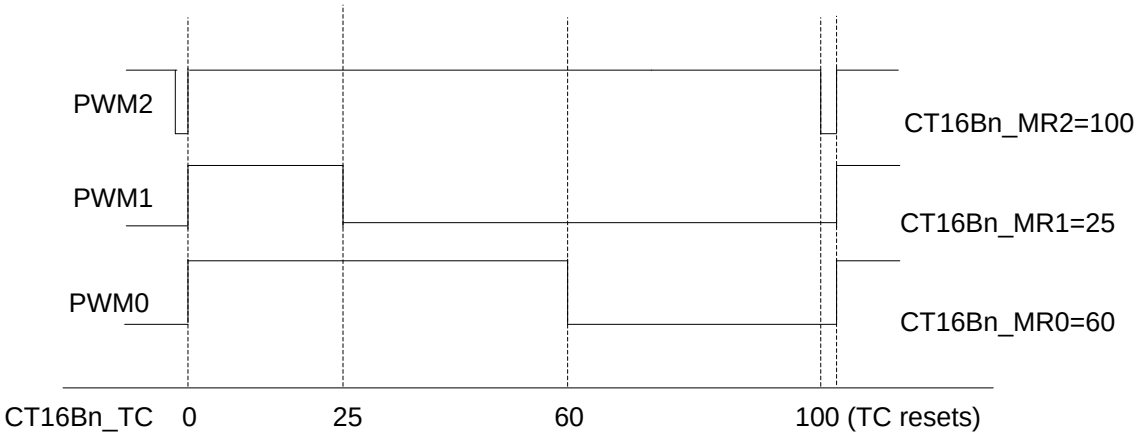
- PWMn is 1 when TC<MRn during Up-counting period
- PWMn is 1 when TC≤MRn during Down-counting period
- Not support in Center-aligned counting mode

Take Edge-aligned up-counting Mode as example,

1. All single edge controlled PWM outputs go HIGH at the beginning of each PWM cycle (timer is set to zero) unless their match value in CT16Bn_MR0~3 registers is equal to zero.
2. Each PWM output will go LOW when its match value is reached. If no match occurs, the PWM output remains continuously HIGH.
3. If a match value larger than the PWM cycle length is written to the CT16Bn_MR0~3 registers, and the PWM signal is LOW already, then the PWM signal will go HIGH on the next start of the next PWM cycle.

4. If a match register contains the same value as the timer reset value (the PWM cycle length), then the PWM output will be reset to HIGH on the next clock tick. Therefore, the PWM output will always consist of a one clock tick wide low pulse with a period determined by the PWM cycle length.

5. If a match register is set to zero, then the PWM output will go LOW the first time the timer goes back to zero and will stay LOW continuously.



✸ ***Note: When the match outputs are selected to perform as PWM outputs, the timer reset (MRnRST) and timer stop (MRnSTOP) bits in CT16Bn_MCTRL register must be set to zero except for the match register setting the PWM cycle length. For this register, set the MRnR bit to one to enable the timer reset when the timer value matches the value of the corresponding match register.***

10.7 INVERSE PWM OUTPUT WITH DEAD-BAND PERIOD

The CT16B2_PWMm builds in inverse output function controlled by PWMmNIOEN[1:0] bits in CT16Bn_PWMCTRL register.

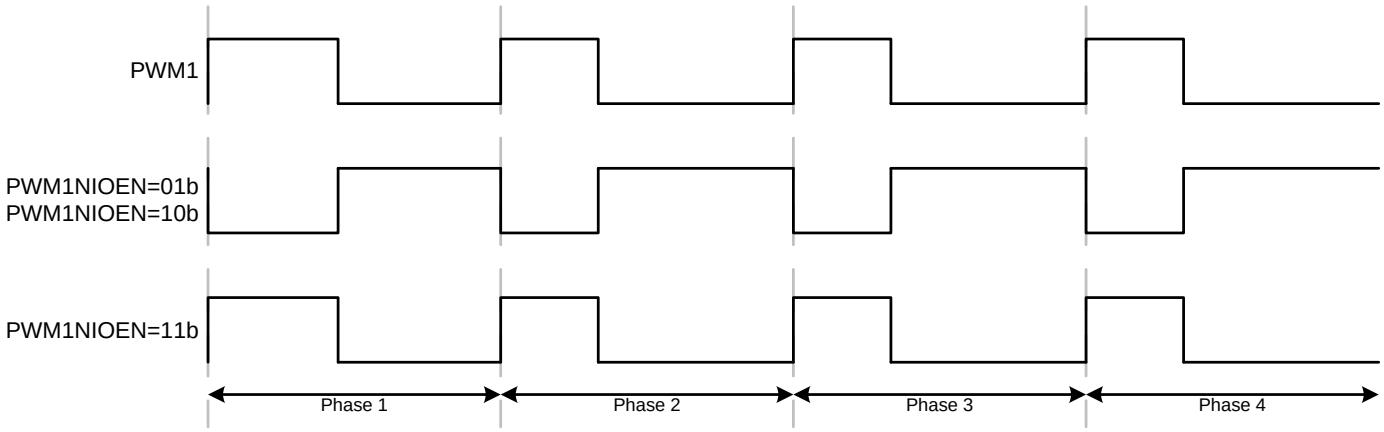
- When PWMmNIOEN[1:0] = 00b, PWMmN pin is GPIO mode.
- When PWMmNIOEN[1:0] = 01b, PWMmN pin changes to inverse PWM output pin which outputs the inverse PWM signal of PWMm with dead-band period, but same High signal during dead-band period.
- When PWMmNIOEN[1:0] = 10b, PWMmN pin changes to inverse PWM output pin which outputs the inverse PWMm signal with dead-band period, but same Low signal during dead-band period.
- When PWMmNIOEN[1:0] = 11b, PWMmN pin changes to non-inverse PWM output pin which outputs the same PWMm signal with dead-band period.

The dead- band period is symmetrical at left-right terminal of PWM high pulse width, and the PWM dead-band period is controlled by CT16Bn_PWMmNDB register. This register is only usable when PWMmNIOEN[1:0] ≠ 00b, and the PWM dead-band function is disabled when the value of this register is 0.

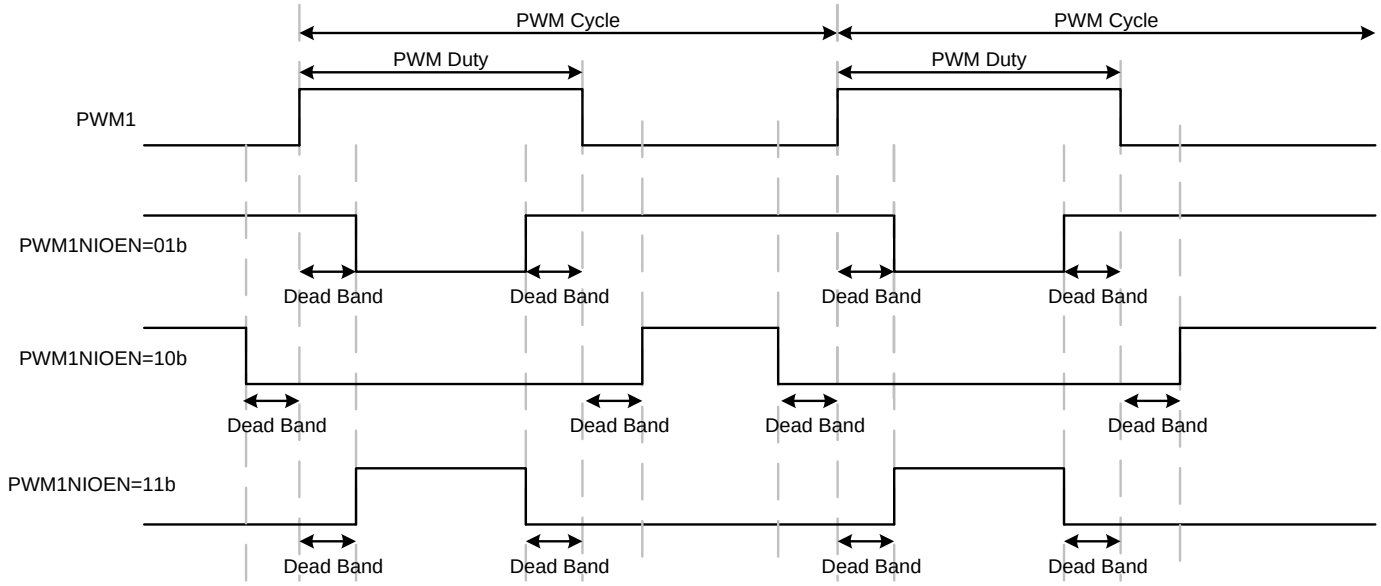
If DB = 1, the dead-band period is set as 1*CT16Bn_PCLK*(PR+1), 1*CT16Bn_PCLK*(PR+1) dead-band is in the left side of PWM high pulse, and the other side also includes one dead-band duration, so the total dead-band period is 2*CT16Bn_PCLK*(PR+1).

To take care the PWM high pulse width with dead-bane function is necessary. Recommend the dead-band period less than PWM high pulse width, or the PWM high pulse width disappears.

The PWMmN waveform without dead-band:



The PWMmN waveform with dead-band:



- ***Note: If the bead-band period is longer than PWM duty, the PWM1N is no output.***
- ***Note: When the dead-band function is enabled in Center-aligned mode, and MR9RST=1, CT16Bn_PWMxN will always output "0"***
- ***Note: When the dead-band function is enabled***
  - ***System will reset TC refer to MR9RST ONLY in Up-counting mode***
  - ***In Down counting mode, TC[15:0] will be reloaded from CT16Bn_MR9 after resetting counter***
  - ***System will reset TC refer to MR9RST ONLY in Center-aligned mode***

10.8 CT16Bn REGISTERS

Base Address: 0x4000 0000 (CT16B0)
0x4000 2000 (CT16B1)
0x4000 4000 (CT16B2)
0x4000 6000 (CT16B3)
0x4000 8000 (CT16B4)
0x4000 A000 (CT16B5)

Register	n	Offset
CT16Bn_TMRCTRL	0/1/2/3/4/5	0x00
CT16Bn_TC	0/1/2/3/4/5	0x04
CT16Bn_PRE	0/1/2/3/4/5	0x08
CT16Bn_PC	0/1/2/3/4/5	0x0C
CT16Bn_CNTCTRL	0/1/2/3/4/5	0x10
CT16Bn_MCTRL	0/1/2/3/4/5	0x14
CT16Bn_MCTRL2	1	0x18
CT16Bn_MR0~MR1	0/1/2/3/4/5	0x20~0x24
CT16Bn_MR2	0/1/2/5	0x28
CT16Bn_MR3	0/1/2/5	0x2C
CT16Bn_MR4~MR8	1	0x30~0x40
CT16Bn_MR9	0/1/2/3/4/5	0x44
CT16Bn_MR10~MR11	1	0x48~0x4C
CT16Bn_MR12	1	0x50
CT16Bn_CAPCTRL	0/1/2/3/4/5	0x84
CT16Bn_CAP0	0/1/2/3/4/5	0x88
CT16Bn_EM	0/1/2/3/4/5	0x8C
CT16Bn_EMC	1	0x90
CT16Bn_PWMCTRL	0/1/2/3/4/5	0x98
CT16Bn_PWMENB	1	0xA0
CT16Bn_PWMIOENB	1	0xA4
CT16Bn_RIS	0/1/2/3/4/5	0xA8
CT16Bn_IC	0/1/2/3/4/5	0xAC
CT16Bn_PWMmNIOCTRL	0/3/4	0xB0
CT16Bn_PWMmNDB, m=0,1,2,3	0/3/4	0xB4~0xBC

10.8.1 CT16Bn Timer Control register (CT16Bn_TMRCTRL) (n=0,2)

Address Offset: 0x00

✷ ***Note: CEN bit shall be set at last!***

Bit	Name	Description	Attribute	Reset
31:7	Reserved		R	0
6:4	CM[2:0]	Counting mode selection 000: Edge-aligned Up-counting mode 001: Edge-aligned Down-counting mode 010: Center-aligned mode 1. The match interrupt flag is set during the down-counting period 100: Center-aligned mode 2. The match interrupt flag is set during the up-counting period 110: Center-aligned mode 3. The match interrupt flag is set during both up-counting and down-counting period	R/W	000b

		Other: Reserved		
3	Reserved		R	0
2	CLKSEL	CT16Bn PCLK source. 0: HCLK 1: PLL_VCO	R/W	0
1	CRST	Counter Reset. 0: Disable counter reset. 1: Timer Counter and the Prescale Counter are synchronously reset on the next positive edge of PCLK. This is cleared by HW when the counter reset operation finishes.	R/W	0
0	CEN	Counter Enable 0: Disable Counter. 1: Enable Timer Counter and Prescale Counter for counting.	R/W	0

10.8.2 CT16Bn Timer Control register (CT16Bn_TMRCTRL) (n=1,3,4)

Address Offset: 0x00

✸ ***Note: CEN bit shall be set at last!***

Bit	Name	Description	Attribute	Reset
31:3	Reserved		R	0
2	CLKSEL	CT16Bn PCLK source. 0: HCLK 1: PLL_VCO	R/W	0
1	CRST	Counter Reset. 0: Disable counter reset. 1: Timer Counter and the Prescale Counter are synchronously reset on the next positive edge of PCLK. This is cleared by HW when the counter reset operation finishes.	R/W	0
0	CEN	Counter Enable 0: Disable Counter. 1: Enable Timer Counter and Prescale Counter for counting.	R/W	0

10.8.3 CT16Bn Timer Control register (CT16Bn_TMRCTRL) (n=5)

Address Offset: 0x00

✸ ***Note: CEN bit shall be set at last!***

Bit	Name	Description	Attribute	Reset
31:7	Reserved		R	0
6:4	CM[2:0]	Counting mode selection 000: Edge-aligned Up-counting mode 001: Edge-aligned Down-counting mode 010: Center-aligned mode 1. The match interrupt flag is set during the down-counting period 100: Center-aligned mode 2. The match interrupt flag is set during the up-counting period 110: Center-aligned mode 3. The match interrupt flag is set during both up-counting and down-counting period Other: Reserved	R/W	000b

3:2	CLKSEL[1:0]	CT16Bn PCLK source. 00: HCLK 01: PLL_VCO 10: ELS X'TAL 11: Reserved	R/W	00b
1	CRST	Counter Reset. 0: Disable counter reset. 1: Timer Counter and the Prescale Counter are synchronously reset on the next positive edge of PCLK. This is cleared by HW when the counter reset operation finishes.	R/W	0
0	CEN	Counter Enable 0: Disable Counter. 1: Enable Timer Counter and Prescale Counter for counting.	R/W	0

10.8.4 CT16Bn Timer Counter register (CT16Bn_TC) (n=0,1,2,3,4,5)

Address Offset: 0x04

In Edge-aligned up-counting mode (CM[2:0]=000b), unless it is reset before reaching its upper limit, the TC will count up to the value 0x0000FFFF and then wrap back to the value 0x00000000. This event does not cause an interrupt, but a Match register can be used to detect an overflow if needed.

In Edge-aligned down-counting mode (CM[2:0]=001b) , the TC[15:0] should be reset to the value of CT16Bn_MR3 after resetting counter (SW set CRST to 1).

Bit	Name	Description	Attribute	Reset
31:16	Reserved		R	0
15:0	TC[15:0]	Timer Counter	R/W	0

10.8.5 CT16Bn Prescale register (CT16Bn_PRE) (n=0,1,2,3,4,5)

Address Offset: 0x08

✸ ***Note: If Counter mode is selected in the CNTCTRL register, PRE[7:0] must be set to 0x0.***

Bit	Name	Description	Attribute	Reset
31:16	Reserved		R	0
15:0	PR[15:0]	Prescale max value.	R/W	0

10.8.6 CT16Bn Prescale Counter register (CT16Bn_PC) (n=0,1,2,3,4,5)

Address Offset: 0x0C

The 8-bit Prescale Counter controls division of PCLK by some constant value before it is applied to the Timer Counter. This allows control of the relationship between the resolution of the timer and the maximum time before the timer overflows. The Prescale Counter is incremented on every PCLK. When it reaches the value stored in the Prescale Register, the Timer Counter is incremented, and the Prescale Counter is reset on the next PCLK. This causes the TC to increment on every PCLK when PR = 0, every 2 PCLKs when PR = 1, etc.

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7:0	PC[7:0]	Prescale Counter	R/W	0

10.8.7 CT16Bn Count Control register (CT16Bn_CNTCTRL) (n=0,1,2,3,4,5)

Address Offset: 0x10

This register is used to select between Timer and Counter mode, and in Counter mode to select the pin and edges for counting.

When Counter Mode is chosen as a mode of operation, the CAP input (selected by the CIS bits) is sampled on every rising edge of the PCLK clock. After comparing two consecutive samples of this CAP input, one of the following four events is recognized: rising edge, falling edge, either of edges or no changes in the level of the selected CAP input. Only if the identified event occurs, and the event corresponds to the one selected by CTM bits in this register, will the Timer Counter register be incremented.

Effective processing of the externally supplied clock to the counter has some limitations. Since two successive rising edges of the PCLK clock are used to identify only one edge on the CAP selected input, the frequency of the CAP input cannot exceed one half of the PCLK clock. Consequently, the duration of the HIGH/LOW levels on the same CAP input in this case cannot be shorter than 1/ (2 x PCLK).

✸ ***Note: If Counter mode is selected in the CNTCTRL register, bit 2 to 0 of Capture Control (CAPCTRL) register and bit 7 to 0 of Prescale(PRE) register must be set to 0x0.***

Bit	Name	Description	Attribute	Reset
31:2	Reserved		R	0
1:0	CTM[1:0]	Counter/Timer Mode. This field selects which rising PCLK edges can increment Timer's Prescale Counter (PC), or clear PC and increment Timer Counter (TC). 00: Timer Mode: every rising PCLK edge 01: Counter Mode: TC is incremented on rising edges on the CAP0 input 10: Counter Mode: TC is incremented on falling edges on the CAP0 input 11: Counter Mode: TC is incremented on both edges on the CAP0 input	R/W	0

10.8.8 CT16Bn Match Control register (CT16Bn_MCTRL) (n=0,2,5)

Address Offset: 0x14

✸ ***Note: When the dead-band function is enabled in Center-aligned mode, and MR9RST=1, CT16Bn_PWMxN will always output "0"***

✸ ***Note: When the dead-band function is enabled***
- ***System will reset TC refer to MR9RST ONLY in Up-counting mode***
- ***In Down counting mode, TC[15:0] will be reloaded from CT16Bn_MR9 after resetting counter***
- ***System will reset TC refer to MR9RST ONLY in Center-aligned mode***

Bit	Name	Description	Attribute	Reset
31:24	PWMKEY[7:0]	PWM register key. Read as 0. When writing to the register you must write 0x5A to PWMKEY, otherwise behaviour of writing to the register is ignored.	W	0
23	MR9STOP	Stop MR9: TC and PC will stop and CEN bit will be cleared if MR9 matches TC. 0: Disable 1: Enable	R/W	0
22	MR9RST	Enable reset TC when MR9 matches TC. 0: Disable 1: Enable	R/W	0
21	MR9IE	Enable generating an interrupt based on CM[2:0] when MR9 matches the value in the TC.	R/W	0

		0: Disable 1: Enable		
20:12	Reserved		R	0
11	MR3STOP	Stop MR3: TC and PC will stop and CEN bit will be cleared if MR3 matches TC. 0: Disable 1: Enable	R/W	0
10	MR3RST	Enable reset TC when MR3 matches TC. 0: Disable 1: Enable	R/W	0
9	MR3IE	Enable generating an interrupt based on CM[2:0] when MR3 matches the value in the TC. 0: Disable 1: Enable	R/W	0
8	MR2STOP	Stop MR2: TC and PC will stop and CEN bit will be cleared if MR2 matches TC. 0: Disable 1: Enable	R/W	0
7	MR2RST	Enable reset TC when MR2 matches TC. 0: Disable 1: Enable	R/W	0
6	MR2IE	Enable generating an interrupt based on CM[2:0] when MR2 matches the value in the TC. 0: Disable 1: Enable	R/W	0
5	MR1STOP	Stop MR1: TC and PC will stop and CEN bit will be cleared if MR1 matches TC. 0: Disable 1: Enable	R/W	0
4	MR1RST	Enable reset TC when MR1 matches TC. 0: Disable 1: Enable	R/W	0
3	MR1IE	Enable generating an interrupt based on CM[2:0] when MR1 matches the value in the TC. 0: Disable 1: Enable	R/W	0
2	MR0STOP	Stop MR0: TC and PC will stop and CEN bit will be cleared if MR0 matches TC. 0: Disable 1: Enable	R/W	0
1	MR0RST	Enable reset TC when MR0 matches TC. 0: Disable 1: Enable	R/W	0
0	MR0IE	Enable generating an interrupt based on CM[2:0] when MR0 matches the value in the TC. 0: Disable 1: Enable	R/W	0

10.8.9 CT16Bn Match Control register (CT16Bn_MCTRL) (n=3,4)

Address Offset: 0x14

- ***Note: When the dead-band function is enabled in Center-aligned mode, and MR9RST=1, CT16Bn_PWMxN will always output "0"***
- ***Note: When the dead-band function is enabled***
  - ***System will reset TC refer to MR9RST ONLY in Up-counting mode***
  - ***In Down counting mode, TC[15:0] will be reloaded from CT16Bn_MR9 after resetting counter***
  - ***System will reset TC refer to MR9RST ONLY in Center-aligned mode***

Bit	Name	Description	Attribute	Reset
31:24	PWMKEY[7:0]	PWM register key. Read as 0. When writing to the register you must write 0x5A to PWMKEY, otherwise behaviour of writing to the register is ignored.	W	0
23	MR9STOP	Stop MR9: TC and PC will stop and CEN bit will be cleared if MR9 matches TC. 0: Disable 1: Enable	R/W	0
22	MR9RST	Enable reset TC when MR9 matches TC. 0: Disable 1: Enable	R/W	0
21	MR9IE	Enable generating an interrupt based on CM[2:0] when MR9 matches the value in the TC. 0: Disable 1: Enable	R/W	0
20:6	Reserved		R	0
5	MR1STOP	Stop MR1: TC and PC will stop and CEN bit will be cleared if MR1 matches TC. 0: Disable 1: Enable	R/W	0
4	MR1RST	Enable reset TC when MR1 matches TC. 0: Disable 1: Enable	R/W	0
3	MR1IE	Enable generating an interrupt based on CM[2:0] when MR1 matches the value in the TC. 0: Disable 1: Enable	R/W	0
2	MR0STOP	Stop MR0: TC and PC will stop and CEN bit will be cleared if MR0 matches TC. 0: Disable 1: Enable	R/W	0
1	MR0RST	Enable reset TC when MR0 matches TC. 0: Disable 1: Enable	R/W	0
0	MR0IE	Enable generating an interrupt based on CM[2:0] when MR0 matches the value in the TC. 0: Disable 1: Enable	R/W	0

10.8.10 CT16Bn Match Control register (CT16Bn_MCTRL) (n=1)

Address Offset: 0x14

✸ ***Note: When the dead-band function is enabled in Center-aligned mode, and MR12RST=1, CT16B1_PWMxN will always output "0"***

✸ ***Note: When the dead-band function is enabled***
- ***System will reset TC refer to MR12RST ONLY in Up-counting mode***
- ***In Down counting mode, TC[15:0] will be reloaded from CT16Bn_MR12 after resetting counter***
- ***System will reset TC refer to MR12RST ONLY in Center-aligned mode***

Bit	Name	Description	Attribute	Reset
31:30	Reserved		R	0
29	MR9STOP	Stop MR9: TC and PC will stop and CEN bit will be cleared if MR9 matches TC. 0: Disable	R/W	0

		1: Enable		
28	MR9RST	Enable reset TC when MR9 matches TC. 0: Disable 1: Enable	R/W	0
27	MR9IE	Enable generating an interrupt when MR9 matches the value in the TC. 0: Disable 1: Enable	R/W	0
26	MR8STOP	Stop MR8: TC and PC will stop and CEN bit will be cleared if MR8 matches TC. 0: Disable 1: Enable	R/W	0
25	MR8RST	Enable reset TC when MR8 matches TC. 0: Disable 1: Enable	R/W	0
24	MR8IE	Enable generating an interrupt when MR8 matches the value in the TC. 0: Disable 1: Enable	R/W	0
23	MR7STOP	Stop MR7: TC and PC will stop and CEN bit will be cleared if MR7 matches TC. 0: Disable 1: Enable	R/W	0
22	MR7RST	Enable reset TC when MR7 matches TC. 0: Disable 1: Enable	R/W	0
21	MR7IE	Enable generating an interrupt when MR7 matches the value in the TC. 0: Disable 1: Enable	R/W	0
20	MR6STOP	Stop MR6: TC and PC will stop and CEN bit will be cleared if MR6 matches TC. 0: Disable 1: Enable	R/W	0
19	MR6RST	Enable reset TC when MR6 matches TC. 0: Disable 1: Enable	R/W	0
18	MR6IE	Enable generating an interrupt when MR6 matches the value in the TC. 0: Disable 1: Enable	R/W	0
17	MR5STOP	Stop MR5: TC and PC will stop and CEN bit will be cleared if MR5 matches TC. 0: Disable 1: Enable	R/W	0
16	MR5RST	Enable reset TC when MR5 matches TC. 0: Disable 1: Enable	R/W	0
15	MR5IE	Enable generating an interrupt when MR5 matches the value in the TC. 0: Disable 1: Enable	R/W	0
14	MR4STOP	Stop MR4: TC and PC will stop and CEN bit will be cleared if MR4 matches TC. 0: Disable 1: Enable	R/W	0
13	MR4RST	Enable reset TC when MR4 matches TC. 0: Disable 1: Enable	R/W	0
12	MR4IE	Enable generating an interrupt when MR4 matches the value in the TC. 0: Disable 1: Enable	R/W	0
11	MR3STOP	Stop MR3: TC and PC will stop and CEN bit will be cleared if MR3 matches TC. 0: Disable 1: Enable	R/W	0
10	MR3RST	Enable reset TC when MR3 matches TC. 0: Disable 1: Enable	R/W	0

9	MR3IE	Enable generating an interrupt when MR3 matches the value in the TC. 0: Disable 1: Enable	R/W	0
8	MR2STOP	Stop MR2: TC and PC will stop and CEN bit will be cleared if MR2 matches TC. 0: Disable 1: Enable	R/W	0
7	MR2RST	Enable reset TC when MR2 matches TC. 0: Disable 1: Enable	R/W	0
6	MR2IE	Enable generating an interrupt when MR2 matches the value in the TC. 0: Disable 1: Enable	R/W	0
5	MR1STOP	Stop MR1: TC and PC will stop and CEN bit will be cleared if MR1 matches TC. 0: Disable 1: Enable	R/W	0
4	MR1RST	Enable reset TC when MR1 matches TC. 0: Disable 1: Enable	R/W	0
3	MR1IE	Enable generating an interrupt when MR1 matches the value in the TC. 0: Disable 1: Enable	R/W	0
2	MR0STOP	Stop MR0: TC and PC will stop and CEN bit will be cleared if MR0 matches TC. 0: Disable 1: Enable	R/W	0
1	MR0RST	Enable reset TC when MR0 matches TC. 0: Disable 1: Enable	R/W	0
0	MR0IE	Enable generating an interrupt when MR0 matches the value in the TC. 0: Disable 1: Enable	R/W	0

10.8.11 CT16Bn Match Control register 2 (CT16Bn_MCTRL2) (n=1)

Address Offset: 0x18

✸ ***Note: When the dead-band function is enabled in Center-aligned mode, and MR12RST=1, CT16B1_PWMxN will always output "0"***

✸ ***Note: When the dead-band function is enabled***
- ***System will reset TC refer to MR12RST ONLY in Up-counting mode***
- ***In Down counting mode, TC[15:0] will be reloaded from CT16Bn_MR12 after resetting counter***
- ***System will reset TC refer to MR12RST ONLY in Center-aligned mode***

Bit	Name	Description	Attribute	Reset
31:9	Reserved		R	0
8	MR12STOP	Stop MR12: TC and PC will stop and CEN bit will be cleared if MR12 matches TC. 0: Disable 1: Enable	R/W	0
7	MR12RST	Enable reset TC when MR12 matches TC. 0: Disable 1: Enable	R/W	0
6	MR12IE	Enable generating an interrupt based on CM[2:0] when MR12 matches the value in the TC. 0: Disable 1: Enable	R/W	0

5	MR11STOP	Stop MR11: TC and PC will stop and CEN bit will be cleared if MR11 matches TC. 0: Disable 1: Enable	R/W	0
4	MR11RST	Enable reset TC when MR11 matches TC. 0: Disable 1: Enable	R/W	0
3	MR11IE	Enable generating an interrupt when MR11 matches the value in the TC. 0: Disable 1: Enable	R/W	0
2	MR10STOP	Stop MR10: TC and PC will stop and CEN bit will be cleared if MR10 matches TC. 0: Disable 1: Enable	R/W	0
1	MR10RST	Enable reset TC when MR10 matches TC. 0: Disable 1: Enable	R/W	0
0	MR10IE	Enable generating an interrupt when MR10 matches the value in the TC. 0: Disable 1: Enable	R/W	0

10.8.12 CT16Bn Match register 0~1 (CT16Bn_MR0~1) (n=0,2,3,4,5)

Address Offset: 0x20, 0x24

The Match register values are continuously compared to the Timer Counter (TC) value. When the two values are equal, actions can be triggered automatically. The action possibilities are to generate an interrupt, reset the Timer Counter, or stop the timer. Actions are controlled by the settings in the CT16Bn_MCTRL register.

Bit	Name	Description	Attribute	Reset
31:24	PWMKEY[7:0]	PWM register key. Read as 0. When writing to the register you must write 0x5A to PWMKEY, otherwise behaviour of writing to the register is ignored.	W	0
23:16	Reserved		R	0
15:0	MR[15:0]	Timer counter match value	R/W	0

10.8.13 CT16Bn Match register 2~3 (CT16Bn_MR2~3) (n=0,2,5)

Address Offset: 0x28, 0x2C

The Match register values are continuously compared to the Timer Counter (TC) value. When the two values are equal, actions can be triggered automatically. The action possibilities are to generate an interrupt, reset the Timer Counter, or stop the timer. Actions are controlled by the settings in the CT16Bn_MCTRL register.

Bit	Name	Description	Attribute	Reset
31:24	PWMKEY[7:0]	PWM register key. Read as 0. When writing to the register you must write 0x5A to PWMKEY, otherwise behaviour of writing to the register is ignored.	W	0
23:16	Reserved		R	0
15:0	MR[15:0]	Timer counter match value	R/W	0

10.8.14 CT16Bn Match register 9 (CT16Bn_MR9) (n=0,2,3,4,5)

Address Offset: 0x44

The Match register values are continuously compared to the Timer Counter (TC) value. When the two values are equal, actions can be triggered automatically. The action possibilities are to generate an interrupt, reset the Timer Counter, or stop the timer. Actions are controlled by the settings in the CT16Bn_MCTRL register.

Bit	Name	Description	Attribute	Reset
31:24	PWMKEY[7:0]	PWM register key. Read as 0. When writing to the register you must write 0x5A to PWMKEY, otherwise behaviour of writing to the register is ignored.	W	0
23:16	Reserved		R	0
15:0	MR[15:0]	Timer counter match value	R/W	0

10.8.15 CT16Bn Match register 0~11 (CT16Bn_MR0~11) (n=1)

Address Offset: 0x20, 0x24, 0x28, 0x2C, 0x30, 0x34, 0x38, 0x3C, 0x40, 0x44, 0x48, 0x4C

The Match register values are continuously compared to the Timer Counter (TC) value. When the two values are equal, actions can be triggered automatically. The action possibilities are to generate an interrupt, reset the Timer Counter, or stop the timer. Actions are controlled by the settings in the CT16Bn_MCTRL register.

Bit	Name	Description	Attribute	Reset
31:16	Reserved		R	0
15:0	MR[15:0]	Timer counter match value	R/W	0

10.8.16 CT16Bn Match register 12 (CT16Bn_MR12) (n=1)

Address Offset: 0x50

The Match register values are continuously compared to the Timer Counter (TC) value. When the two values are equal, actions can be triggered automatically. The action possibilities are to generate an interrupt, reset the Timer Counter, or stop the timer. Actions are controlled by the settings in the CT16Bn_MCTRL register.

Bit	Name	Description	Attribute	Reset
31:16	Reserved		R	0
15:0	MR[15:0]	Timer counter match value	R/W	0

10.8.17 CT16Bn Capture Control register (CT16Bn_CAPCTRL) (n=0,1,2,3,4,5)

Address Offset: 0x84

The Capture Control register is used to control whether the Capture register is loaded with the value in the Counter/timer when the capture event occurs, and whether an interrupt is generated by the capture event. Setting both the rising and falling bits at the same time is a valid configuration, resulting in a capture event for both edges.

✸ ***Note: HW will switch I/O Configuration directly when CAP0EN=1.***

Bit	Name	Description	Attribute	Reset
31:4	Reserved		R	0
3	CAP0EN	Capture 0 function enable bit 0: Disable 1: Enable.	R/W	0
2	CAP0IE	Interrupt on CT16Bn_CAP0 event: a CAP0 load due to a CT16Bn_CAP0 event will generate an interrupt. 0: Disable 1: Enable	R/W	0
1	CAP0FE	Capture on CT16Bn_CAP0 falling edge: a sequence of 1 then 0 on CT16Bn_CAP0 will cause CAP0 to be loaded with the contents of TC. 0: Disable 1: Enable	R/W	0
0	CAP0RE	Capture on CT16Bn_CAP0 rising edge: a sequence of 0 then 1 on CT16Bn_CAP0 will cause CAP0 to be loaded with the contents of TC. 0: Disable 1: Enable	R/W	0

10.8.18 CT16Bn Capture 0 register (CT16Bn_CAP0) (n=0,1,2,3,4,5)

Address Offset: 0x88

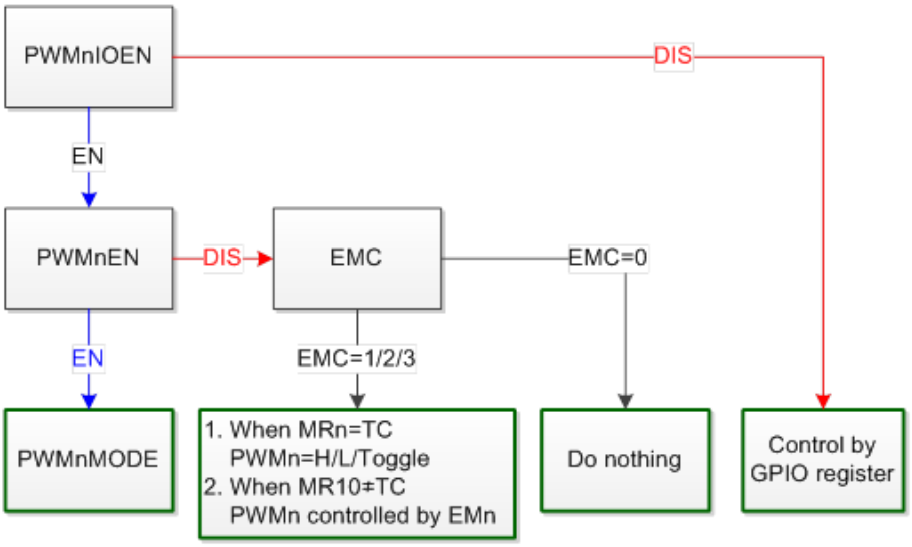
Each Capture register is associated with a device pin and may be loaded with the counter/timer value when a specified event occurs on that pin. The settings in the Capture Control register determine whether the capture function is enabled, and whether a capture event happens on the rising edge of the associated pin, the falling edge, or on both edges.

Bit	Name	Description	Attribute	Reset
31:16	Reserved		R	0
15:0	CAP0[15:0]	Timer counter capture value	R	0

10.8.19 CT16Bn External Match register (CT16Bn_EM) (n=0,2,5)

Address Offset: 0x8C

The External Match register provides both control and status of CT16Bn_PWM[2:0]. If the match outputs are configured as PWM output, the function of the external match registers is determined by the PWM rules.

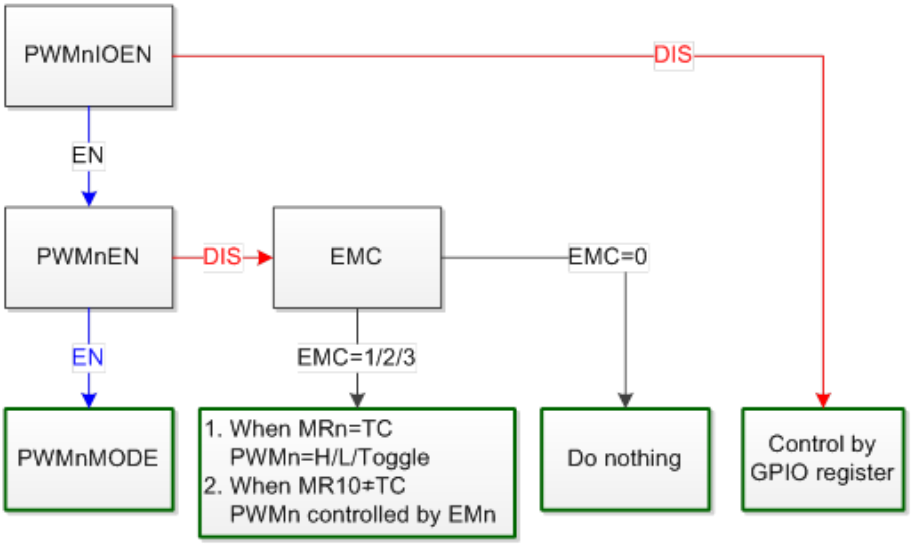


Bit	Name	Description	Attribute	Reset
31:24	PWMKEY[7:0]	PWM register key. Read as 0. When writing to the register you must write 0x5A to PWMKEY, otherwise behaviour of writing to the register is ignored.	W	0
23:12	Reserved		R	0
11:10	EMC3[1:0]	Determines the functionality of CT16Bn_PWM3 when MR3=TC. 00: Do Nothing. 01: CT16Bn_PWM3 pin is LOW 10: CT16Bn_PWM3 pin is HIGH 11: Toggle CT16Bn_PWM3 pin.	R/W	0
9:8	EMC2[1:0]	Determines the functionality of CT16Bn_PWM2 when MR2=TC. 00: Do Nothing. 01: CT16Bn_PWM2 pin is LOW 10: CT16Bn_PWM2 pin is HIGH 11: Toggle CT16Bn_PWM2 pin.	R/W	0
7:6	EMC1[1:0]	Determines the functionality of CT16Bn_PWM1 when MR1=TC. 00: Do Nothing. 01: CT16Bn_PWM1 pin is LOW 10: CT16Bn_PWM1 pin is HIGH. 11: Toggle CT16Bn_PWM1 pin.	R/W	0
5:4	EMC0[1:0]	Determines the functionality of CT16Bn_PWM0 when MR0=TC. 00: Do Nothing. 01: CT16Bn_PWM0 pin is LOW 10: CT16Bn_PWM0 pin is HIGH 11: Toggle CT16Bn_PWM0 pin.	R/W	0
3	EM3	When EMC3≠00b and MR3≠TC, this bit will drive the state of CT16Bn_PWM3 output.	R/W	0
2	EM2	When EMC2≠00b and MR2≠TC, this bit will drive the state of CT16Bn_PWM2 output.	R/W	0
1	EM1	When EMC1≠00b and MR1≠TC, this bit will drive the state of CT16Bn_PWM1 output.	R/W	0
0	EM0	When EMC0≠00b and MR0≠TC, this bit will drive the state of CT16Bn_PWM0 output.	R/W	0

10.8.20 CT16Bn External Match register (CT16Bn_EM) (n=3,4)

Address Offset: 0x8C

The External Match register provides both control and status of CT16Bn_PWM[2:0]. If the match outputs are configured as PWM output, the function of the external match registers is determined by the PWM rules.

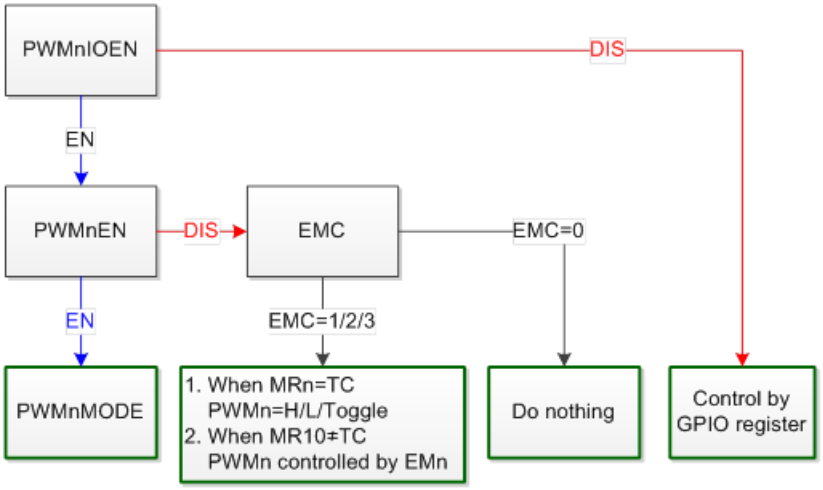


Bit	Name	Description	Attribute	Reset
31:24	PWMKEY[7:0]	PWM register key. Read as 0. When writing to the register you must write 0x5A to PWMKEY, otherwise behaviour of writing to the register is ignored.	W	0
23:8	Reserved		R	0
7:6	EMC1[1:0]	Determines the functionality of CT16Bn_PWM1 when MR1=TC. 00: Do Nothing. 01: CT16Bn_PWM1 pin is LOW 10: CT16Bn_PWM1 pin is HIGH. 11: Toggle CT16Bn_PWM1 pin.	R/W	0
5:4	EMC0[1:0]	Determines the functionality of CT16Bn_PWM0 when MR0=TC. 00: Do Nothing. 01: CT16Bn_PWM0 pin is LOW 10: CT16Bn_PWM0 pin is HIGH 11: Toggle CT16Bn_PWM0 pin.	R/W	0
3:2	Reserved		R	0
1	EM1	When EMC1≠00b and MR1≠TC, this bit will drive the state of CT16Bn_PWM1 output.	R/W	0
0	EM0	When EMC0≠00b and MR0≠TC, this bit will drive the state of CT16Bn_PWM0 output.	R/W	0

10.8.21 CT16Bn External Match register (CT16Bn_EM) (n=1)

Address Offset: 0x8C

The External Match register provides both control and status of CT16B1_PWM[11:0]. If the match outputs are configured as PWM output, the function of the external match registers is determined by the PWM rules.

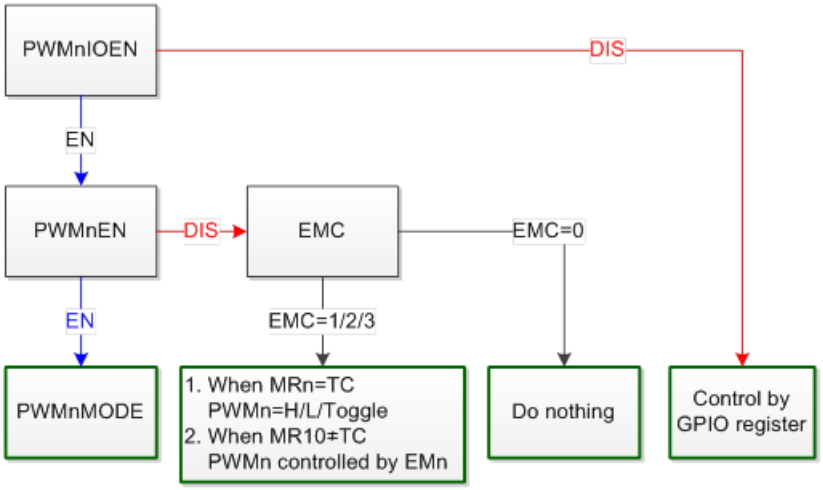


Bit	Name	Description	Attribute	Reset
31:12	Reserved		R	0
11	EM11	When EMC11≠00b and MR11≠TC, this bit will drive the state of CT16Bn_PWM11 output.	R/W	0
10	EM10	When EMC10≠00b and MR10≠TC, this bit will drive the state of CT16Bn_PWM10 output.	R/W	0
9	EM9	When EMC9≠00b and MR9≠TC, this bit will drive the state of CT16Bn_PWM9 output.	R/W	0
8	EM8	When EMC8≠00b and MR8≠TC, this bit will drive the state of CT16Bn_PWM8 output.	R/W	0
7	EM7	When EMC7≠00b and MR7≠TC, this bit will drive the state of CT16Bn_PWM7 output.	R/W	0
6	EM6	When EMC6≠00b and MR6≠TC, this bit will drive the state of CT16Bn_PWM6 output.	R/W	0
5	EM5	When EMC5≠00b and MR5≠TC, this bit will drive the state of CT16Bn_PWM5 output.	R/W	0
4	EM4	When EMC4≠00b and MR4≠TC, this bit will drive the state of CT16Bn_PWM4 output.	R/W	0
3	EM3	When EMC3≠00b and MR3≠TC, this bit will drive the state of CT16Bn_PWM3 output.	R/W	0
2	EM2	When EMC2≠00b and MR2≠TC, this bit will drive the state of CT16Bn_PWM2 output.	R/W	0
1	EM1	When EMC1≠00b and MR1≠TC, this bit will drive the state of CT16Bn_PWM1 output.	R/W	0
0	EM0	When EMC0≠00b and MR0≠TC, this bit will drive the state of CT16Bn_PWM0 output.	R/W	0

10.8.22 CT16Bn External Match Control register (CT16Bn_EMC) (n=1)

Address Offset: 0x90

The External Match Control register provides control of CT16B1_PWM[11:0]. If the match outputs are configured as PWM output, the function of the external match registers is determined by the PWM rules.



Bit	Name	Description	Attribute	Reset
31:24	Reserved		R	0
23:22	EMC11[1:0]	Determines the functionality of CT16Bn_PWM11 when MR11=TC. 00: Do Nothing. 01: CT16Bn_PWM11 pin is LOW. 10: CT16Bn_PWM11 pin is HIGH. 11: Toggle CT16Bn_PWM11 pin.	R/W	0
21:20	EMC10[1:0]	Determines the functionality of CT16Bn_PWM10 when MR10=TC. 00: Do Nothing. 01: CT16Bn_PWM10 pin is LOW. 10: CT16Bn_PWM10 pin is HIGH. 11: Toggle CT16Bn_PWM10 pin.	R/W	0
19:18	EMC9[1:0]	Determines the functionality of CT16Bn_PWM9 when MR9=TC. 00: Do Nothing. 01: CT16Bn_PWM9 pin is LOW. 10: CT16Bn_PWM9 pin is HIGH. 11: Toggle CT16Bn_PWM9 pin.	R/W	0
17:16	EMC8[1:0]	Determines the functionality of CT16Bn_PWM8 when MR8=TC. 00: Do Nothing. 01: CT16Bn_PWM8 pin is LOW. 10: CT16Bn_PWM8 pin is HIGH. 11: Toggle CT16Bn_PWM8 pin.	R/W	0
15:14	EMC7[1:0]	Determines the functionality of CT16Bn_PWM7 when MR7=TC. 00: Do Nothing. 01: CT16Bn_PWM7 pin is LOW. 10: CT16Bn_PWM7 pin is HIGH. 11: Toggle CT16Bn_PWM7 pin.	R/W	0
13:12	EMC6[1:0]	Determines the functionality of CT16Bn_PWM6 when MR6=TC. 00: Do Nothing. 01: CT16Bn_PWM6 pin is LOW. 10: CT16Bn_PWM6 pin is HIGH. 11: Toggle CT16Bn_PWM6 pin.	R/W	0
:10	EMC5[1:0]	Determines the functionality of CT16Bn_PWM5 when MR5=TC. 00: Do Nothing. 01: CT16Bn_PWM5 pin is LOW. 10: CT16Bn_PWM5 pin is HIGH. 11: Toggle CT16Bn_PWM5 pin.	R/W	0

9:8	EMC4[1:0]	Determines the functionality of CT16Bn_PWM4 when MR4=TC. 00: Do Nothing. 01: CT16Bn_PWM4 pin is LOW. 10: CT16Bn_PWM4 pin is HIGH. 11: Toggle CT16Bn_PWM4 pin.	R/W	0
7:6	EMC3[1:0]	Determines the functionality of CT16Bn_PWM3 when MR3=TC. 00: Do Nothing. 01: CT16Bn_PWM3 pin is LOW. 10: CT16Bn_PWM3 pin is HIGH. 11: Toggle CT16Bn_PWM3 pin.	R/W	0
5:4	EMC2[1:0]	Determines the functionality of CT16Bn_PWM2 when MR2=TC. 00: Do Nothing. 01: CT16Bn_PWM2 pin is LOW. 10: CT16Bn_PWM2 pin is HIGH. 11: Toggle CT16Bn_PWM2 pin.	R/W	0
3:2	EMC1[1:0]	Determines the functionality of CT16Bn_PWM1 when MR1=TC. 00: Do Nothing. 01: CT16Bn_PWM1 pin is LOW. 10: CT16Bn_PWM1 pin is HIGH. 11: Toggle CT16Bn_PWM1 pin.	R/W	0
1:0	EMC0[1:0]	Determines the functionality of CT16Bn_PWM0 when MR0=TC. 00: Do Nothing. 01: CT16Bn_PWM0 pin is LOW. 10: CT16Bn_PWM0 pin is HIGH. 11: Toggle CT16Bn_PWM0 pin.	R/W	0

10.8.23 CT16Bn PWM Control register (CT16Bn_PWMCTRL) (n=0,2,5)

Address Offset: 0x98

The PWM Control register is used to configure the match outputs as PWM outputs. Each match output can be independently set to perform either as PWM output or as match output whose function is controlled by CT16Bn_EM register.

For CT16B0/2/5, a maximum of 4 single edge controlled PWM outputs can be selected on the CT16Bn_PWMCTRL[3:0] outputs. One additional match register determines the PWM cycle length. When a match occurs in any of the other match registers, the PWM output is set to HIGH. The timer is reset by the match register that is configured to set the PWM cycle length. When the timer is reset to zero, all currently HIGH match outputs configured as PWM outputs are cleared.

Bit	Name	Description	Attribute	Reset
31:24	PWMKEY[7:0]	PWM register key. Read as 0. When writing to the register you must write 0x5A to PWMKEY, otherwise behaviour of writing to the register is ignored.	W	0
23	PWM3IOEN	CT16Bn_PWM3/GPIO selection bit 0: CT16Bn_PWM3 pin act as GPIO 1: CT16Bn_PWM3 pin act as match output, and output signal depends on PWM3EN bit.	R/W	0
22	PWM2IOEN	CT16Bn_PWM2/GPIO selection bit 0: CT16Bn_PWM2 pin act as GPIO 1: CT16Bn_PWM2 pin act as match output, and output signal depends on PWM2EN bit.	R/W	0
21	PWM1IOEN	CT16Bn_PWM1/GPIO selection bit 0: CT16Bn_PWM1 pin act as GPIO 1: CT16Bn_PWM1 pin act as match output, and output signal depends on PWM1EN bit.	R/W	0
20	PWM0IOEN	CT16Bn_PWM0/GPIO selection bit 0: CT16Bn_PWM0 pin act as GPIO 1: CT16Bn_PWM0 pin act as match output, and output signal depends on PWM0EN bit.	R/W	0

19:12	Reserved		R	0
11:10	PWM3MODE[1:0]	PWM3 output mode 00: PWM mode 1 PWM3 is 0 when TC<MR3 during Up-counting period PWM3 is 0 when TC≤MR3 during Down-counting period 01: PWM mode 2 PWM3 is 1 when TC<MR3 during Up-counting period PWM3 is 1 when TC≤MR3 during Down-counting period 10: PWM3 is forced to 0. 11: PWM3 is forced to 1.	R/W	0
9:8	PWM2MODE[1:0]	PWM2 output mode 00: PWM mode 1 PWM2 is 0 when TC<MR2 during Up-counting period PWM2 is 0 when TC≤MR2 during Down-counting period 01: PWM mode 2 PWM2 is 1 when TC<MR2 during Up-counting period PWM2 is 1 when TC≤MR2 during Down-counting period 10: PWM2 is forced to 0. 11: PWM2 is forced to 1.	R/W	0
7:6	PWM1MODE[1:0]	PWM1 output mode 00: PWM mode 1 PWM1 is 0 when TC<MR1 during Up-counting period PWM1 is 0 when TC≤MR1 during Down-counting period 01: PWM mode 2 PWM1 is 1 when TC<MR1 during Up-counting period PWM1 is 1 when TC≤MR1 during Down-counting period 10: PWM1 is forced to 0. 11: PWM1 is forced to 1.	R/W	0
5:4	PWM0MODE[1:0]	PWM0 output mode 00: PWM mode 1 PWM0 is 0 when TC<MR0 during Up-counting period PWM0 is 0 when TC≤MR0 during Down-counting period 01: PWM mode 2 PWM0 is 1 when TC<MR0 during Up-counting period PWM0 is 1 when TC≤MR0 during Down-counting period 10: PWM0 is forced to 0. 11: PWM0 is forced to 1.	R/W	0
3	PWM3EN	PWM3 enable 0: CT16Bn_PWM3 is controlled by EMC3. 1: PWM mode is enabled for CT16Bn_PWM3.	R/W	0
2	PWM2EN	PWM2 enable 0: CT16Bn_PWM2 is controlled by EMC2. 1: PWM mode is enabled for CT16Bn_PWM2.	R/W	0
1	PWM1EN	PWM1 enable 0: CT16Bn_PWM1 is controlled by EMC1. 1: PWM mode is enabled for CT16Bn_PWM1.	R/W	0
0	PWM0EN	PWM0 enable 0: CT16Bn_PWM0 is controlled by EMC0. 1: PWM mode is enabled for CT16Bn_PWM0.	R/W	0

10.8.24 CT16Bn PWM Control register (CT16Bn_PWMCTRL) (n=3,4)

Address Offset: 0x98

The PWM Control register is used to configure the match outputs as PWM outputs. Each match output can be independently set to perform either as PWM output or as match output whose function is controlled by CT16Bn_EM register.

For CT16B3/4, a maximum of 2 single edge controlled PWM outputs can be selected on the CT16Bn_PWMCTRL[1:0] outputs. One additional match register determines the PWM cycle length. When a match occurs in any of the other match registers, the PWM output is set to HIGH. The timer is reset by the match register that is configured to set the PWM cycle length. When the timer is reset to zero, all currently HIGH match outputs configured as PWM outputs are cleared.

Bit	Name	Description	Attribute	Reset
31:22	PWMKEY[7:0]	PWM register key. Read as 0. When writing to the register you must write 0x5A to PWMKEY, otherwise behaviour of writing to the register is ignored.	W	0
21	PWM1IOEN	CT16Bn_PWM1/GPIO selection bit 0: CT16Bn_PWM1 pin act as GPIO 1: CT16Bn_PWM1 pin act as match output, and output signal depends on PWM1EN bit.	R/W	0
20	PWM0IOEN	CT16Bn_PWM0/GPIO selection bit 0: CT16Bn_PWM0 pin act as GPIO 1: CT16Bn_PWM0 pin act as match output, and output signal depends on PWM0EN bit.	R/W	0
19:8	Reserved		R	0
7:6	PWM1MODE[1:0]	PWM1 output mode 00: PWM mode 1 PWM1 is 0 when TC<MR1 during Up-counting period PWM1 is 0 when TC≤MR1 during Down-counting period 01: PWM mode 2 PWM1 is 1 when TC<MR1 during Up-counting period PWM1 is 1 when TC≤MR1 during Down-counting period 10: PWM1 is forced to 0. 11: PWM1 is forced to 1.	R/W	0
5:4	PWM0MODE[1:0]	PWM0 output mode 00: PWM mode 1 PWM0 is 0 when TC<MR0 during Up-counting period PWM0 is 0 when TC≤MR0 during Down-counting period 01: PWM mode 2 PWM0 is 1 when TC<MR0 during Up-counting period PWM0 is 1 when TC≤MR0 during Down-counting period 10: PWM0 is forced to 0. 11: PWM0 is forced to 1.	R/W	0
3:2	Reserved		R	0
1	PWM1EN	PWM1 enable 0: CT16Bn_PWM1 is controlled by EMC1. 1: PWM mode is enabled for CT16Bn_PWM1.	R/W	0
0	PWM0EN	PWM0 enable 0: CT16Bn_PWM0 is controlled by EMC0. 1: PWM mode is enabled for CT16Bn_PWM0.	R/W	0

10.8.25 CT16Bn PWM Control register (CT16Bn_PWMCTRL) (n=1)

Address Offset: 0x98

The PWM Control register is used to configure the match outputs as PWM outputs. Each match output can be independently set to perform either as PWM output or as match output whose function is controlled by CT16Bn_EM register.

For CT16B1, a maximum of 12 single edge controlled PWM outputs can be selected on the CT16Bn_PWMCTRL[11:0] outputs. One additional match register determines the PWM cycle length. When a match occurs in any of the other match registers, the PWM output is set to HIGH. The timer is reset by the match register that is configured to set the PWM cycle length. When the timer is reset to zero, all currently HIGH match outputs configured as PWM outputs are cleared.

Bit	Name	Description	Attribute	Reset
31:24	Reserved		R	0
23:22	PWM11MODE[1:0]	PWM11 output 00: PWM mode 1 PWM11 is 0 when TC<MR11 during Up-counting period 01: PWM mode 2	R/W	0

		PWM11 is 1 when TC<MR11 during Up-counting period 10: PWM11 is forced to 0. 11: PWM11 is forced to 1.		
21:20	PWM10MODE[1:0]	PWM10 output 00: PWM mode 1 PWM10 is 0 when TC<MR10 during Up-counting period 01: PWM mode 2 PWM10 is 1 when TC<MR10 during Up-counting period 10: PWM10 is forced to 0. 11: PWM10 is forced to 1.	R/W	0
19:18	PWM9MODE[1:0]	PWM9 output mode 00: PWM mode 1 PWM9 is 0 when TC<MR9 during Up-counting period PWM9 is 1 when TC<MR9 during Up-counting period 10: PWM9 is forced to 0. 11: PWM9 is forced to 1.	R/W	0
17:16	PWM8MODE[1:0]	PWM8 output mode 00: PWM mode 1 PWM8 is 0 when TC<MR8 during Up-counting period 01: PWM mode 2 PWM8 is 1 when TC<MR8 during Up-counting period 10: PWM8 is forced to 0. 11: PWM8 is forced to 1.	R/W	0
15:14	PWM7MODE[1:0]	PWM7 output mode 00: PWM mode 1 PWM7 is 0 when TC<MR7 during Up-counting period 01: PWM mode 2 PWM7 is 1 when TC<MR7 during Up-counting period 10: PWM7 is forced to 0. 11: PWM7 is forced to 1.	R/W	0
13:12	PWM6MODE[1:0]	PWM6 output mode 00: PWM mode 1 PWM6 is 0 when TC<MR6 during Up-counting period 01: PWM mode 2 PWM6 is 1 when TC<MR6 during Up-counting period 10: PWM6 is forced to 0. 11: PWM6 is forced to 1.	R/W	0
11:10	PWM5MODE[1:0]	PWM5 output 00: PWM mode 1 PWM5 is 0 when TC<MR5 during Up-counting period 01: PWM mode 2 PWM5 is 1 when TC<MR5 during Up-counting period 10: PWM5 is forced to 0. 11: PWM5 is forced to 1.	R/W	0
9:8	PWM4MODE[1:0]	PWM4 output 00: PWM mode 1 PWM4 is 0 when TC<MR4 during Up-counting period 01: PWM mode 2 PWM4 is 1 when TC<MR4 during Up-counting period 10: PWM4 is forced to 0. 11: PWM4 is forced to 1.	R/W	0
7:6	PWM3MODE[1:0]	PWM3 output mode 00: PWM mode 1 PWM3 is 0 when TC<MR3 during Up-counting period 01: PWM mode 2 PWM3 is 1 when TC<MR3 during Up-counting period 10: PWM3 is forced to 0. 11: PWM3 is forced to 1.	R/W	0
5:4	PWM2MODE[1:0]	PWM2 output mode 00: PWM mode 1 PWM2 is 0 when TC<MR2 during Up-counting period 01: PWM mode 2 PWM2 is 1 when TC<MR2 during Up-counting period 10: PWM2 is forced to 0. 11: PWM2 is forced to 1.	R/W	0
3:2	PWM1MODE[1:0]	PWM1 output mode	R/W	0

		00: PWM mode 1 PWM1 is 0 when TC<MR1 during Up-counting period 01: PWM mode 2 PWM1 is 1 when TC<MR1 during Up-counting period 10: PWM1 is forced to 0. 11: PWM1 is forced to 1.		
1:0	PWM0MODE[1:0]	PWM0 output mode 00: PWM mode 1 PWM0 is 0 when TC<MR0 during Up-counting period 01: PWM mode 2 PWM0 is 1 when TC<MR0 during Up-counting period 10: PWM0 is forced to 0. 11: PWM0 is forced to 1.	R/W	0

10.8.26 CT16Bn PWM Enable register (CT16Bn_PWMENB) (n=1)

Address Offset: 0xA0

The PWM Control register is used to configure the match outputs as PWM outputs. Each match output can be independently set to perform either as PWM output or as match output whose function is controlled by CT16Bn_EM register.

For CT16B1, a maximum of 12 single edge controlled PWM outputs can be selected on the CT16B1_PWMCTRL[11:0] outputs. One additional match register determines the PWM cycle length. When a match occurs in any of the other match registers, the PWM output is set to HIGH. The timer is reset by the match register that is configured to set the PWM cycle length. When the timer is reset to zero, all currently HIGH match outputs configured as PWM outputs are cleared.

Bit	Name	Description	Attribute	Reset
31:12	Reserved	-	R	0
11	PWM11EN	PWM11 enable 0: CT16Bn_PWM11 is controlled by EMC11. 1: PWM mode is enabled for CT16Bn_PWM11.	R/W	0
10	PWM10EN	PWM10 enable 0: CT16Bn_PWM10 is controlled by EMC10. 1: PWM mode is enabled for CT16Bn_PWM10.	R/W	0
9	PWM9EN	PWM9 enable 0: CT16Bn_PWM9 is controlled by EMC9. 1: PWM mode is enabled for CT16Bn_PWM9.	R/W	0
8	PWM8EN	PWM8 enable 0: CT16Bn_PWM8 is controlled by EMC8. 1: PWM mode is enabled for CT16Bn_PWM8.	R/W	0
7	PWM7EN	PWM7 enable 0: CT16Bn_PWM7 is controlled by EMC7. 1: PWM mode is enabled for CT16Bn_PWM7.	R/W	0
6	PWM6EN	PWM6 enable 0: CT16Bn_PWM6 is controlled by EMC6. 1: PWM mode is enabled for CT16Bn_PWM6.	R/W	0
5	PWM5EN	PWM5 enable 0: CT16Bn_PWM5 is controlled by EMC5. 1: PWM mode is enabled for CT16Bn_PWM5.	R/W	0
4	PWM4EN	PWM4 enable 0: CT16Bn_PWM4 is controlled by EMC4. 1: PWM mode is enabled for CT16Bn_PWM4.	R/W	0
3	PWM3EN	PWM3 enable 0: CT16Bn_PWM3 is controlled by EMC3. 1: PWM mode is enabled for CT16Bn_PWM3.	R/W	0
2	PWM2EN	PWM2 enable 0: CT16Bn_PWM2 is controlled by EMC2. 1: PWM mode is enabled for CT16Bn_PWM2.	R/W	0
1	PWM1EN	PWM1 enable 0: CT16Bn_PWM1 is controlled by EMC1. 1: PWM mode is enabled for CT16Bn_PWM1.	R/W	0

0	PWM0EN	PWM0 enable 0: CT16Bn_PWM0 is controlled by EMC0. 1: PWM mode is enabled for CT16Bn_PWM0.	R/W	0

10.8.27 CT16Bn PWM IO Enable register (CT16Bn_PWMIOENB) (n=1)

Address Offset: 0xA4

The PWM Control register is used to configure the match outputs as PWM outputs. Each match output can be independently set to perform either as PWM output or as match output whose function is controlled by CT16Bn_EM register.

For CT16B1, a maximum of 12 single edge controlled PWM outputs can be selected on the CT16Bn_PWMCTRL[11:0] outputs. One additional match register determines the PWM cycle length. When a match occurs in any of the other match registers, the PWM output is set to HIGH. The timer is reset by the match register that is configured to set the PWM cycle length. When the timer is reset to zero, all currently HIGH match outputs configured as PWM outputs are cleared.

Bit	Name	Description	Attribute	Reset
31:12	Reserved		R	0
11	PWM11IOEN	CT16Bn_PWM11/GPIO selection bit 0: CT16Bn_PWM11 pin act as GPIO 1: CT16Bn_PWM11 pin act as match output, and output signal depends on PWM11EN bit.	R/W	0
10	PWM10IOEN	CT16Bn_PWM10/GPIO selection bit 0: CT16Bn_PWM10 pin act as GPIO 1: CT16Bn_PWM10 pin act as match output, and output signal depends on PWM10EN bit.	R/W	0
9	PWM9IOEN	CT16Bn_PWM9/GPIO selection bit 0: CT16Bn_PWM9 pin act as GPIO 1: CT16Bn_PWM9 pin act as match output, and output signal depends on PWM9EN bit.	R/W	0
8	PWM8IOEN	CT16Bn_PWM8/GPIO selection bit 0: CT16Bn_PWM8 pin act as GPIO 1: CT16Bn_PWM8 pin act as match output, and output signal depends on PWM8EN bit.	R/W	0
7	PWM7IOEN	CT16Bn_PWM7/GPIO selection bit 0: CT16Bn_PWM7 pin act as GPIO 1: CT16Bn_PWM7 pin act as match output, and output signal depends on PWM7EN bit.	R/W	0
6	PWM6IOEN	CT16Bn_PWM6/GPIO selection bit 0: CT16Bn_PWM6 pin act as GPIO 1: CT16Bn_PWM6 pin act as match output, and output signal depends on PWM6EN bit.	R/W	0
5	PWM5IOEN	CT16Bn_PWM5/GPIO selection bit 0: CT16Bn_PWM5 pin act as GPIO 1: CT16Bn_PWM5 pin act as match output, and output signal depends on PWM5EN bit.	R/W	0
4	PWM4IOEN	CT16Bn_PWM4/GPIO selection bit 0: CT16Bn_PWM4 pin act as GPIO 1: CT16Bn_PWM4 pin act as match output, and output signal depends on PWM4EN bit.	R/W	0
3	PWM3IOEN	CT16Bn_PWM3/GPIO selection bit 0: CT16Bn_PWM3 pin act as GPIO 1: CT16Bn_PWM3 pin act as match output, and output signal depends on PWM3EN bit.	R/W	0
2	PWM2IOEN	CT16Bn_PWM2/GPIO selection bit 0: CT16Bn_PWM2 pin act as GPIO	R/W	0

		1: CT16Bn_PWM2 pin act as match output, and output signal depends on PWM2EN bit.		
1	PWM1IOEN	CT16Bn_PWM1/GPIO selection bit 0: CT16Bn_PWM1 pin act as GPIO 1: CT16Bn_PWM1 pin act as match output, and output signal depends on PWM1EN bit.	R/W	0
0	PWM0IOEN	CT16Bn_PWM0/GPIO selection bit 0: CT16Bn_PWM0 pin act as GPIO 1: CT16Bn_PWM0 pin act as match output, and output signal depends on PWM0EN bit.	R/W	0

10.8.28 CT16Bn Timer Raw Interrupt Status register (CT16Bn_RIS) (n=0,2,5)

Address Offset: 0xA8

This register indicates the raw status for Timer/PWM interrupts. A Timer/PWM interrupt is sent to the interrupt controller if the corresponding bit in the CT16Bn_IE register is set.

Bit	Name	Description	Attribute	Reset
31:6	Reserved		R	0
5	MR9IF	Interrupt flag for match channel 9. 0: No interrupt on match channel 9 1: Interrupt requirements met on match channel 9.	R	0
4	CAP0IF	Interrupt flag for capture channel 0. 0: No interrupt on CAP0 1: Interrupt requirements met on CAP0.	R	0
3	MR3IF	Interrupt flag for match channel 3. 0: No interrupt on match channel 3 1: Interrupt requirements met on match channel 3.	R	0
2	MR2IF	Interrupt flag for match channel 2. 0: No interrupt on match channel 2 1: Interrupt requirements met on match channel 2.	R	0
1	MR1IF	Interrupt flag for match channel 1. 0: No interrupt on match channel 1 1: Interrupt requirements met on match channel 1.	R	0
0	MR0IF	Interrupt flag for match channel 0. 0: No interrupt on match channel 0 1: Interrupt requirements met on match channel 0.	R	0

10.8.29 T16Bn Timer Raw Interrupt Status register (CT16Bn_RIS) (n=3,4)

Address Offset: 0xA8

This register indicates the raw status for Timer/PWM interrupts. A Timer/PWM interrupt is sent to the interrupt controller if the corresponding bit in the CT16Bn_IE register is set.

Bit	Name	Description	Attribute	Reset
31:6	Reserved		R	0
5	MR9IF	Interrupt flag for match channel 9. 0: No interrupt on match channel 9. 1: Interrupt requirements met on match channel 9.	R	0
4	CAP0IF	Interrupt flag for capture channel 0. 0: No interrupt on CAP0. 1: Interrupt requirements met on CAP0.	R	0

3:2	Reserved		R	0
1	MR1IF	Interrupt flag for match channel 1. 0: No interrupt on match channel 1. 1: Interrupt requirements met on match channel 1.	R	0
0	MR0IF	Interrupt flag for match channel 0. 0: No interrupt on match channel 0. 1: Interrupt requirements met on match channel 0.	R	0

10.8.30 CT16Bn Timer Raw Interrupt Status register (CT16Bn_RIS) (n=1)

Address Offset: 0xA8

This register indicates the raw status for Timer/PWM interrupts. A Timer/PWM interrupt is sent to the interrupt controller if the corresponding bit in the CT16Bn_IE register is set.

Bit	Name	Description	Attribute	Reset
31:14	Reserved		R	0
13	CAP0IF	Interrupt flag for capture channel 0. 0: No interrupt on CAP0. 1: Interrupt requirements met on CAP0.	R	0
12	MR12IF	Interrupt flag for match channel 12. 0: No interrupt on match channel 12. 1: Interrupt requirements met on match channel 12.	R	0
11	MR11IF	Interrupt flag for match channel 11. 0: No interrupt on match channel 11. 1: Interrupt requirements met on match channel 11.	R	0
10	MR10IF	Interrupt flag for match channel 10. 0: No interrupt on match channel 10. 1: Interrupt requirements met on match channel 10.	R	0
9	MR9IF	Interrupt flag for match channel 9. 0: No interrupt on match channel 9. 1: Interrupt requirements met on match channel 9.	R	0
8	MR8IF	Interrupt flag for match channel 8. 0: No interrupt on match channel 8. 1: Interrupt requirements met on match channel 8.	R	0
7	MR7IF	Interrupt flag for match channel 7. 0: No interrupt on match channel 7. 1: Interrupt requirements met on match channel 7.	R	0
6	MR6IF	Interrupt flag for match channel 6. 0: No interrupt on match channel 6. 1: Interrupt requirements met on match channel 6.	R	0
5	MR5IF	Interrupt flag for match channel 5. 0: No interrupt on match channel 5. 1: Interrupt requirements met on match channel 5.	R	0
4	MR4IF	Interrupt flag for match channel 4. 0: No interrupt on match channel 4. 1: Interrupt requirements met on match channel 4.	R	0
3	MR3IF	Interrupt flag for match channel 3. 0: No interrupt on match channel 3. 1: Interrupt requirements met on match channel 3.	R	0
2	MR2IF	Interrupt flag for match channel 2. 0: No interrupt on match channel 2. 1: Interrupt requirements met on match channel 2.	R	0
1	MR1IF	Interrupt flag for match channel 1.	R	0

		0: No interrupt on match channel 1. 1: Interrupt requirements met on match channel 1.		
0	MR0IF	Interrupt flag for match channel 0. 0: No interrupt on match channel 0. 1: Interrupt requirements met on match channel 0.	R	0

10.8.31 CT16Bn Timer Interrupt Clear register (CT16Bn_IC) (n=0,2,5)

Address Offset: 0xAC

Bit	Name	Description	Attribute	Reset
31:6	Reserved		R	0
5	MR9IC	0: No effect 1: Clear MR9IF bit	W	0
4	CAP0IC	0: No effect 1: Clear CAP0IF bit	W	0
3	MR3IC	0: No effect 1: Clear MR3IF bit	W	0
2	MR2IC	0: No effect 1: Clear MR2IF bit	W	0
1	MR1IC	0: No effect 1: Clear MR1IF bit	W	0
0	MR0IC	0: No effect 1: Clear MR0IF bit	W	0

10.8.32 CT16Bn Timer Interrupt Clear register (CT16Bn_IC) (n=1)

Address Offset: 0xAC

Bit	Name	Description	Attribute	Reset
31:14	Reserved		R	0
13	CAP0IC	0: No effect 1: Clear CAP0IF bit	W	0
12	MR12IC	0: No effect 1: Clear MR12IF bit	W	0
11	MR11IC	0: No effect 1: Clear MR11IF bit	W	0
10	MR10IC	0: No effect 1: Clear MR10IF bit	W	0
9	MR9IC	0: No effect 1: Clear MR9IF bit	W	0
8	MR8IC	0: No effect 1: Clear MR8IF bit	W	0
7	MR7IC	0: No effect 1: Clear MR7IF bit	W	0
6	MR6IC	0: No effect 1: Clear MR6IF bit	W	0
5	MR5IC	0: No effect 1: Clear MR5IF bit	W	0
4	MR4IC	0: No effect 1: Clear MR4IF bit	W	0

3	MR3IC	0: No effect 1: Clear MR3IF bit	W	0
2	MR2IC	0: No effect 1: Clear MR2IF bit	W	0
1	MR1IC	0: No effect 1: Clear MR1IF bit	W	0
0	MR0IC	0: No effect 1: Clear MR0IF bit	W	0

10.8.33 CT16Bn Timer Interrupt Clear register (CT16Bn_IC) (n=3,4)

Address Offset: 0xAC

Bit	Name	Description	Attribute	Reset
31:6	Reserved		R	0
5	MR9IC	0: No effect 1: Clear MR9IF bit	W	0
4	CAP0IC	0: No effect 1: Clear CAP0IF bit	W	0
3:2	Reserved		R	0
1	MR1IC	0: No effect 1: Clear MR1IF bit	W	0
0	MR0IC	0: No effect 1: Clear MR0IF bit	W	0

10.8.34 CT16Bn PWMmN IO Control register (CT16Bn_PWMmNIOCTRL) (n=0)

Address Offset: 0xB0

Bit	Name	Description	Attribute	Reset
31:24	PWMKEY[7:0]	PWM register key. Read as 0. When writing to the register you must write 0x5A to PWMKEY, otherwise behaviour of writing to the register is ignored.	W	0
23:8	Reserved		R	0
7:6	PWM3NIOEN[1:0]	CT16Bn_PWM3N/GPIO selection bit 00: CT16Bn_PWM3N pin act as GPIO 01: CT16Bn_PWM3N pin outputs the inverse signal with dead-band of CT16Bn_PWM3, but same High signal during dead-band period. 10: CT16Bn_PWM3N pin outputs the inverse signal with dead-band of CT16Bn_PWM3, but same Low signal during dead-band period. 11: CT16Bn_PWM3N pin outputs the same signal with dead-band of CT16Bn_PWM3.	R/W	0
5:4	PWM2NIOEN[1:0]	CT16Bn_PWM2N/GPIO selection bit 00: CT16Bn_PWM2N pin act as GPIO 01: CT16Bn_PWM2N pin outputs the inverse signal with dead-band of CT16Bn_PWM2, but same High signal during dead-band period. 10: CT16Bn_PWM2N pin outputs the inverse signal with dead-band of CT16Bn_PWM2, but same Low signal during dead-band period. 11: CT16Bn_PWM2N pin outputs the same signal with dead-band of CT16Bn_PWM2.	R/W	0
3:2	PWM1NIOEN[1:0]	CT16Bn_PWM1N/GPIO selection bit 00: CT16Bn_PWM1N pin act as GPIO 01: CT16Bn_PWM1N pin outputs the inverse signal with dead-band of	R/W	0

		CT16Bn_PWM1, but same High signal during dead-band period. 10: CT16Bn_PWM1N pin outputs the inverse signal with dead-band of CT16Bn_PWM1, but same Low signal during dead-band period. 11: CT16Bn_PWM1N pin outputs the same signal with dead-band of CT16Bn_PWM1.		
1:0	PWM0NIOEN[1:0]	CT16Bn_PWM0N/GPIO selection bit 00: CT16Bn_PWM0N pin act as GPIO 01: CT16Bn_PWM0N pin outputs the inverse signal with dead-band of CT16Bn_PWM0, but same High signal during dead-band period. 10: CT16Bn_PWM0N pin outputs the inverse signal with dead-band of CT16Bn_PWM0, but same Low signal during dead-band period. 11: CT16Bn_PWM0N pin outputs the same signal with dead-band of CT16Bn_PWM0.	R/W	0

10.8.35 CT16Bn PWMmN IO Control register (CT16Bn_PWMmNIOCTRL) (n=3,4)

Address Offset: 0xB0

Bit	Name	Description	Attribute	Reset
31:24	PWMKEY[7:0]	PWM register key. Read as 0. When writing to the register you must write 0x5A to PWMKEY, otherwise behaviour of writing to the register is ignored.	W	0
23:4	Reserved		R	0
3:2	PWM1NIOEN[1:0]	CT16Bn_PWM1N/GPIO selection bit 00: CT16Bn_PWM1N pin act as GPIO 01: CT16Bn_PWM1N pin outputs the inverse signal with dead-band of CT16Bn_PWM1, but same High signal during dead-band period. 10: CT16Bn_PWM1N pin outputs the inverse signal with dead-band of CT16Bn_PWM1, but same Low signal during dead-band period. 11: CT16Bn_PWM1N pin outputs the same signal with dead-band of CT16Bn_PWM1.	R/W	0
1:0	PWM0NIOEN[1:0]	CT16Bn_PWM0N/GPIO selection bit 00: CT16Bn_PWM0N pin act as GPIO 01: CT16Bn_PWM0N pin outputs the inverse signal with dead-band of CT16Bn_PWM0, but same High signal during dead-band period. 10: CT16Bn_PWM0N pin outputs the inverse signal with dead-band of CT16Bn_PWM0, but same Low signal during dead-band period. 11: CT16Bn_PWM0N pin outputs the same signal with dead-band of CT16Bn_PWM0.	R/W	0

10.8.36 CT16Bn PWMmN Dead-band Period register (CT16Bn_PWMmNDB) (n=0)

Address Offset: 0xB4, 0xB8, 0xBC, 0xC0

The PWMmNDB register is used to configure the dead-band period of the PWMmN outputs, and is only usable when PWMmNIOEN[1:0]≠00b.

Bit	Name	Description	Attribute	Reset
31:24	PWMKEY[7:0]	PWM register key. Read as 0. When writing to the register you must write 0x5A to PWMKEY, otherwise behaviour of writing to the register is ignored.	W	0
23:10	Reserved		R	0
9:0	DB[9:0]	Count of PWMmN output dead-band period time PWMmN output dead-band period time = DB * CT16B_PCLK * (PR+1) cycle	R/W	0

10.8.37 CT16Bn PWMmN Dead-band Period register (CT16Bn_PWMmNDB) (n=3,4)

Address Offset: 0xB4, 0xB8

The PWMmNDB register is used to configure the dead-band period of the PWMmN outputs, and is only usable when PWMmNIOEN[1:0]≠00b.

Bit	Name	Description	Attribute	Reset
31:24	PWMKEY[7:0]	PWM register key. Read as 0. When writing to the register you must write 0x5A to PWMKEY, otherwise behaviour of writing to the register is ignored.	W	0
23:10	Reserved		R	0
9:0	DB[9:0]	Count of PWMmN output dead-band period time PWMmN output dead-band period time = DB * CT16B_PCLK * (PR+1) cycle	R/W	0

11 WATCHDOG TIMER (WDT)

11.1 OVERVIEW

The purpose of the Watchdog is to reset the MCU within a reasonable amount of time if it enters an erroneous state. When enabled, the Watchdog will generate a system reset or interrupt if the user program fails to "feed" (or reload) the Watchdog within a predetermined amount of time.

The Watchdog consists of a divide by 128 fixed pre-scaler and an 8-bit counter. The clock is fed to the timer via a pre-scaler. The timer decrements when clocked. The minimum value from which the counter decrements is 0x01. Hence the minimum Watchdog interval is ($T_{WDT\_PCLK} \times 128 \times 1$) and the maximum Watchdog interval is ($T_{WDT\_PCLK} \times 128 \times 256$).

The Watchdog should be used in the following manner:

1. Set the prescale value for the watchdog clock with WDTPRE bits in APB Clock Prescale register 1 (SYS1_APBCP1) register.
2. Set the Watchdog timer constant reload value in WDT_TC register.
3. Enable the Watchdog and setup the Watchdog timer operating mode in WDT_CFG register.
4. The Watchdog should be fed again by writing 0x55AA to WDT_FEED register before the Watchdog counter underflows to prevent reset or interrupt.

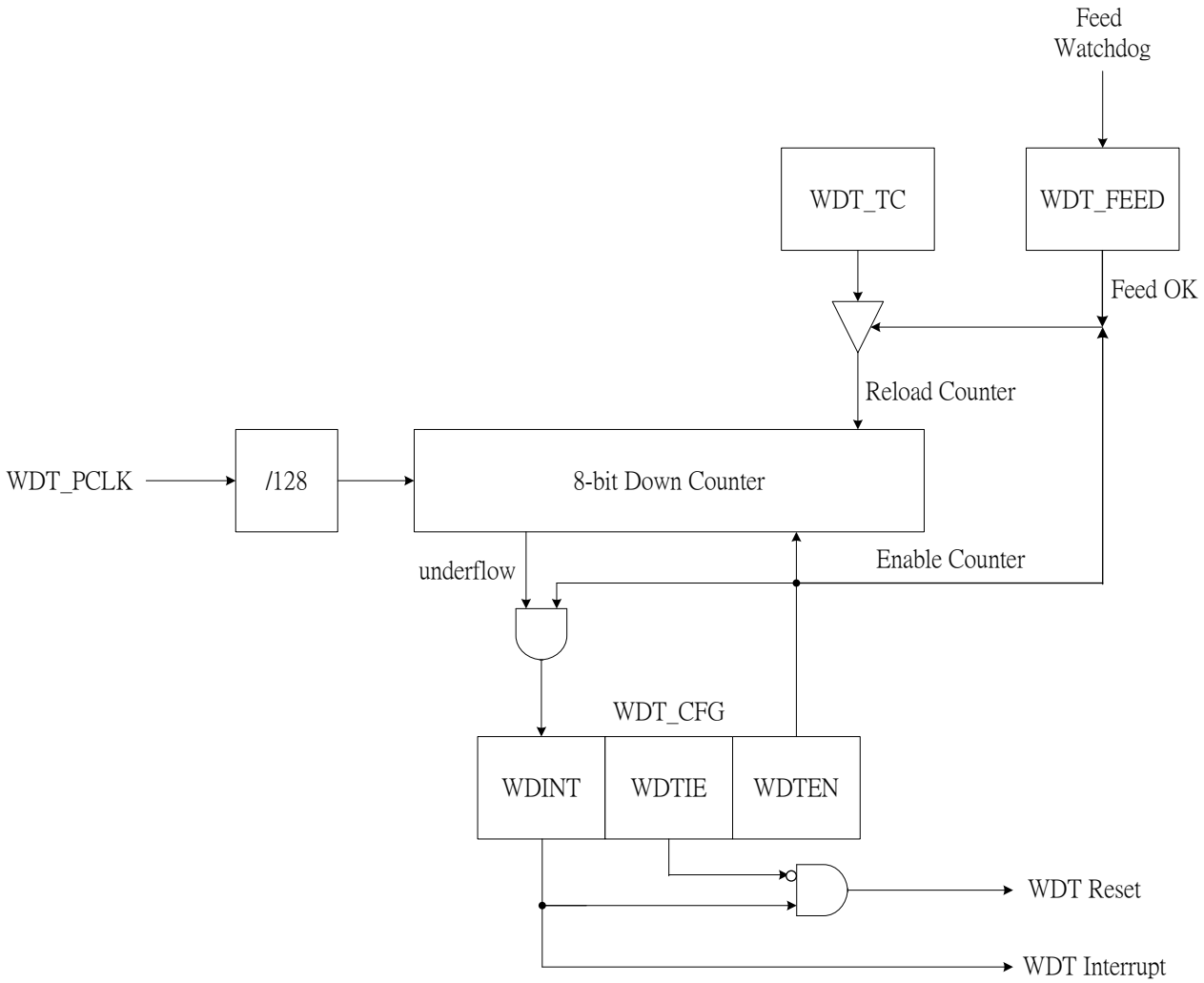
When the watchdog is started by setting the WDTEN in WDT_CFG register, the time constant value is loaded in the watchdog counter and the counter starts counting down. When the Watchdog is in the reset mode and the counter underflows, the CPU will be reset, loading the stack pointer and program counter from the vector table as in the case of external reset. Whenever the value 0x55AA is written in WDT_FEED register, the WDT_TC value is reloaded in the watchdog counter and the watchdog reset or interrupt is prevented.

The watchdog timer block uses two clocks: HCLK and WDT_PCLK. HCLK is used for the AHB accesses to the watchdog registers and is derived from the system clock. The WDT_PCLK is used for the watchdog timer counting.
ILRC is the clock source for WDT_PCLK.

The clock to the watchdog register block can be disabled in AHB Clock Enable register (SYS1_AHBCLKEN) register for power savings.

Watchdog reset or interrupt will occur any time the watchdog is running and has an operating clock source.

11.2 BLOCK DIAGRAM



11.3 WDT REGISTERS

Base Address: 0x4001 0000

11.3.1 Watchdog Configuration register (WDT_CFG)

Address Offset: 0x00

The WDT_CFG register controls the operation of the Watchdog through the combination of WDTEN and WDTIE bits. This register indicates the raw status for Watchdog Timer interrupts. A WDT interrupt is sent to the interrupt controller if both the WDTINT bit and the WDTIE bit are set.

Bit	Name	Description	Attribute	Reset
31:16	WDKEY	Watchdog register key. Read as 0. When writing to the register you must write 0x5AFA to WDKEY, otherwise behavior of writing to the register is ignored.	W	0
15:3	Reserved		R	0
2	WDTINT	Watchdog interrupt flag 0: Read→Watchdog does not cause an interrupt. Write→ Clear this flag. SW shall feed Watchdog before clearing. 1: Watchdog timeout and causes an interrupt (Only when WDTIE =1).	R/W	0
1	WDTIE	Watchdog interrupt enable 0: Watchdog timeout will cause a chip reset. (Watchdog reset mode) Watchdog counter underflow will reset the MCU, and will clear the WDTINT flag. 1: Watchdog timeout will cause an interrupt. (Watchdog interrupt mode)	R/W	0
0	WDTEN	Watchdog enable 0: Disable 1: Enable. When enable the watchdog, the WDT_TC value is loaded in the watchdog counter.	R/W	0

11.3.2 Watchdog Timer Constant register (WDT_TC)

Address Offset: 0x08

The WDT_TC register determines the time-out value. Every time a feed sequence occurs the WDT_TC content is reloaded in to the Watchdog timer. It's an 8-bit counter. Thus the time-out interval is T_{WDT_PCLK} × 128 x 1 ~ T_{WDT_PCLK} × 128 x 256.

Bit	Name	Description	Attribute	Reset
31:16	WDKEY	Watchdog register key. Read as 0. When writing to the register you must write 0x5AFA to WDKEY, otherwise behavior of writing to the register is ignored.	W	0
15:8	Reserved		R	0
7:0	TC[7:0]	Watchdog timer constant reload value = TC[7:0]+1 0000 0000 : Timer constant = 1 0000 0001 : Timer constant = 2 ……. ……. 1111 1110 : Timer constant = 255 1111 1111 : Timer constant = 256	R/W	0xFF

11.3.3 Watchdog Feed register (WDT_FEED)

Address Offset: 0x0C

Bit	Name	Description	Attribute	Reset
31:16	WDKEY	Watchdog register key. Read as 0. When writing to the register you must write 0x5AFA to WDKEY, otherwise behavior of writing to the register is ignored.	W	0
15:0	FV[15:0]	Feed value (Read as 0x0) 0x55AA: The watchdog is fed, and the WDT_TC value is reloaded in the watchdog counter.	W	0

12 REAL-TIME CLOCK (RTC)

12.1 OVERVIEW

The RTC is an independent timer. The RTC provides a set of continuously running counters which can be used to provide a clock-calendar function with suitable software.
The counter values can be written to set the current time/date of the system.

12.2 FEATURES

- Programmable prescale value: division factor up to 2^{20}
- 32-bit programmable counter for long-term measurement
- The RTC clock source could be any of the following:
  - ELS X'TAL
  - ILRC
- Reset sources of the RTC Core (Prescale value, Counter and Divider):
  - "Cold" boot
- Three dedicated enabled interrupt lines:
  - Seconds interrupt: generating a periodic interrupt signal with a programmable period length (up to 1 second).

12.3 FUNCTIONAL DESCRIPTION

12.3.1 INTRODUCTION

RTC core includes a 20-bit preload value (RTC SECCNTV). Every TR_CLK period, the RTC generates an interrupt (Second Interrupt) if it is enabled in RTC_IE register.

12.3.2 RESET RTC REGISTERS

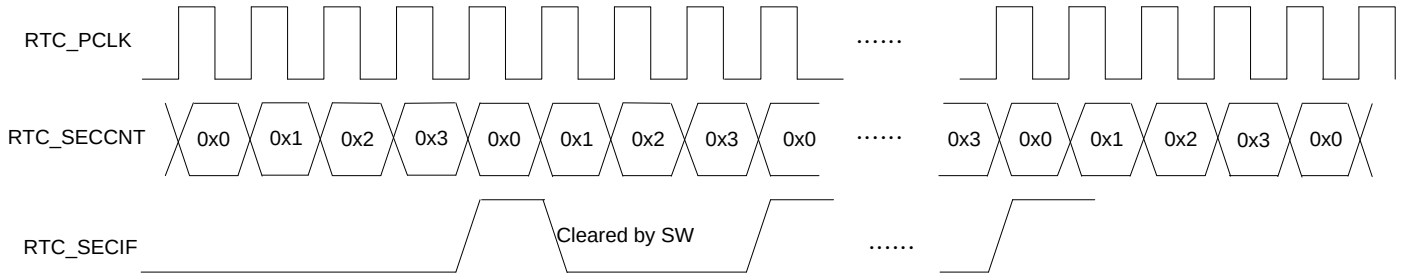
The RTC_SECCNTV and RTC_SECCNT registers are reset by "cold" boot.

12.3.3 RTC FLAG ASSERTION

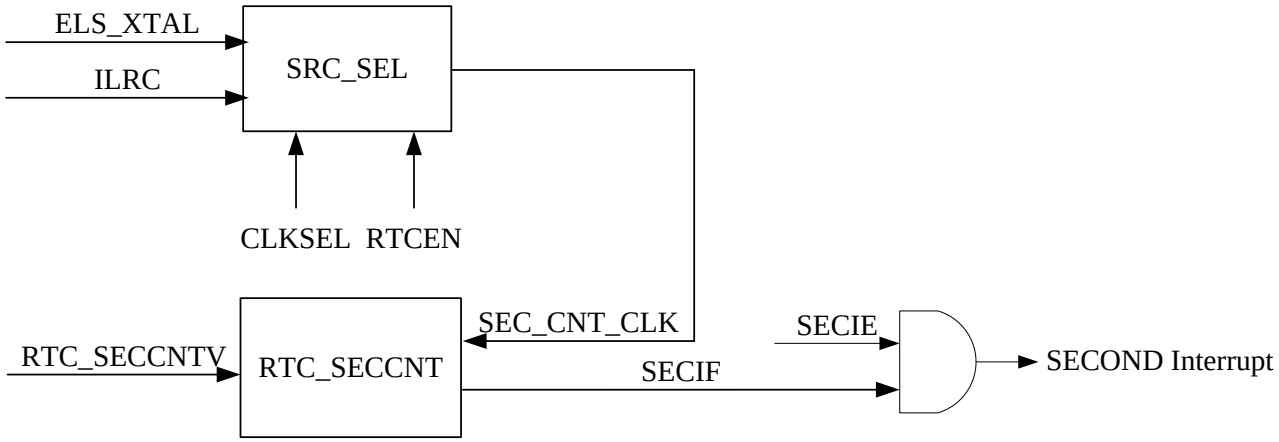
The RTC Second interrupt flag (SECIF) is asserted on each RTC Core clock cycle before the update of the RTC Counter.

12.3.4 RTC OPERATION

The following figure shows the RTC waveform when it is configured with RTC_SECCNTV=3.



12.4 BLOCK DIAGRAM



12.5 RTC REGISTERS

Base Address: 0x4001 2000

12.5.1 RTC Control register (RTC_CTRL)

Address offset: 0x00

✸ ***Note: RTCEN bit shall be set at last!***

Bit	Name	Description	Attribute	Reset
31:1	Reserved		R	0
0	RTCEN	RTC enable bit 0: Disable 1: Enable. Reset SEC_CNT.	R/W	0

12.5.2 RTC Clock Source Select register (RTC_CLKS)

Address offset: 0x04

✸ ***Note: SW shall disable RTC (RTCEN=0) when changing the value of this register.***

Bit	Name	Description	Attribute	Reset
31:1	Reserved		R	0
0	CLKSEL	RTC clock source selection. HW will reset SEC_CNT and ALM_CNT when changing the value. 0: ILRC 1: ELS X'TAL	R/W	0

12.5.3 RTC Interrupt Enable register (RTC_IE)

Address offset: 0x08

Bit	Name	Description	Attribute	Reset
31:1	Reserved		R	0
0	SECIE	Second interrupt enable 0: Disable 1: Enable	R/W	0

12.5.4 RTC Raw Interrupt Status register (RTC_RIS)

Address offset: 0x0C

Bit	Name	Description	Attribute	Reset
31:1	Reserved		R	0
0	SECIF	Second interrupt flag This bit is set by HW when SEC_CNT=SEC_CNTV. An interrupt is generated if SECIE=1. 0: Second flag condition not met. 1: Second flag condition met.	R	0

12.5.5 RTC Interrupt Clear register (RTC_IC)

Address offset: 0x10

Bit	Name	Description	Attribute	Reset
31:1	Reserved		R	0
0	SECIC	0: No effect 1: Clear SECIF bit	W	0

12.5.6 RTC Second Counter Reload Value register (RTC_SECCNTV)

Address offset: 0x14

Bit	Name	Description	Attribute	Reset
31:20	Reserved		R	0
19:0	SECCNTV[19:0]	RTC second counter reload value. Update this register will reset RTC_SECCNT register. The zero value is not recommended, and will be replaced with default value (0x8000) by HW.	R/W	0x8000

12.5.7 RTC Second Count register (RTC_SECCNT)

Address offset: 0x18

The RTC core has one 32-bit programmable counter, and this register keeps the current counting value of this counter.

Bit	Name	Description	Attribute	Reset
31:0	SECCNT[31:0]	RTC second counter The current value of the RTC counter.	R	0

13 SPI

13.1 OVERVIEW

The SPI is a Synchronous Serial Port controller capable of operation on a SPI bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of 4 to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice it is often the case that only one of these data flows carries meaningful data.

13.2 FEATURES

- Compatible with Motorola SPI bus.
- Synchronous Serial Communication.
- Supports master or slave operation.
- 8-frame FIFO for both transmitter and receiver.
- 4-bit to 16-bit frame.
- Maximum SPI speed of 36 Mbps (master) or 12 Mbps (slave)
- Data transfer format is from MSB or LSB controlled by register.
- The start phase of data sampling location selection is 1st-phase or 2nd-phase controlled register.

13.3 PIN DESCRIPTION

Pin Name	Type	Description	GPIO Configuration
SCKn	O	SPI Serial clock (Master)	
	I	SPI Serial clock (Slave)	Depends on GPIOn_CFG
SELn	O	SPI Slave Select (Master)	
	I	SPI Slave Select (Slave)	Depends on GPIOn_CFG
MISOn	I	Master In Slave Out (Master)	Depends on GPIOn_CFG
	O	Master In Slave Out (Slave)	
MOSIn	O	Master Out Slave In (Master)	
	I	Master Out Slave In (Slave)	Depends on GPIOn_CFG

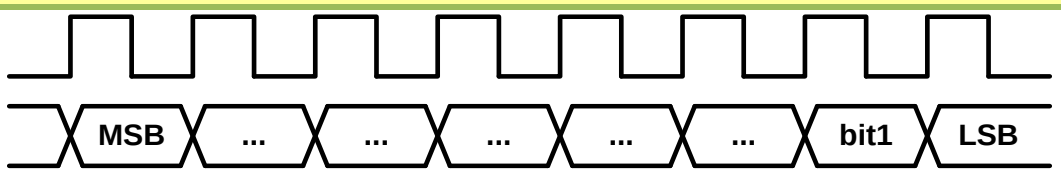
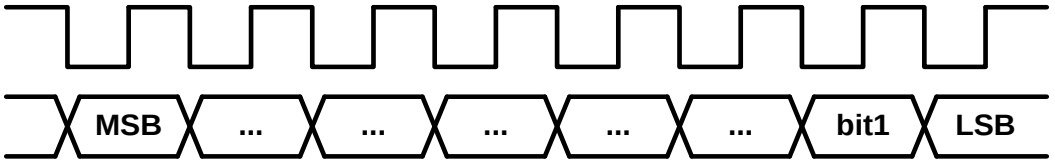
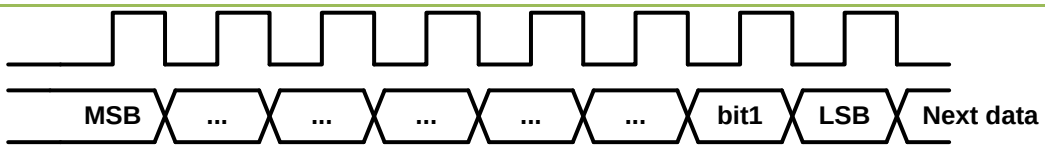
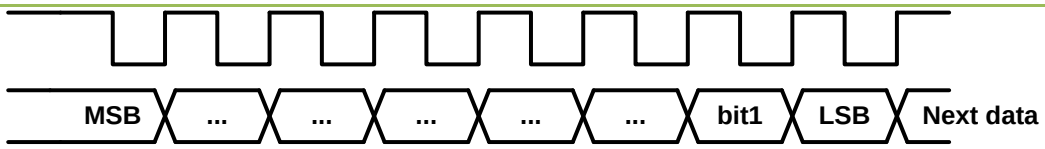
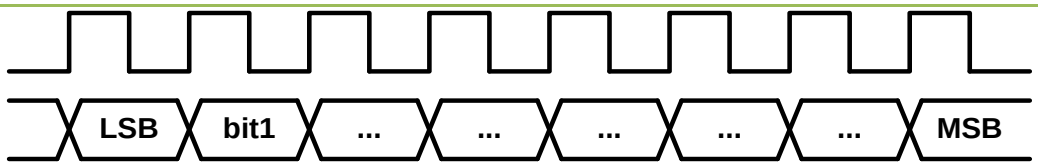
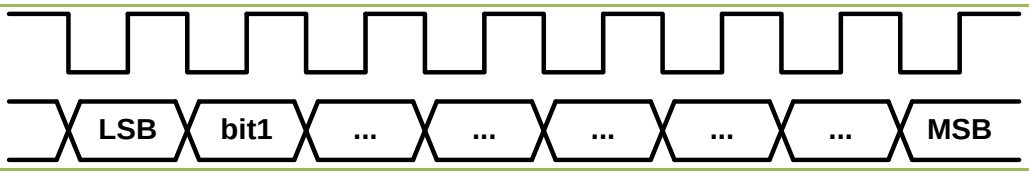
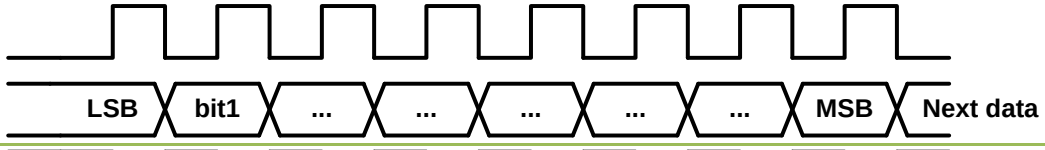
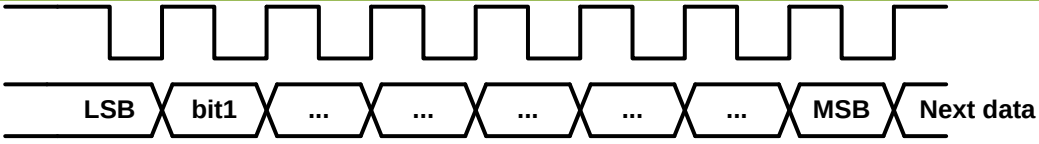
13.4 INTERFACE DESCRIPTION

13.4.1 SPI

The SPI interface is a 4-wire interface where the SEL signal behaves as a slave select. The main feature of the SPI format is that the inactive state and phase of the SCK signal are programmable through the CPOL and CPHA bits in SPIn_CTRL1 register.

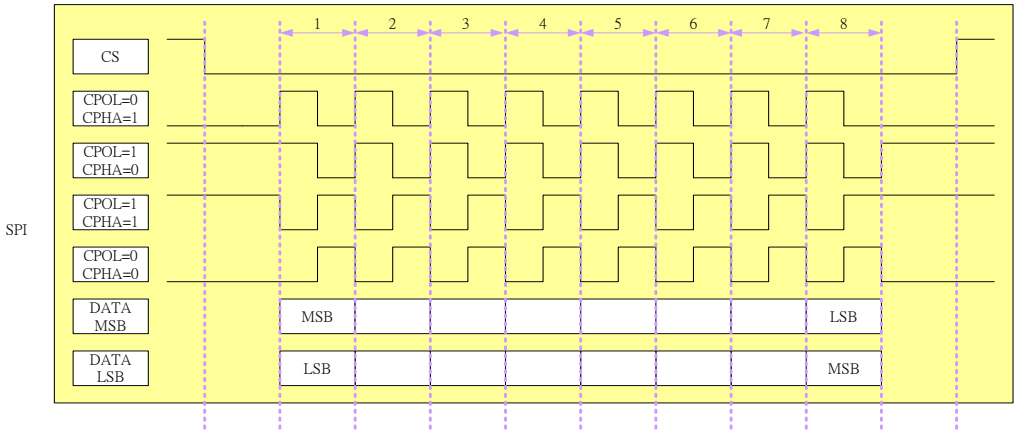
When the “CPOL” clock polarity control bit is LOW, it produces a steady state low value on the SCK pin. If the CPOL clock polarity control bit is HIGH, a steady state high value is placed on the CLK pin when data is not being transferred. The “CPHA” clock phase bit controls the phase of the clock on which data is sampled. When CPHA=1, the SCK first edge is for data transition, and receive and transmit data is at SCK 2nd edge. When CPHA=0, the 1st bit is fixed already, and the SCK first edge is to receive and transmit data.

The SPI data transfer timing as following figure:

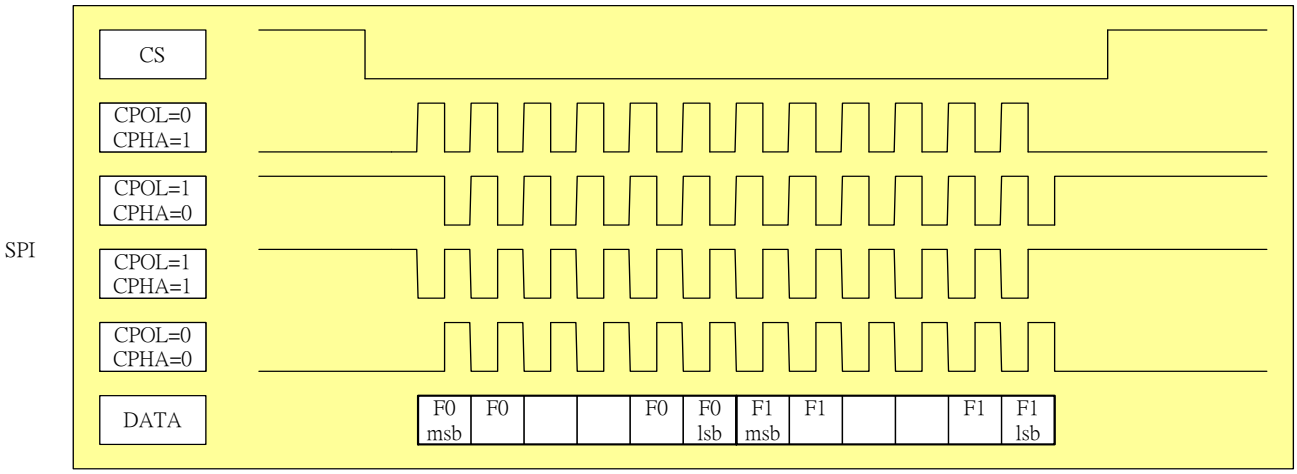
MLSB	CPOL	CPHA	SCK Idle Status	Diagrams
0	0	1	Low	
0	1	1	High	
0	0	0	Low	
0	1	0	High	
1	0	1	Low	
1	1	1	High	
1	0	0	Low	
1	1	0	High	

13.4.2 COMMUNICATION FLOW

13.4.2.1 SINGLE-FRAME



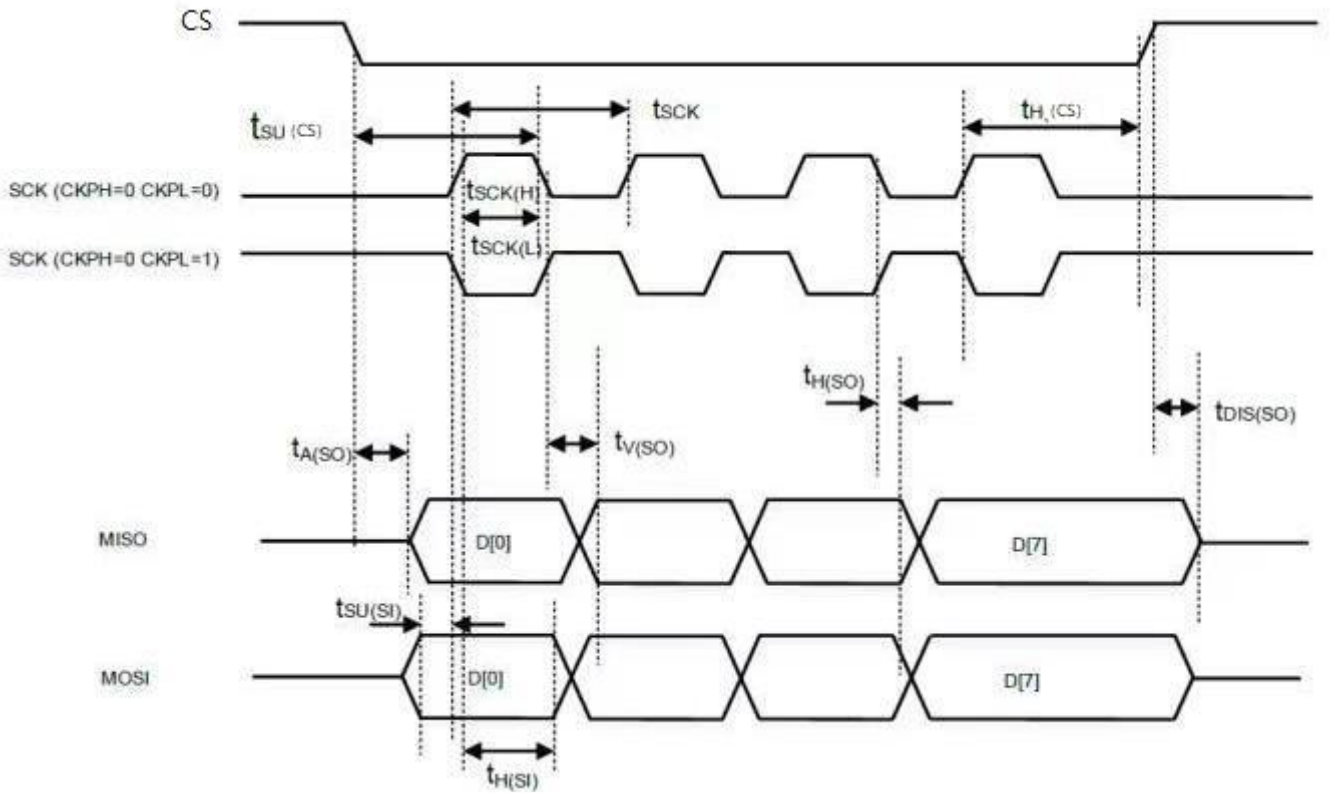
13.4.2.2 MULTI-FRAME



13.5 AUTO-SEL

The Auto-SEL function is disabled (SELDIS = 1) by default, HW does NOT control SELn pin at all, and SELn pin is GPIO. If Auto-SEL function is enabled (SELDIS = 0), SPI HW controls the SELn activity, and SELn is assigned by PFPA_SPI register.

13.6 TIMING CHARACTERISTICS



13.6.1 MASTER MODE

Symbol	Parameter	Min	Typ	Max	Unit
t_{sck}	SCK out period	33			ns
$t_{sck}(H)$	SCK out high pulse	t_{sck}*0.4			ns
$t_{sck}(L)$	SCK out low pulse	t_{sck}*0.4			ns
$t_{SU}(CS)$	CS out setup time	t_{sck}*2			ns
$t_H(CS)$	CS out hold time	t_{sck}*1.5			ns
$t_{SU}(MISO)$	Data in setup time	t_{sck}*0.4			ns
$t_H(MISO)$	Data in hold time	t_{sck}*0.4			ns
$t_{SU}(MOSI)$	Data out setup time	t_{sck}*0.4			ns
$t_H(MOSI)$	Data out hold time	t_{sck}*0.4			ns

13.6.2 SLAVE MODE

Symbol	Parameter	Min	Typ	Max	Unit
t_{sck}	SCK in period	33			ns
$t_{sck}(H)$	SCK in high pulse	t_{sck}*0.4			ns
$t_{sck}(L)$	SCK in low pulse	t_{sck}*0.4			ns
$t_{SU}(CS)$	CS in setup time	t_{sck}*1.5			ns
$t_H(CS)$	CS in hold time	t_{sck}			ns
$t_{SU}(MISO)$	Data out setup time	t_{sck}*0.4			ns
$t_H(MISO)$	Data out hold time	t_{sck}*0.4			ns
$t_{SU}(MOSI)$	Data in setup time	t_{sck}*0.4			ns
$t_H(MOSI)$	Data in hold time	t_{sck}*0.4			ns

13.7 SPI REGISTERS

Base Address: 0x4001 C000 (SPI0)
0x4005 8000 (SPI1)

13.7.1 SPI n Control register 0 (SPIn_CTRL0) (n=0,1)

Address Offset:0x00

✸ ***Note:***
1. Must reset SPI FSM with FRESET[1:0] after changing any configuration of SPI when SPIEN = 1.
2. HW will switch I/O configurations refer to FORMAT bit directly when SPIEN = 1.

Bit	Name	Description	Attribute	Reset
31:19	Reserved		R	0
18	SELDIS	Auto-SEL disable bit. 0: Enable Auto-SEL flow control. 1: Disable Auto-SEL flow control.	R/W	1
17:15	RXFIFOTH[2:0]	RX FIFO Threshold level 000: RX FIFO threshold level = 0 001: RX FIFO threshold level = 1 … … 111: RX FIFO threshold level = 7	R/W	000b
14:12	TXFIFOTH[2:0]	TX FIFO Threshold level 000: TX FIFO threshold level = 0 001: TX FIFO threshold level = 1 … … 111: TX FIFO threshold level = 7	R/W	000b
11:8	DL[3:0]	Data length = DL[3:0] + 1 0000~0001: Reversed 0010: data length = 3 … … 1110: data length = 15 1111: data length = 16	R/W	1111b
7:6	FRESET[1:0]	SPI FSM and FIFO Reset bit 00: No effect 01: Reserved 10: Reserved 11: Reset finite state machine and FIFO. (BUF_BUSY = 0, data in shift BUF is cleared, TX_EMPTY = 1, TX_FULL = 0, RX_EMPTY = 1, RX_FULL = 0, and data in FIFO is cleared). This bit will be cleared by HW automatically.	W	0
5	Reserved		R	0
4	FORMAT	Interface format. 0: SPI 1: Reserved	R/W	0
3	MS	Master/Slave selection bit 0: Act as Master. 1: Act as Slave.	R/W	0
2	SDODIS	Slave data output disable bit (ONLY used in slave mode) 0: Enable slave data output. 1: Disable slave data output. (MISO=0)	R/W	0
1	LOOPBACK	Loop back mode enable 0: Disable 1: Data input from data output	R/W	0
0	SPIEN	SPI enable bit 0: Disable 1: Enable.	R/W	0

13.7.2 SPI n Control register 1 (SPIn_CTRL1) (n=0,1)

Address Offset: 0x04

Bit	Name	Description	Attribute	Reset
31:3	Reserved		R	0
2	CPHA	Clock phase for edge sampling. 0: Data changes at clock falling edge, latches at clock rising edge when CPOL = 0; Data changes at clock rising edge, latches at clock falling edge when CPOL = 1. 1: Data changes at clock rising edge, latches at clock falling edge when CPOL = 0; Data changes at clock falling edge, latches at clock rising edge when CPOL = 1.	R/W	0
1	CPOL	Clock polarity selection bit 0: SCK idles at Low level. 1: SCK idles at High level.	R/W	0
0	MLSB	MSB/LSB selection bit 0: MSB transmit first. 1: LSB transmit first.	R/W	0

13.7.3 SPI n Clock Divider register (SPIn_CLKDIV) (n=0,1)

Address Offset: 0x08

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7:0	DIV[7:0]	SPIn clock divider 0: SCK = SPIn_PCLK / 2 1: SCK = SPIn_PCLK / 4 2: SCK = SPIn_PCLK / 6 X: SCK = SPIn_PCLK / (2X+2)	R/W	0

13.7.4 SPI n Status register (SPIn_STAT) (n=0,1)

Address Offset: 0x0C

Bit	Name	Description	Attribute	Reset
31:7	Reserved		R	0
6	RXFIFOTHF	RX FIFO threshold flag 0: Data in RX FIFO ≤ RXFIFOTH 1: Data in RX FIFO > RXFIFOTH	R	0
5	TXFIFOTHF	TX FIFO threshold flag 0: Data in TX FIFO > TXFIFOTH 1: Data in TX FIFO ≤ TXFIFOTH	R	1
4	BUSY	Busy flag. 0: SPI controller is idle. 1: SPI controller is transferring.	R	0
3	RX_FULL	RX FIFO full flag. 0: RX FIFO is NOT full. 1: RX FIFO is full.	R	0
2	RX_EMPTY	RX FIFO empty flag 0: RX FIFO is NOT empty. 1: RX FIFO is empty.	R	1
1	TX_FULL	TX FIFO full flag. 0: TX FIFO is NOT full. 1: TX FIFO is full.	R	0
0	TX_EMPTY	TX FIFO empty flag 0: TX FIFO is NOT empty. In Master mode, the transmitter will begin to transmit automatically. 1: TX FIFO is empty.	R	1

13.7.5 SPI n Interrupt Enable register (SPIn_IE) (n=0,1)

Address Offset: 0x10

This register controls whether each of the four possible interrupt conditions in the SPI controller is enabled.

Bit	Name	Description	Attribute	Reset
31:6	Reserved		R	0
5	DMATCIE	DMA transfer complete interrupt enable bit (SPI0 only) 0: Disable 1: Enable	R/W	0
4	DMAHTIE	DMA half transfer interrupt enable bit (SPI0 only) 0: Disable 1: Enable	R/W	0
3	TXFIFOTHIE	TX FIFO threshold interrupt enable 0: Disable 1: Enable	R/W	0
2	RXFIFOTHIE	RX FIFO threshold interrupt enable 0: Disable 1: Enable	R/W	0
1	RXTOIE	RX time-out interrupt enable 0: Disable 1: Enable	R/W	0
0	RXOVFIE	RX Overflow interrupt enable 0: Disable 1: Enable	R/W	0

13.7.6 SPI n Raw Interrupt Status register (SPIn_RIS) (n=0,1)

Address Offset: 0x14

This register contains the status for each interrupt condition, regardless of whether or not the interrupt is enabled in SPIn_IE register.

This register indicates the status for SPI control raw interrupts. An SPI interrupt is sent to the interrupt controller if the corresponding bit in the SPIn_IE register is set.

Bit	Name	Description	Attribute	Reset
31:6	Reserved		R	0
5	DMATCIF	DMA transfer complete flag (SPI0 only) 0: No transfer completion 1: A transfer complete event occurs	R	0
4	DMAHTIF	DMA half transfer flag (SPI0 only) 0: No half transfer event 1: A half transfer event occurs	R	0
3	TXFIFOTHIF	TX FIFO threshold interrupt flag 0: No TX FIFO threshold interrupt 1: TX FIFO threshold triggered.	R	0
2	RXFIFOTHIF	RX FIFO threshold interrupt flag 0: No RX FIFO threshold interrupt 1: RX FIFO threshold triggered.	R	0
1	RXTOIF	RX time-out interrupt flag RXTO occurs when the RX FIFO is not empty, and has not been read for a time-out period (32*SPIn_PCLK). The time-out period is the same for master and slave modes. 0: RXTO doesn't occur. 1: RXTO occurs.	R	0
0	RXOVFIF	RX Overflow interrupt flag RXOVF occurs when the RX FIFO is full and another frame is completely received. The ARM spec implies that the preceding frame data is overwritten by the new frame data when this occurs. 0: RXOVF doesn't occur. 1: RXOVF occurs.	R	0

13.7.7 SPI n Interrupt Clear register (SPIn_IC) (n=0,1)

Address Offset: 0x18

Bit	Name	Description	Attribute	Reset
31:6	Reserved		R	0
5	DMATCIC	Select the DMATCIF flag to be cleared (SPI0 only) 0: No effect 1: Clear DMATCIF flag	W	0
4	DMAHTIC	Select the DMAHTIF flag to be cleared (SPI0 only) 0: No effect 1: Clear DMAHTIF flag	W	0
3	TXFIFOTHIC	0: No effect 1: Clear TXFIFOTHIF bit	W	0
2	RXFIFOTHIC	0: No effect 1: Clear RXFIFOTHIF bit	W	0
1	RXTOIC	0: No effect 1: Clear RXTOIF bit.	W	0
0	RXOVFIC	0: No effect 1: Clear RXOVFIF bit.	W	0

13.7.8 SPI n Data register (SPIn_DATA) (n=0,1)

Address Offset: 0x1C

Bit	Name	Description	Attribute	Reset
31:16	Reserved		R	0
15:0	DATA[15:0]	Write SW can write data to be sent in a future frame to this register when TX_FULL = 0 in SPIn_STAT register (TX FIFO is not full). If the TX FIFO was previously empty and the SPI controller is not busy on the bus, transmission of the data will begin immediately. Otherwise the data written to this register will be sent as soon as all previous data has been sent (and received). Read SW can read data from this register when RX_EMPTY=0 in SPIn_STAT register (Rx FIFO is not empty). When SW reads this register, the SPI controller returns data from the least recent frame in the RX FIFO. If the data length is less than 16 bit, the data is right-justified in this field with higher order bits filled with 0s.	R/W	0

13.7.9 SPI n Data Fetch register (SPIn_DF) (n=0,1)

Address Offset: 0x20

Bit	Name	Description	Attribute	Reset
31:1	Reserved		R	0
0	DF	SPI data fetch control bit 0: Disable 1: Enable when SCKn frequency > 6MHz	R/W	0

13.7.10 SPI n DMA Control register (SPIn_DMACTRL) (n=0)

Address Offset: 0x24

SPIn DMA (Direct memory access) is only used in order to provide high-speed data transfer between external SPI-flash and TFT-LCD. Data can be moved from SPI FIFOs to TFT-LCD by DMA without any CPU actions. This keeps CPU resources free for other operations. The data length of SPIn DMA is 8 bits. Please refer to Section 18.6 8080 MODE DMA-CONTROLLED TFT-LCD for more detail.

Bit	Name	Description	Attribute	Reset
31:2	Reserved		R	0
1	DIR	SPI data transfer direction 0: SPI1_DATA(RX) to SPI0_DATA(TX), when DMATCIE and DMAHTIE enable, and trigger SPI0 interrupt 1: SPI0_DATA(RX) to SPI1_DATA(TX) , when DMATCIE and DMAHTIE enable, and trigger SPI1 interrupt	R/W	0
0	DMAEN	SPI to SPI DMA enable bit 0: Disable (cleared by HW) 1: Enable	R/W	0

13.7.11 SPI n DMA Number of Data Transfer register (SPIn_DMACNT) (n=0)

Address Offset: 0x28

Bit	Name	Description	Attribute	Reset
31:28	Reserved		R	0
27:0	CNT[27:0]	Number of data to DMA RX count transfer (0 up 0xFFFFFFF) This register can only be written when the DMA is disabled. Once the DMA is enabled, this register is read-only, indicating the remaining bytes to be transmitted. Once the transfer is completed(CURCNT=CNT), and trigger DMATC interrupt.	R/W	0

13.7.12 SPI n DMA Number of Half Data Transfer register (SPIn_DMAHTCNT) (n=0)

Address Offset: 0x2C

Bit	Name	Description	Attribute	Reset
31:28	Reserved		R	0
27:0	HTCNT[27:0]	Number of data to DMA RX half count transfer (0 up 0xFFFFFFF) This register can only be written when the DMA is disabled. Once the DMA is enabled, this register is read-only, indicating the remaining bytes to be transmitted. Once the half transfer is completed(CURCNT=HTCNT), and trigger DMATC interrupt.	R/W	0xFFFFFFF

13.7.13 SPI n DMA Current Transfer Data Counter register (SPIn_CURCNT) (n=0)

Address Offset: 0x30

Bit	Name	Description	Attribute	Reset
31:28	Reserved		R	0
27:0	CURCNT[27:0]	This field indicates DMA current transfer data counter pointer. Count from 0 to DMACNT.	R	0

14 I2C

14.1 OVERVIEW

The I2C bus is bidirectional for inter-IC control using only two wires: Serial Clock Line (SCL) and Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I2C is a multi-master bus and can be controlled by more than one bus master connected to it. It is also SMBus 2.0 compatible.

The I2C interface is byte oriented and has four operating modes:

- Master transmitter mode
- Master receiver mode
- Slave transmitter mode
- Slave receiver mode

14.2 FEATURES

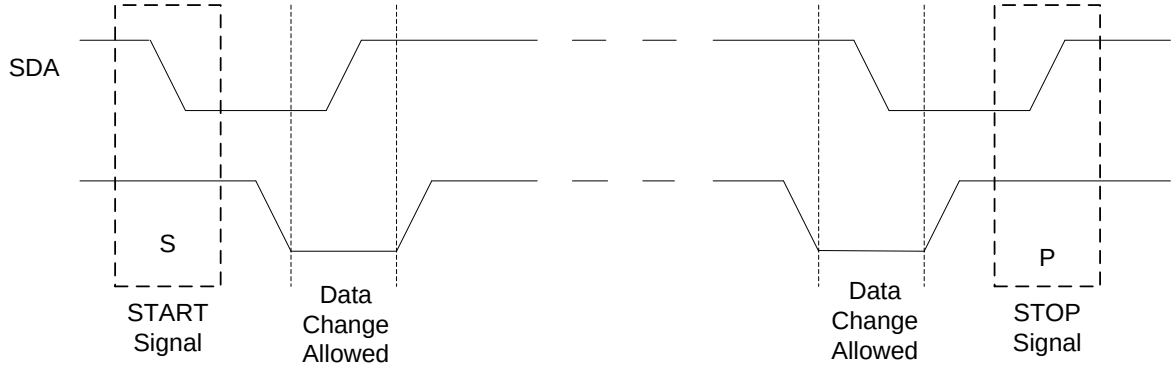
The I2C interface complies with the entire I2C specification, supporting the ability to turn power off to the ARM Cortex-M0 without interfering with other devices on the same I2C-bus.

- Standard I2C-compliant bus interfaces may be configured as Master or Slave.
- I2C Master features:
  - Clock generation
  - Start and Stop generation
- I2C Slave features:
  - Programmable I2C Address detection
  - Optional recognition of up to four distinct slave addresses
  - Stop bit detection
- Supports different communication speeds:
  - Standard Speed (up to 100KHz)
  - Fast Speed (up to 400 KHz)
- Arbitration is handled between simultaneously transmitting masters without corruption of serial data on the bus.
- Programmable clock allows adjustment of I2C transfer rates.
- Data transfer is bidirectional between masters and slaves.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization is used as a handshake mechanism to suspend and resume serial transfer.
- I2C-bus can be used for test and diagnostic purposes.
- Generation and detection of 7-bit/10-bit addressing and General Call.

14.3 PIN DESCRIPTION

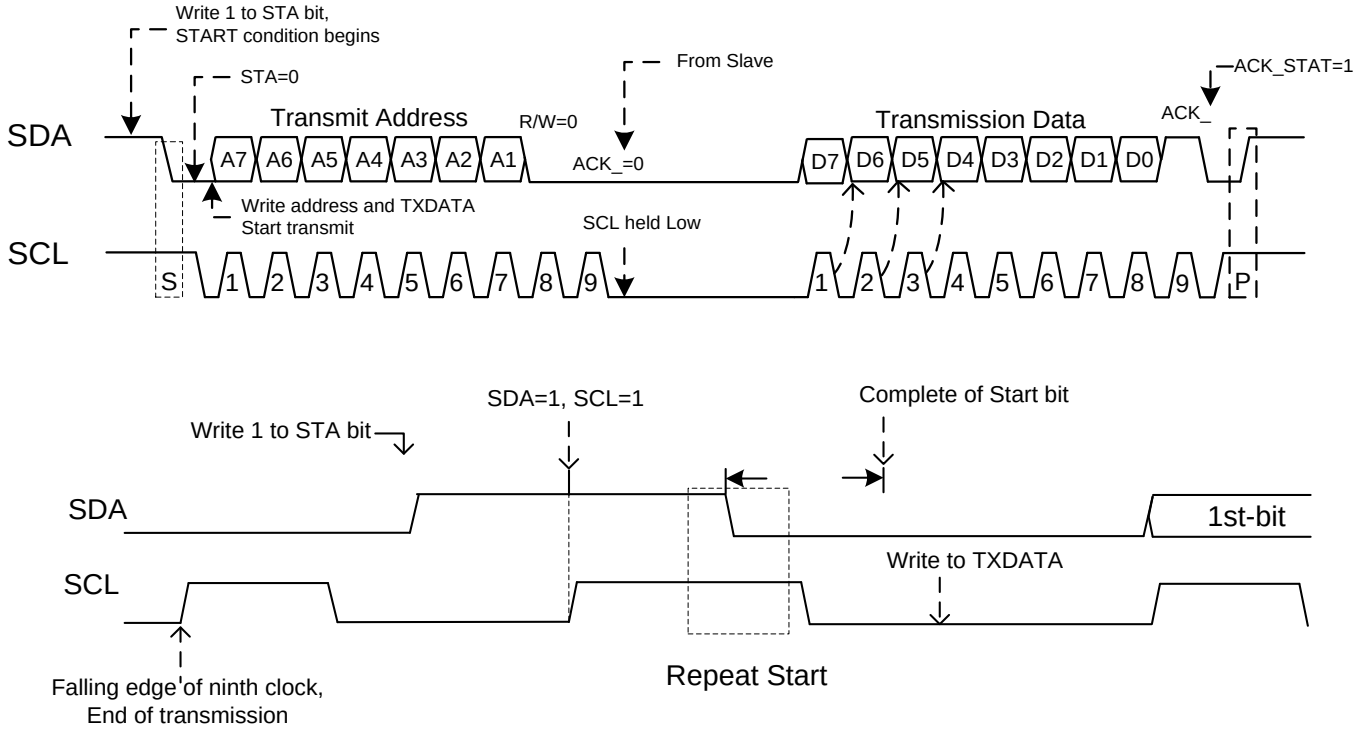
Pin Name	Type	Description	GPIO Configuration
SCLn	I/O	I2C Serial clock	Output with Open-drain Input depends on GPIOn_CFG
SDAn	I/O	I2C Serial data	Output with Open-drain Input depends on GPIOn_CFG

14.4 WAVE CHARACTERISTICS

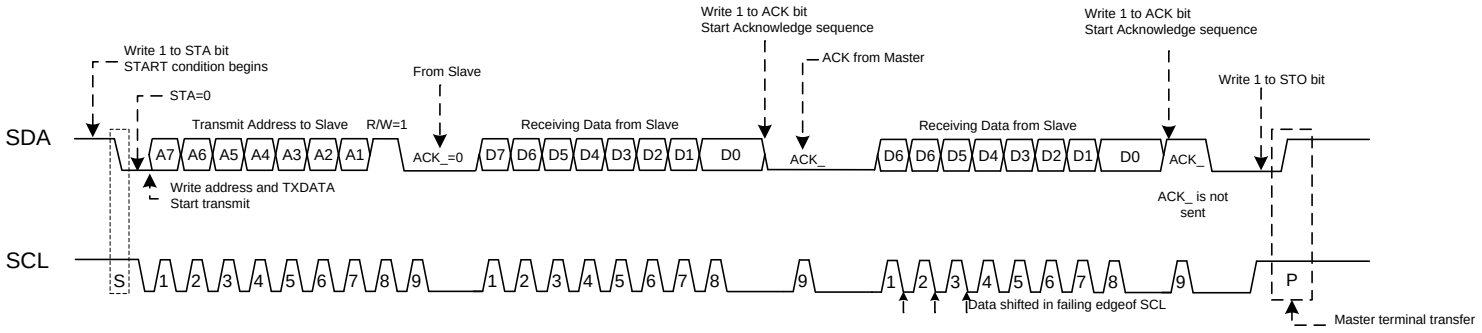


14.5 I2C MASTER MODES

14.5.1 MASTER TRANSMITTER MODE



14.5.2 MASTER RECEIVER MODE



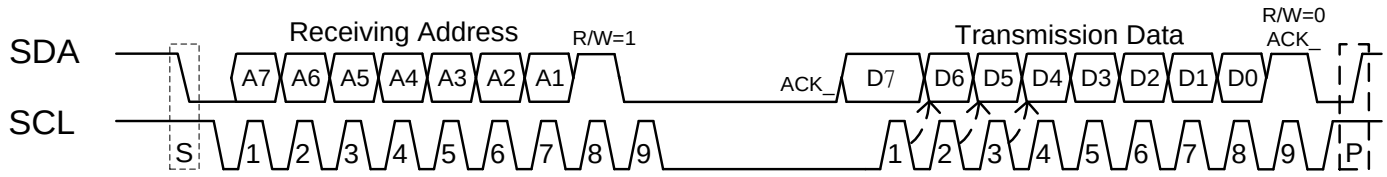
14.5.3 ARBITRATION

In the master transmitter mode, the arbitration logic checks that every transmitted logic 1 actually appears as logic 1 on the I2C bus. If another device on the bus overrules a logic 1 and pulls the SDA line low, arbitration is lost, and the I2C block immediately changes from master transmitter to slave receiver. The I2C block will continue to output clock pulses (on SCL) until transmission of the current serial byte is complete.

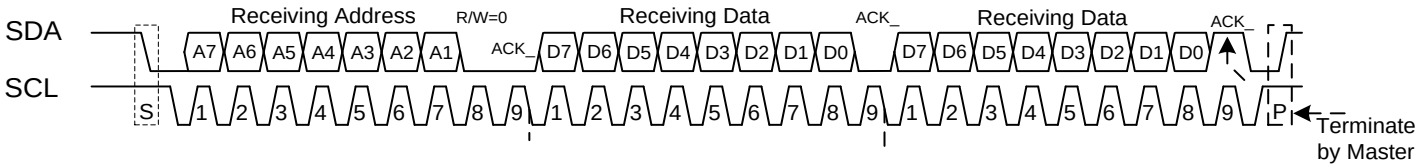
Arbitration may also be lost in the master receiver mode. Loss of arbitration in this mode can only occur while the I2C block is returning a “not acknowledge” to the bus. Arbitration is lost when another device on the bus pulls this signal low. Since this can occur only at the end of a serial byte, the I2C block generates no further clock pulses.

14.6 I2C SLAVE MODES

14.6.1 SLAVE TRANSMITTER MODE



14.6.2 SLAVE RECEIVER MODE



14.7 I2C REGISTERS

Base Address: 0x4001 8000 (I2C0)
0x4005 A000 (I2C1)

14.7.1 I2C n Control register (I2Cn_CTRL) (n=0,1)

Address Offset: 0x00

Setting of the bits in this register controls operation of the I2C interface.

When STA =1 and the I2C interface is not already in master mode, it enters master mode, checks the bus and generates a START condition if the bus is free. If the bus is not free, it waits for a STOP condition (which will free the bus) and generates a START condition after a delay of a half clock period of the internal clock generator. If the I2C interface is already in master mode and data has been transmitted or received, it transmits a Repeated START condition. STA may be set at any time, including when the I2C interface is in an addressed slave mode.

When STO = 1 in master mode, a STOP condition is transmitted on the I2C bus. When the bus detects the STOP condition, STO is cleared automatically. In slave mode, setting STO bit can recover from an error condition. In this case, no STOP condition is transmitted to the bus. The HW behaves as if a STOP condition has been received and it switches to “not addressed” slave receiver mode.

If STA and STO are both set, then a STOP condition is transmitted on the I2C bus if it the interface is in master mode, and transmits a START condition thereafter. If the I2C interface is in slave mode, an internal STOP condition is generated, but is not transmitted on the bus.

✸ ***Note:***

1. ***I2CEN shall be set at last.***
2. ***HW will assign SCL0/SCL1 and SDA0/SDA1 pins as output pins with open-drain function instead of GPIO automatically.***
3. ***ACK and NACK bits can’t both be “1” when receiving data.***
4. ***User has to write 1 to ACK or NACK bit in Master mode to continue next RX process.***

Bit	Name	Description	Attribute	Reset
31:9	Reserved		R	0
8	I2CEN	I2C Interface enable bit 0: Disable. The STO bit is forced to “0”. 1: Enable. I2EN shall not be used to temporarily release the I2C bus since the bus status is lost when I2CEN resets. The ACK flag should be used instead.	R/W	0
7:6	Reserved		R	0
5	STA	START bit. 0: No START condition or Repeated START condition will be generated. 1: Cause the I2C interface to enter master mode and transmit a START or a Repeated START condition. Automatically cleared by HW.	R/W	0
4	STO	STOP flag 0: Stop condition idle. 1: Cause the I2C interface to transmit a STOP condition in master mode, or recover from an error condition in slave mode. Automatically cleared by HW.	R/W	0
3	Reserved		R	0
2	ACK	Assert ACK flag. HW will clear after issuing ACK automatically. 0: Master mode→ No function Slave mode→Return a NACK after receiving address or data. 1: An ACK will be returned during the acknowledge clock pulse on SCLn when ➢ The address in the Slave Address register has been received. ➢ The General Call address has been received while the General Call enable bit (GCEN) in SLVADDR0 register is set. ➢ A data byte has been received while the I2C is in the master	R/W	0

		receiver mode. ➢ A data byte has been received while the I2C is in the addressed slave receiver mode.		
1	NACK	Assert NACK flag. HW will clear after issuing NACK automatically. 0: No function 1: An NACK will be returned during the acknowledge clock pulse on SCLn when ➢ A data byte has been received while the I2C is in the master receiver mode.	R/W	0
0	Reserved		R	0

14.7.2 I2C n Status register (I2Cn_STAT) (n=0,1)

Address Offset: 0x04

Check this register when I2C interrupt occurs, and all status will be cleared automatically by writing I2Cn_CTRL or I2Cn_TXDATA register.

While I2CIF =1, the low period of the serial clock on the SCL line is stretched, and the serial transfer is suspended. When SCL is HIGH, it is unaffected by the state of I2CIF.

Following events will trigger I2C interrupt if I2C interrupt is enabled in NVIC interrupt controller.

- **START/Repeat START condition**
- **STOP condition**
- **Timeout**
- **Data byte transmitted or received**
- **ACK Transmit or received**
- **NACK Transmit or received**

Bit	Name	Description	Attribute	Reset
31:16	Reserved		R	0
15	I2CIF	I2C Interrupt flag. 0: I2C status doesn't change. 1: Read→I2C status changes. Write→Clear this flag.	R/W	0
14:10	Reserved		R	0
9	TIMEOUT	Time-out status 0: No Timeout 1: Timeout	R	0
8	LOST_ARB	Lost arbitration 0: Not lost arbitration 1: Lost arbitration	R	0
7	SLV_TX_HIT	0: No matched slave address. 1: Slave address hit, and is called for TX in slave mode.	R	0
6	SLV_RX_HIT	0: No matched slave address. 1: Slave address hit, and is called for RX in slave mode.	R	0
5	MST	Master/Slave status 0: I2C is in Slave state. 1: I2C is in Master state.	R	0
4	START_DN	Start done status 0: No START bit. 1: MASTER mode→ a START bit was issued. SLAVE mode→a START bit was received.	R	0
3	STOP_DN	Stop done status 0: No STOP bit. 1: MASTER mode→a STOP condition was issued. SLAVE mode→a STOP condition was received.	R	0
2	NACK_STAT	NACK done status 0 : Not received a NACK 1 : Received a NACK	R	0

1	ACK_STAT	ACK done status 0 : Not received an ACK 1 : Received an ACK	R	0
0	RX_DN	RX done status 0: No RX with ACK/NACK transfer. 1: 8-bit RX with ACK/NACK transfer is done.	R	0

14.7.3 I2C n TX Data register (I2Cn_TXDATA) (n=0,1)

Address Offset: 0x08

This register contains the data to be transmitted.

In Master TX mode, CPU writes this register will trigger a TX function. In Slave TX mode, CPU has to write this register before next TX procedure.

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7:0	DATA[7:0]	Data to be transmitted.	R/W	0x00

14.7.4 I2C n RX Data register (I2Cn_RXDATA) (n=0,1)

Address Offset: 0x0C

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7:0	DATA[7:0]	Contains the data received. Read this register when RX_DN = 1.	R	0x00

14.7.5 I2C n Slave Address 0 register (I2Cn_SLVADDR0) (n=0,1)

Address Offset: 0x10

Only used in slave mode. In master mode, this register has no effect.
If this register contains 0x00, the I2C will not acknowledge any address on the bus. Register ADR0 to ADR3 will be cleared to this disabled state on reset.

Bit	Name	Description	Attribute	Reset
31	ADD_MODE	Slave address mode. 0 : 7-bit address mode 1: 10-bit address mode	RW	0
30	GCEN	General call address enable bit. 0: Disable 1: Enable general call address (0x0)	RW	0
29:10	Reserved		R	0
9:0	ADDR[9:0]	The I2C slave address. ADD[9:0] is valid when ADD_MODE = 1 ADD[7:1] is valid when ADD_MODE = 0	R/W	0

14.7.6 I2C n Slave Address 1~3 register (I2Cn_SLVADDR1~3) (n=0,1)

Address Offset: 0x14, 0x18, 0x1C

Bit	Name	Description	Attribute	Reset
31:10	Reserved		R	0

9:0	ADDR[9:0]	The I2C slave address. ADD[9:0] is valid when ADD_MODE = 1 ADD[7:1] is valid when ADD_MODE = 0	R/W	0

14.7.7 I2C n SCL High Time register (I2Cn_SCLHT) (n=0,1)

Address Offset: 0x20

✸ ***Note: I2C Bit Frequency = I2Cn_PCLK / (I2Cn_SCLHT+I2Cn_SCLLT)***

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7:0	SCLH[7:0]	Count for SCL High Period time SCL High Period Time = (SCLH+1) * I2C0_PCLK cycle	R/W	0x04

14.7.8 I2C n SCL Low Time register (I2Cn_SCLLT) (n=0,1)

Address Offset: 0x24

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7:0	SCLL[7:0]	Count for SCL Low Period time SCL Low Period Time = (SCLL+1) * I2C0_PCLK cycle	R/W	0x04

14.7.9 I2C n Timeout Control register (I2Cn_TOCTRL) (n=0,1)

Address Offset: 0x2C

Timeout happens when Master/Slave SCL remained LOW for:

TO * 32 * I2C0_PCLK cycle

When I2C timeout occurs, the I2C transfer will return to “IDLE” state, and issue a TO interrupt to inform user. That means SCL/SDA will be released by HW after timeout. User can issue a STOP after timeout interrupt occurred in Master mode.

Time-out status will be cleared automatically by writing I2Cn_CTRL or I2Cn_TXDATA register.

Bit	Name	Description	Attribute	Reset
31:16	Reserved		R	0
15:0	TO[15:0]	Count for checking Timeout. 0: Disable Timeout checking N: Timeout period time = N*32*I2Cn_PCLK cycle	R/W	0x0

15 UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER (UART)

15.1 OVERVIEW

The UART offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. The serial interface is applied to low speed data transfer and communicate with low speed peripheral devices. The UART offers a very wide range of baud rates using a fractional baud rate generator.

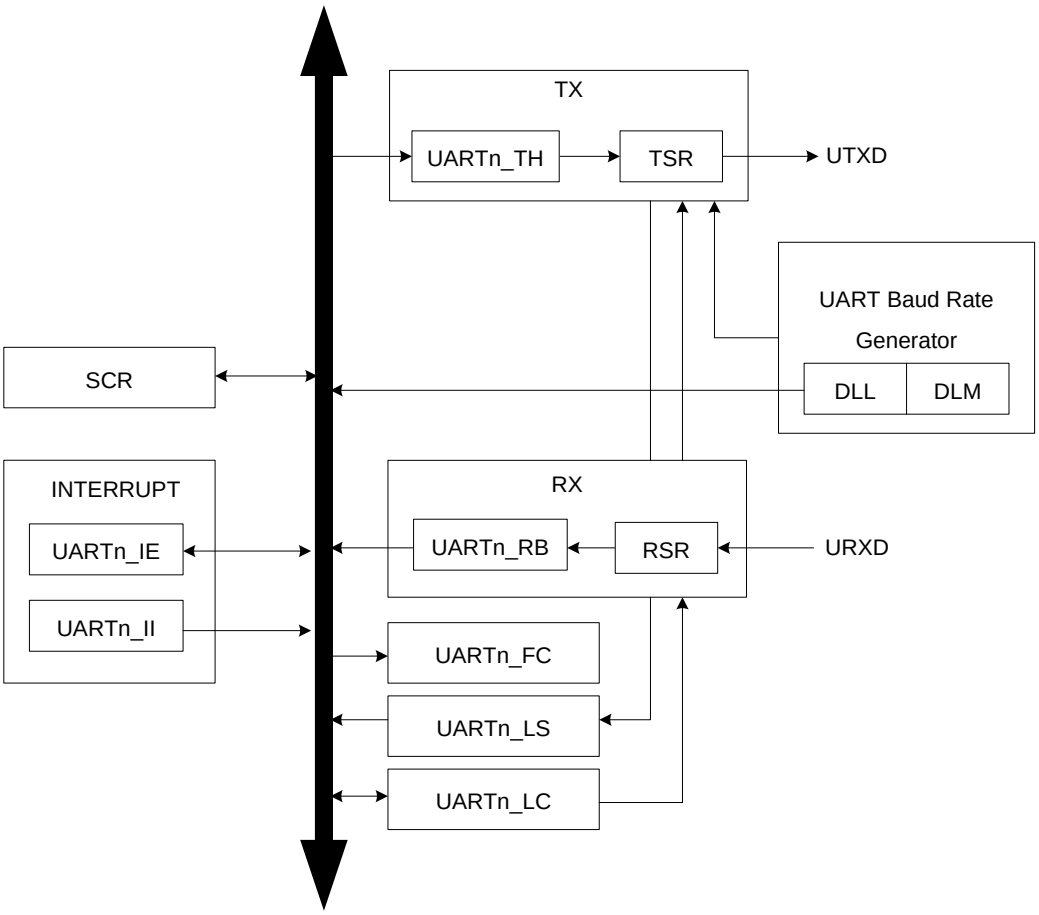
15.2 FEATURES

- Full-duplex, 2-wire asynchronous data transfer.
- Single-wire half-duplex communication
- Register locations conform to 16550 industry standard.
- Receiver FIFO trigger points at 1 byte
- Built-in baud rate generator.
- Software or hardware flow control.

15.3 PIN DESCRIPTION

Pin Name	Type	Description	GPIO Configuration
UTXDn	O	Serial Transmit data.	
URXDn	I	Serial Receive data.	Depends on GPIOn_CFG

15.4 BLOCK DIAGRAM



15.5 BAUD RATE CALCULATION

The UART baud rate is calculated as:

$$UART_{BAUDRATE} = \frac{UARTn\_PCLK}{Oversampling \times (256 \times DLM + DLL) \times (1 + DIVADDVAL / MULVAL)}$$

Where UARTn_PCLK is the peripheral clock, UARTn_DLM and UARTn_DLL are the standard UART baud rate divider registers, and DIVADDVAL and MULVAL are UART fractional baud rate generator specific parameters in UARTn_FD register.

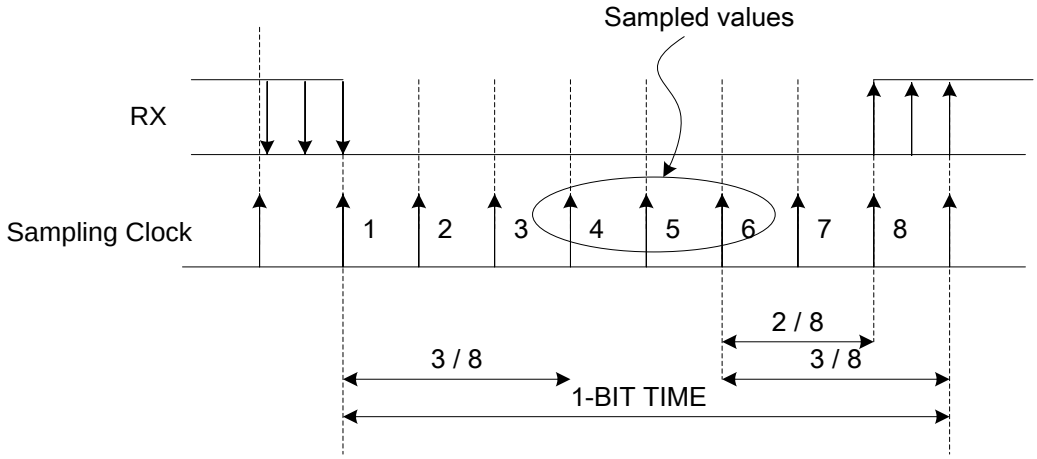
The value of MULVAL and DIVADDVAL should comply with the following conditions:

1. 1 ≤ MULVAL ≤ 15
2. 0 ≤ DIVADDVAL ≤ 14
3. DIVADDVAL< MULVAL
4. MULVAL – DIVADDVAL≠2
5. Oversampling is 8 or 16

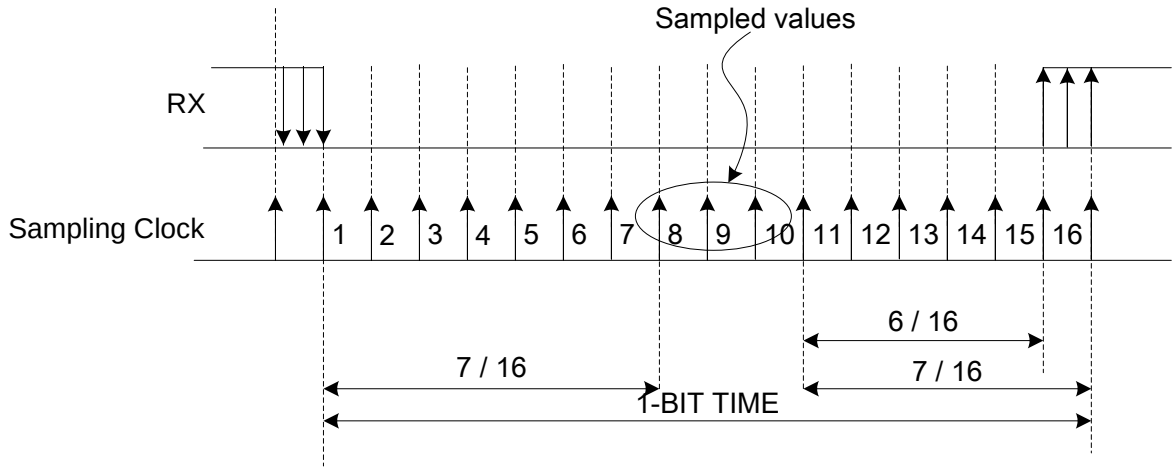
The value of the UARTn_FD register should not be modified while transmitting/receiving data or data may be lost or corrupted.

The oversampling method can be selected by programming the OVER8 bit in UARTn_FD register and can be either 16 or 8 times the baud rate clock.

● OVER8=1: Oversampling by 8 to achieve higher speed (up to UARTn_PCLK/8). In this case the maximum receiver tolerance to clock deviation is reduced.



● OVER8=0: Oversampling by 16 to increase the tolerance of the receiver to clock deviations. In this case, the maximum speed is limited to maximum UARTn_PCLK/16



If the UARTn_FD register value does not comply with these two requests, then the fractional divider output is undefined. If DIVADDVAL is zero then the fractional divider is disabled, and the clock will not be divided.

UART can operate with or without using the Fractional Divider. The desired baud rate can be achieved using several different Fractional Divider settings. The following algorithm illustrates one way of finding a set of DLM, DLL, MULVAL, and DIVADDVAL values. Such set of parameters yields a baud rate with a relative error of less than 1.1% from the desired one.

The following example illustrates selecting the DIVADDVAL, MULVAL, DLM, and DLL to generate BR = 115200 when UARTn_PCLK = 12 MHz, and Oversampling = 16.

$$UART_{BAUDRATE} = \frac{UARTn\_PCLK}{Oversampling \times (256 \times DLM + DLL) \times (1 + DIVADDVAL / MULVAL)}$$

$$115200 = \frac{12000000}{16 \times (256 \times DLM + DLL) \times (1 + DIVADDVAL / MULVAL)}$$

$$(256 \times DLM + DLL) \times (1 + DIVADDVAL / MULVAL) = 6.51$$

Since the value of MULVAL and DIVADDVAL should comply with the following conditions:

1. $1 \leq MULVAL \leq 15$
2. $0 \leq DIVADDVAL \leq 14$
3. DIVADDVAL< MULVAL
4. $MULVAL - DIVADDVAL \neq 2$

Thus, the suggested UART settings would be: DLM = 0, DLL = 4, DIVADDVAL = 5, and MULVAL = 8 (fill in 7 in the MULVAL bits). The baud rate generated is 115384, and has a relative error of 0.16% from the originally specified 115200.

15.6 AUTO-BAUD FLOW

15.6.1 AUTO-BAUD

The UART auto-baud function can be used to measure the incoming baud rate based on the “AT” protocol (Hayes command). If enabled the auto-baud feature will measure the bit time of the receive data stream and set the divisor latch registers UARTn_DLM and UARTn_DLL accordingly.

Auto-baud function is started by setting the START bit in UARTn_ABCTRL register, and can be stopped by clearing the START bit. The START bit will clear once auto-baud has finished and reading the bit will return the status of auto-baud (pending/finished). When auto-baud function is started, FIFO will be cleared, not available to write the TX FIFO, and the

transmitter will stop transmitting until auto-baud function finishes or be stopped.

Two auto-baud measuring modes are available which can be selected by the MODE bit in UARTn_ABCTRL register. In Mode 0 the baud rate is measured on two subsequent falling edges of the UART RX pin (the falling edge of the start bit and the falling edge of the least significant bit). In Mode 1 the baud rate is measured between the falling edge and the subsequent rising edge of the UART RX pin (the length of the start bit).

The AUTORESTART bit in UARTn_ABCTRL register can be used to automatically restart baud rate measurement if a timeout occurs (the rate measurement counter overflows). If this bit is set, the rate measurement will restart at the next falling edge of the URXD pin.

The auto-baud function can generate two interrupts.

- The ABTOINT interrupt in UARTn_II register will get set if the interrupt is enabled (ABTOIE bit in UARTn_IE register is set and the auto-baud rate measurement counter overflows).
- The ABEOINT interrupt in UARTn_II register will get set if the interrupt is enabled (ABTOIE bit in UARTn_IE register is set and the auto-baud has completed successfully).

The auto-baud interrupts have to be cleared by setting the corresponding ABTOINTCLR and ABEOIE bits in UARTn_IE register.

The fractional baud rate generator must be disabled (DIVADDVAL = 0) during auto-baud. Also, when auto-baud is used, any write to UARTn_DLM and UARTn_DLL registers should be done before UARTn_ABCCTRL register write. The minimum and the maximum baud rates supported by UART are a function of UARTn_PCLK and the number of data bits, stop bits and parity bits.

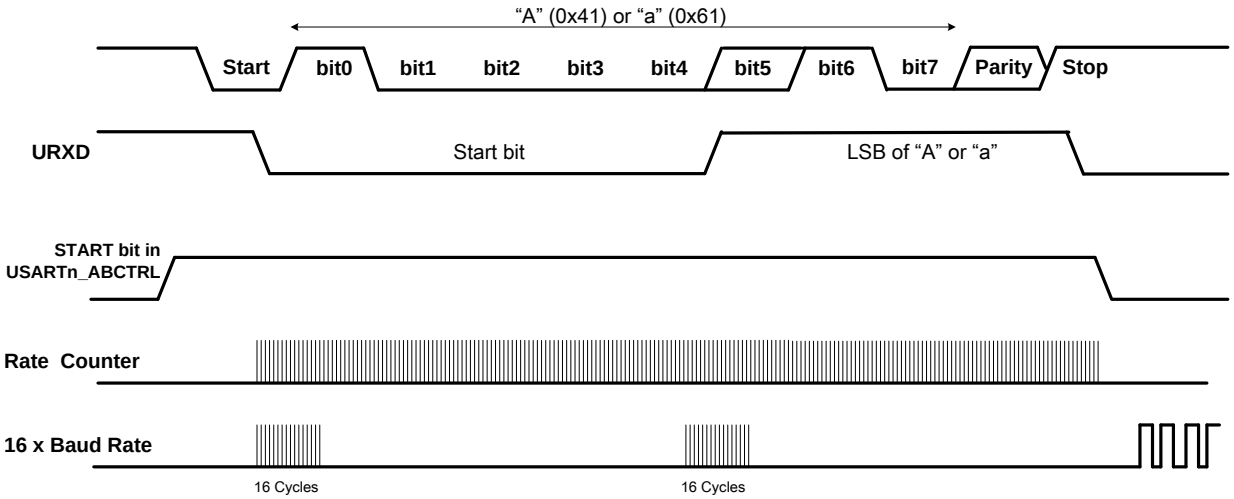
$$ratemin = \frac{2 \times PCLK}{16 \times 2^{15}} \leq UART_{baudrate} \leq \frac{PCLK}{16 \times (2 + databits + paritybits + stopbits)} = ratemax$$

15.6.2 AUTO-BAUD MODES

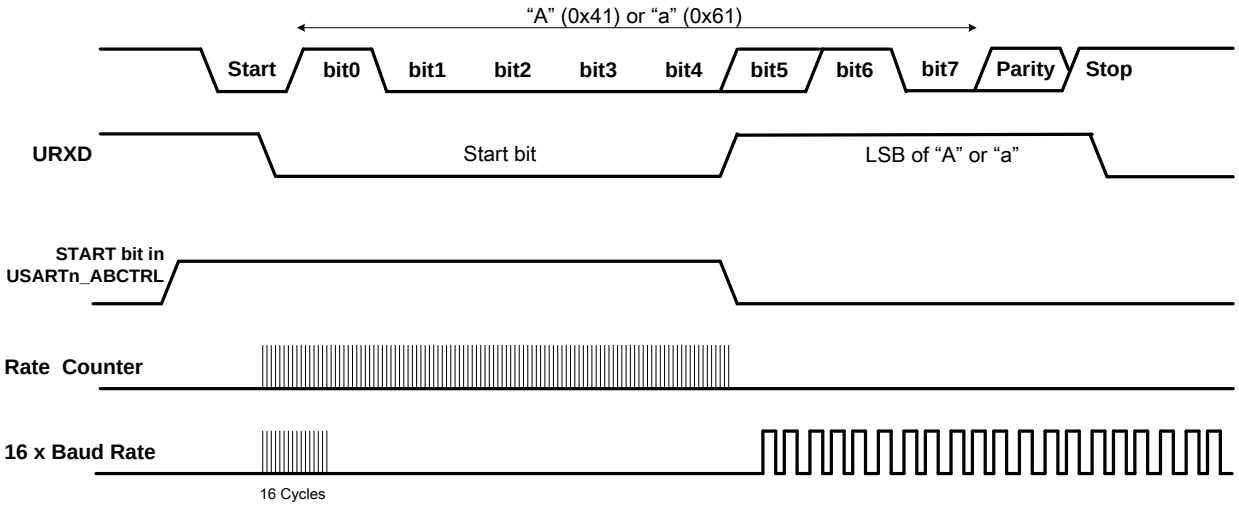
When the SW is expecting an “AT” command, it configures the UART with the expected character format and sets the ACR Start bit. The initial values in the divisor latches DLM and DLM don‘t care. Because of the “A” or “a” ASCII coding (“A” = 0x41, “a” = 0x61), the UART Rx pin sensed start bit and the LSB of the expected character are delimited by two falling edges. When the ACR Start bit is set, the auto-baud protocol will execute the following phases:

1. On START bit setting, the baud rate measurement counter is reset and the RSR is reset. The RSR baud rate is switched to the highest rate.
2. A falling edge on URXD pin triggers the beginning of the start bit. The rate measuring counter will start counting UARTn_PCLK cycles.
3. During the receipt of the start bit, 16 pulses are generated on the RSR baud input with the frequency of the UART input clock, guaranteeing the start bit is stored in the RSR.
4. During the receipt of the start bit (and the character LSB for MODE = 0 in UARTn_ABCTRL register), the rate counter will continue incrementing with the pre-scaled UART input clock (UARTn_PCLK).
5. If MODE = 0, the rate counter will stop on next falling edge of the UART RX pin. If MODE = 1, the rate counter will stop on the next rising edge of the URXD pin.
6. The rate counter is loaded into UARTn_DLM/UARTn_DLL and the baud rate will be switched to normal operation. After setting the DLM/DLL, the end of auto-baud interrupt ABEOINT in UARTn_II register will be set, if enabled. The RSR will now continue receiving the remaining bits of the character.

➢ **AUTO-BAUD RATE MODE 0 Waveform**



➢ **AUTO-BAUD RATE MODE 1 Waveform**



15.7 UART REGISTERS

Base Address: 0x4001 6000 (UART0)
0x4005 6000 (UART1)
0x4005 4000 (UART2)
0x4005 2000 (UART3)

15.7.1 UART n Receiver Buffer register (UARTn_RB) (n=0,1,2,3)

Address Offset: 0x00

This register is the byte of the UART RX FIFO, and contains the character received and can be read via the bus interface. The LSB (bit 0) contains the first-received data bit. If the character received is less than 8 bits, the unused MSBs are padded with zeros.

The Divisor Latch Access Bit (DLAB) in the UARTn_LC register must be zero in order to access this register.
Since PE, FE and BI bits correspond to the byte on the top of the UART RX FIFO (i.e. the one that will be read in the next read from this register), the right approach for fetching the valid pair of received byte and its status bits is first to read the content of the UARTn_LS register, and then to read a byte from this register.

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7:0	RB[7:0]	Contains the received byte in the UART RX FIFO.	R	0

15.7.2 UART n Transmitter Holding register (UARTn_TH) (n=0,1,2,3)

Address Offset: 0x00

This register is the byte of the UART TX FIFO. The byte is the character in the TX FIFO and can be written via the bus interface. The LSB represents the first bit to transmit.
The Divisor Latch Access Bit (DLAB) in UARTn_LC register must be zero in order to access this register.

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7:0	TH[7:0]	The byte will be sent when it is the byte in TX FIFO and the transmitter is available.	W	0

15.7.3 UART n Divisor Latch LSB registers (UARTn_DLL) (n =0,1,2,3)

Address Offset: 0x00

The UART Divisor Latch is part of the UART Baud Rate Generator and holds the value used (optionally with the Fractional Divider) to divide the UARTn_PCLK clock in order to produce the baud rate clock, which must be the multiple of the desired baud rate that is specified by the Oversampling Register (typically 16X).

The UARTn_DLL and UARTn_DLM registers together form a 16-bit divisor, and DLAB bit in UARTn_LC register must be one in order to access these registers.

DLL contains the lower 8 bits of the divisor and DLM contains the higher 8 bits. A zero value is treated like 0x0001.

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7:0	DLL[7:0]	The UART Divisor Latch LSB Register, along with the DLM register, determines the baud rate of the UART.	R/W	0

15.7.4 UART n Divisor Latch MSB register (UARTn_DLM) (n=0,1,2,3)

Address Offset: 0x04

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7:0	DLM[7:0]	The UART Divisor Latch MSB Register, along with the DLL register, determines the baud rate of the UART.	R/W	0

15.7.5 UART n Interrupt Enable register (UARTn_IE) (n=0,1,2,3)

Address Offset: 0x04

The DLAB bit in the UARTn_LC register must be zero in order to access this register.

Bit	Name	Description	Attribute	Reset
31:10	Reserved		R	0
9	ABTOIE	Enables the auto-baud time-out interrupt enable bit. 0: Disable 1: Enable	R/W	0
8	ABEOIE	End of auto-baud interrupt enable bit. 0: Disable 1: Enable	R/W	0
7:5	Reserved		R	0
4	TEMTIE	TEMT interrupt enable bit. The status of this interrupt can be read from TEMT bit in UARTn_LS register. 0: Disable 1: Enable	R/W	0
3	Reserved		R	0
2	RLSIE	Receive Line Status (RLS) interrupt enable bit. The status of this interrupt can be read from UARTn_LS[4:1]. 0: Disable 1: Enable	R/W	0
1	THREIE	THRE interrupt enable bit. The status of this interrupt can be read from THRE bit in UARTn_LS register. 0: Disable 1: Enable	R/W	0
0	RDAIE	RDA interrupt enable bit. Enables the Receive Data Available interrupt. It also controls the Character Receive Time-out interrupt. 0: Disable 1: Enable	R/W	0

15.7.6 UART n Interrupt Identification register (UARTn_II) (n=0,1,2,3)

Address Offset: 0x08

This register provides a status code that denotes the priority and source of a pending interrupt.
The interrupts are frozen during a UARTn_II register access. If an interrupt occurs during a UARTn_II register access, the interrupt is recorded for the next UARTn_II register access.

Bit	Name	Description	Attribute	Reset
31:10	Reserved		R	0
9	ABTOIF	Auto-baud time-out interrupt flag. 0: Auto-baud has not timed-out	R	0

		1: Auto-baud has timed out and interrupt is enabled.		
8	ABEOIF	End of auto-baud interrupt flag 0: Auto-baud has not finished. 1: Auto-baud has finished successfully and interrupt is enabled.	R	0
7:4	Reserved		R	0100b
3:1	INTID[2:0]	Interrupt identification which identifies an interrupt corresponding to the USARTn RX FIFO. 0x3: 1 - Receive Line Status (RLS). 0x2: 2a - Receive Data Available (RDA). 0x1: 3a - THRE Interrupt. 0x7: 3b – TEMT Interrupt. Other: Reserved	R	0
0	INTSTATUS	Interrupt status. The pending interrupt can be determined by evaluating USARTn_II[3:1]. 0: At least one interrupt is pending. 1: No interrupt is pending.	R	1

Bits UARTn_II[9:8] are set by the auto-baud function and signal a time-out or end of auto-baud condition. The auto-baud interrupt conditions are cleared by setting the corresponding Clear bits in the Auto-baud Control Register.

Given the status of UARTn_II[3:0], an interrupt handler routine can determine the cause of the interrupt and how to clear the active interrupt. The UARTn_II register must be read in order to clear the interrupt prior to exiting the Interrupt service routine.

Interrupt	USARTn_II [3:0]	Priority	Interrupt Source	Interrupt Reset
RLS	0110	Highest	Overrun error (OE), Parity error (PE), Framing error (FE) or Break interrupt (BI)	Read UARTn_LS register
RDA	0100	2nd	RX data in FIFO reached trigger level (FCR0=1)	Read UARTn_RB register or UART FIFO drops below trigger level
THRE	0010	3rd	THRE	Read UARTn_II register (if source of interrupt) or Write THR register
TEMT	1110	3rd	TEMT	Read UARTn_II register (if source of interrupt) or Write THR register

15.7.7 UART n FIFO Control register (UARTn_FIFOCTRL) (n=0,1,2,3)

Address Offset: 0x08

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7:6	RXTL[1:0]	RX Trigger Level. These two bits determine how many receiver UART FIFO characters must be written before an interrupt is activated. 00: Trigger level 0 (1 character) Other: Reserved	W	0
5:1	Reserved		R	0
0	FIFOEN	FIFO enable 0: No effect 1: Enable for both UART Rx and TX FIFOs and UARTn_FIFOCTRL[7:1] access. This bit must be set for proper UART operation.	W	1

15.7.8 UART n Line Control register (UARTn_LC) (n=0,1,2,3)

Address Offset: 0x0C

This register determines the format of the data character that is to be transmitted or received.

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7	DLAB	Divisor Latch Access bit 0: Disable access to Divisor Latches. 1: Enable access to Divisor Latches.	R/W	0
6	BC	Break Control bit 0: Disable break transmission. 1: Enable break transmission. Output pin UART TXD is forced to logic 0.	R/W	0
5:4	PS[1:0]	Parity Select bits 00: Odd parity. Number of 1s in the transmitted character and the attached parity bit will be odd. 01: Even Parity. Number of 1s in the transmitted character and the attached parity bit will be even. 10: Forced 1 stick parity. 11: Forced 0 stick parity.	R/W	0
3	PE	Parity Enable bit 0: Disable parity generation and checking. 1: Enable parity generation and checking.	R/W	0
2	SBS	Stop Bit Select bit 0: 1 stop bit. 1: 2 stop bits (1.5 if WLS bits=00)	R/W	0
1:0	WLS[1:0]	Word Length Select bits 00: 5-bit character length. 01: 6-bit character length. 10: 7-bit character length. 11: 8-bit character length.	R/W	0

15.7.9 UART n Line Status register (UARTn_LS) (n=0,1,2,3)

Address Offset: 0x14

✸ ***Note:***
- ✸ ***The break interrupt (BI) is associated with the character in the UARTn_RB FIFO.***
- ✸ ***The framing error (FE) is associated with the character in the UARTn_RB FIFO.***
- ✸ ***The parity error (PE) is associated with the character in the UARTn_RB FIFO.***

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7	RXFE	Error in RX FIFO flag. RXFE =1 when a character with a RX error such as framing error, parity error, or break interrupt, is loaded into the UARTn_RB register. This bit is cleared when the UARTn_LS register is read and there are no subsequent errors in the UART FIFO. 0: UARTn_RB register contains no UART RX errors or FIFOEN=0 1: UARTn_RB register contains at least one UART RX error.	R	0
6	TEMT	Transmitter Empty flag TEMT=1 when both THR and TSR are empty; TEMT is cleared when either the TSR or the THR contain valid data. 0: THR and/or TSR contains valid data. 1: THR and TSR are empty.	R	1
5	THRE	Transmitter Holding Register Empty flag THRE indicates that the UART is ready to accept a new character for	R	1

		transmission. In addition, this bit causes the UART to issue THRE interrupt to if THREIE=1. THRE=1 when a character is transferred from the THR into the TSR. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU. 0: THR contains valid data. 1: THR (TX FIFO) is empty.		
4	BI	Break Interrupt flag. When RXD1 is held in the spacing state (all zeros) for one full character transmission (start, data, parity, stop), a break interrupt occurs. Once the break condition has been detected, the receiver goes idle until RXD1 goes to marking state (all ones). A UARTn_LS register read clears BI bit. The time of break detection is dependent on FIFOEN bit in UARTn_FIFOCTRL register. 0: Break interrupt status is inactive. 1: Break interrupt status is active.	R	0
3	FE	Framing Error flag. When the stop bit of a received character is a logic 0, a framing error occurs. A UARTn_LS register read clears FE bit. The time of the framing error detection is dependent on FIFOEN bit in UARTn_FIFOCTRL register. Upon detection of a framing error, the RX will attempt to re-synchronize to the data and assume that the bad stop bit is actually an early start bit. However, it cannot be assumed that the next received byte will be correct even if there is no Framing Error. 0: Framing error status is inactive. 1: Framing error status is active.	R	0
2	PE	Parity Error flag. When the parity bit of a received character is in the wrong state, a parity error occurs. A UARTn_LS register read clears PE bit. Time of parity error detection is dependent on FIFOEN bit in UARTn_FIFOCTRL register. 0: Parity error status is inactive. 1: Parity error status is active.	R	0
1	OE	Overrun Error flag. The overrun error condition is set as soon as it occurs. A UARTn_LS register read clears OE bit. OE=1 when UART RSR has a new character assembled and the UARTn_RB FIFO is full. In this case, the USARTn_RB FIFO will not be overwritten and the character in the USARTn_RS register will be lost. 0: Overrun error status is inactive. 1: Overrun error status is active.	R	0
0	RDR	Receiver Data Ready flag RDR=1 when the UARTn_RB FIFO holds an unread character and is cleared when the UARTn_RB FIFO is empty. 0: UARTn_RB FIFO is empty. 1: UARTn_RB FIFO contains valid data.	R	0

15.7.10 UART n Scratch Pad register (UARTn_SP) (n=0,1,2,3)

Address Offset: 0x1C

This register has no effect on the UART operation. This register can be written and/or read at user's discretion. There is no provision in the interrupt interface that would indicate to the host that a read or write of this register has occurred.

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7:0	PAD[7:0]	A readable, writable byte.	R/W	0

15.7.11 UART n Auto-baud Control register (UARTn_ABCTRL) (n=0,1,2,3)

Address Offset: 0x20

This register controls the process of measuring the incoming clock/data rate for the baud rate generation and can be

read and written at user's discretion. Besides, it also controls the clock pre-scaler for the baud rate generation. The reset value of the register keeps the fractional capabilities of UART disabled making sure that UART is fully SW and HW compatible with UARTs not equipped with this feature.

Bit	Name	Description	Attribute	Reset
31:10	Reserved		R	0
9	ABTOIFC	Auto-baud time-out interrupt flag clear bit 0: No effect. 1: Clear ABTOIF bit. This bit is automatically cleared by HW.	W	0
8	ABEOIFC	End of auto-baud interrupt flag clear bit 0: No effect. 1: Clear ABEOIF bit. This bit is automatically cleared by HW.	W	0
7:3	Reserved		R	0
2	AUTORESTART	Restart mode 0: No restart 1: Restart in case of timeout (counter restarts at next UART RX falling edge)	R/W	0
1	MODE	Auto-baud mode select bit. 0: Mode 0. 1: Mode 1.	R/W	0
0	START	This bit is automatically cleared after auto-baud completion. 0: Auto-baud stop (auto-baud is not running). 1: Auto-baud start (auto-baud is running). Auto-baud run bit. This bit is automatically cleared by HW after auto-baud completion.	R/W	0

15.7.12 UART n Fractional Divider register (UARTn_FD) (n=0,1,2,3)

Address Offset: 0x28

This register controls the clock prescaler for the baud rate generation and can be read and written at the user's discretion. This prescaler takes the APB clock and generates an output clock according to the specified fractional requirements.

In most applications, the UART samples received data 16 times in each nominal bit time, and sends bits that are 16 input clocks wide. OVER8 bit allows software to control the ratio between the input clock and bit clock. This is required for smart card mode, and provides an alternative to fractional division for other modes.

✸ ***Note:***
1. ***If the fractional divider is active (DIVADDVAL>0) and UARTn_DLM=0, the value of the UARTn_DLL register must ≥ 3.***
2. ***MULVAL – DIVADDVAL ≠2***

Bit	Name	Description	Attribute	Reset
31:9	Reserved		R	0
8	OVER8	Oversampling value 0: Oversampling by 16 1: Oversampling by 8	R/W	0
7:4	MULVAL[3:0]	Baud rate pre-scaler multiplier value = MULVAL[3:0] +1 0000: Baud rate pre-scaler multiplier value is 1 for HW. 0001: Baud rate pre-scaler multiplier value is 2 for HW. … … 1111: Baud rate pre-scaler multiplier value is 16 for HW.	R/W	0
3:0	DIVADDVAL[3:0]	Baud rate generation pre-scaler divisor value. If this field is 0, fractional baud rate generator will not impact the UART baud rate	R/W	0

15.7.13 UART n Control register (UARTn_CTRL) (n=0,1,2,3)

Address Offset: 0x30

In addition to HW flow control (Auto-CTS and Auto-RTS mechanisms), this register enables implementation of SW flow control.

When TXEN = 1, the UART transmitter will keep sending data as long as they are available. As soon as TXEN bit becomes 0, UART transmission will stop.

It is strongly suggested to let the UART HW implemented auto flow control features take care of limit the scope of TXEN to SW flow control.

✷ ***Note: It is advised that TXEN and RXEN are set in the same instruction if needed in order to minimize the setup and the hold time of the receiver.***

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7	TXEN	When this bit is 1, data written to the UARTn_TH register is output on the TXD pin as soon as any preceding data has been sent. If this bit is cleared to 0 while a character is being sent, the transmission of that character is completed, but no further characters are sent until this bit is set again.	R/W	1
6	RXEN	0: Disable RX related function 1: Enable RX	R/W	1
5:4	Reserved		R	0
3:1	MODE[2:0]	UARTn Mode 000: UART mode. HW will switch GPIO to UTXDn and URXDn. Other: Reserved	R/W	0
0	UARTEN	UART enable 0: Disable 1: Enable. HW switches GPIO to UART pin according to MODE bits automatically.	R/W	0

15.7.14 UART n Half-duplex Enable register (UARTn_HDEN) (n=0,1,2,3)

Address Offset: 0x34

After reset the UART will be in full-duplex mode, meaning that both TX and RX work independently. After setting the HDEN bit, the UART will be in half-duplex mode. In this mode, the UART ensures that the receiver is locked when idle, or will enter a locked state after having received a complete ongoing character reception. Line conflicts must be handled in SW.

The behavior of the UART is unpredictable when data is presented for reception while data is being transmitted. For this reason, the value of the HDEN register should not be modified while sending or receiving data, or data may be lost or corrupted.

Bit	Name	Description	Attribute	Reset
31:1	Reserved		R	0
0	HDEN	Half-duplex mode enable bit 0: Disable 1: Enable	R/W	0

16 I2S

16.1 OVERVIEW

The I2S bus specification defines a 5-wire serial bus, having data in, data out, BCLK, MCLK, and word select signal. The basic I2S connection has one master, which is always the master, and one slave.

16.2 FEATURES

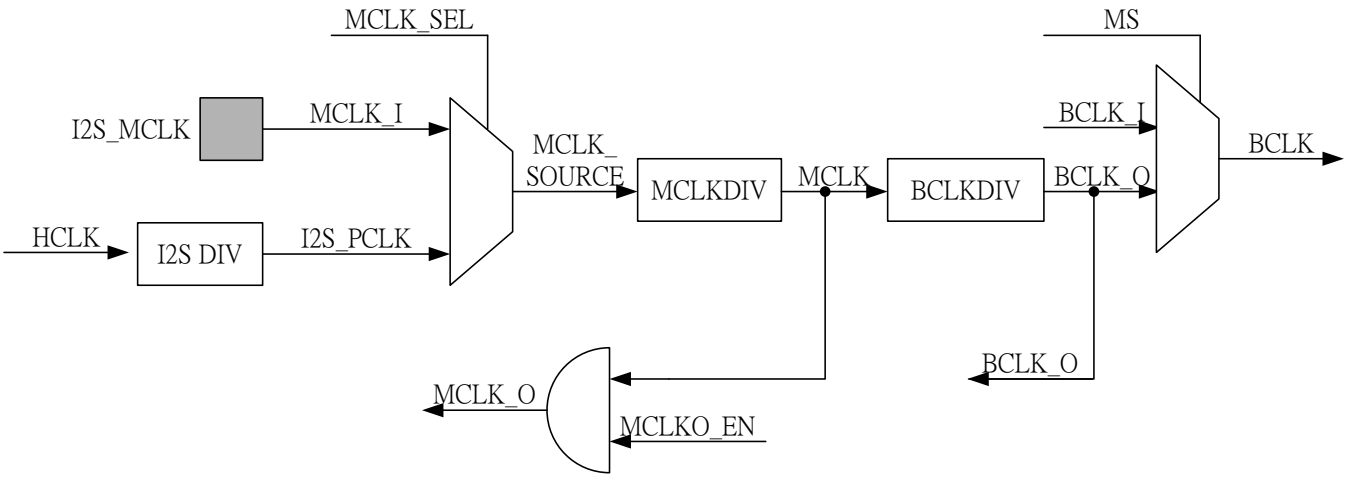
- I2S can operate as either master or slave.
- Capable of handling 8/16/24/32-bit data length.
- Mono and stereo audio data supported.
- I2S and MSB justified data format supported.
- 8 word (32-bit) FIFO data buffers are provided.
- Generate interrupt requests when buffer levels cross a programmable boundary.
- Controls include reset, stop and mute options separately for I2S input and I2S output.

16.3 PIN DESCRIPTION

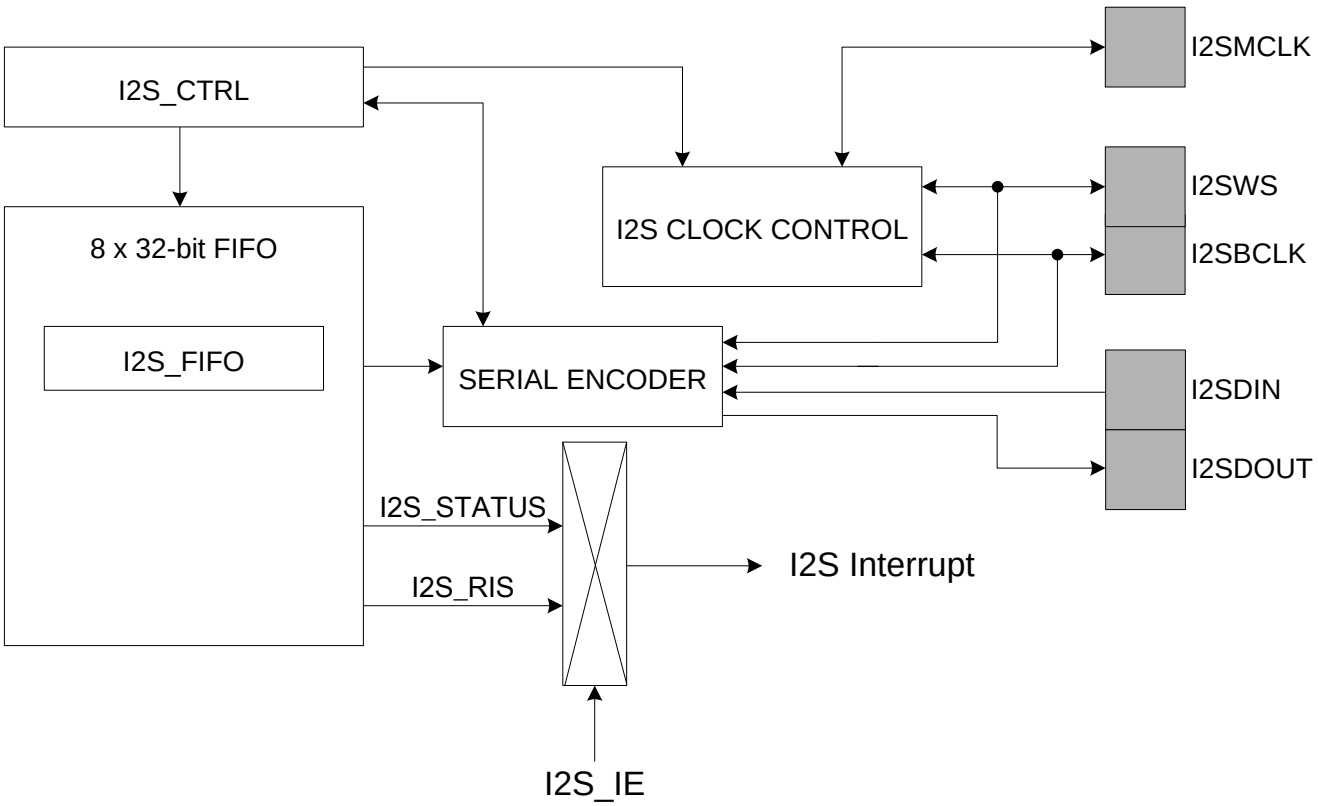
Pin Name	Type	Description	GPIO Configuration
I2SBCLK	O	I2S Bit clock (Master)	
	I	I2S Bit clock (Slave)	Depends on GPIOn_CFG
I2SWS	O	I2S Word Select (Master)	
	I	I2S Word Select (Slave)	Depends on GPIOn_CFG
I2SDIN	I	I2S Received Serial data	Depends on GPIOn_CFG
I2SDOUT	O	I2S Transmitted Serial data	
I2SMCLK	O	I2S Master clock output	
	I	I2S Master clock input from GPIO	Depends on GPIOn_CFG

16.4 BLOCK DIAGRAM

16.4.1 I2S CLCOK CONTROL



16.4.2 I2S BLOCK DIAGRAM

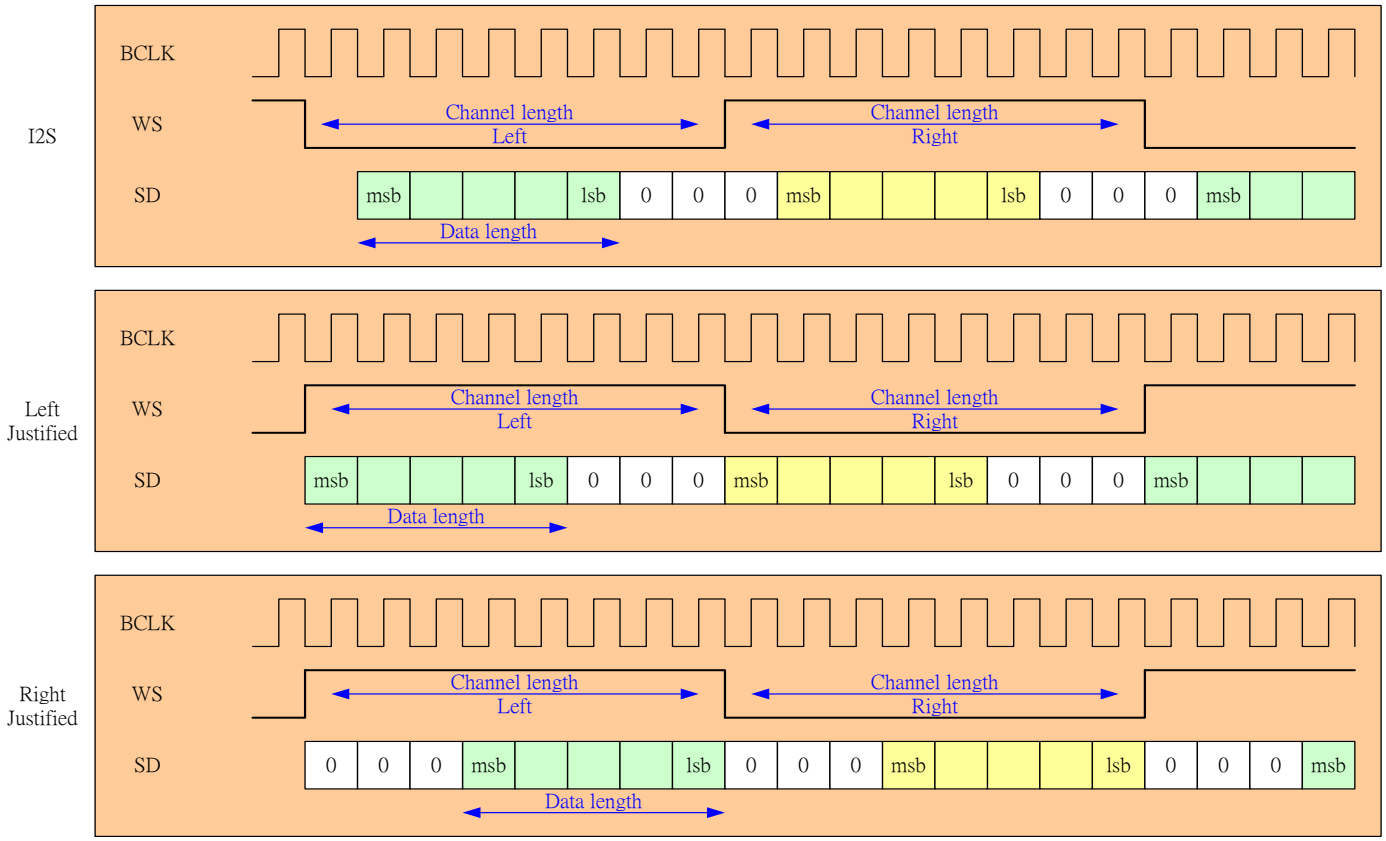


16.5 FUNCTIONAL DESCRIPTION

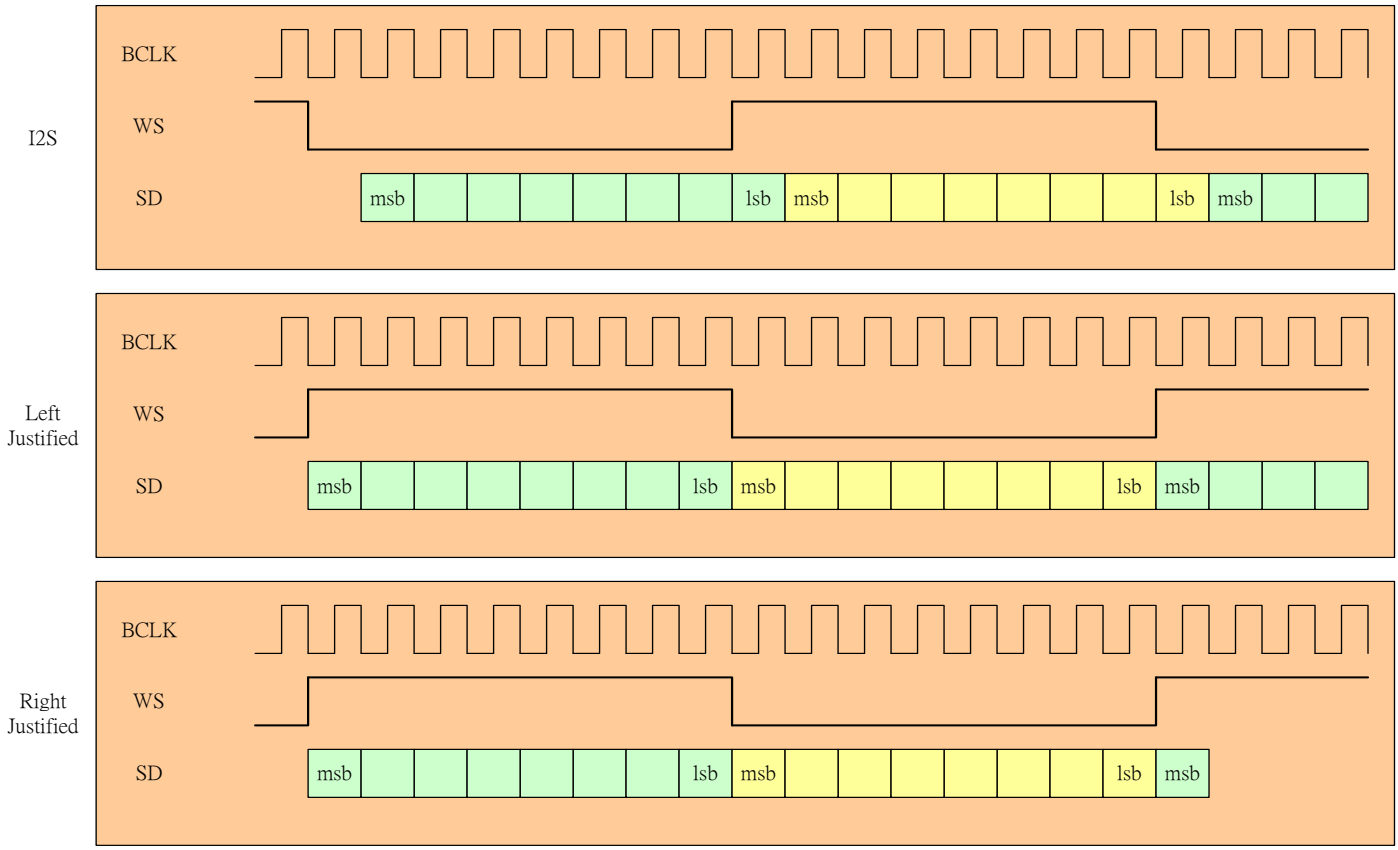
16.5.1 I2S OPERATION

- Standard I2S
- Right-justified Data Format
- MSB (Left)-justified Data Format

Channel Length > Data Length:



Channel Length = Data Length



16.5.2 I2S FIFO OPERAION

16.5.2.1 MONO

8bit

N+3	N+2	N+1	N
N+7	N+6	N+5	N+4

16bit

N+1	N
N+3	N+2

24 bit

	N
	N+1

32 bit

N
N+1

16.5.2.2 STEREO

8bit

RIGHT +1	LEFT +1	RIGHT	LEFT
RIGHT +3	LEFT +3	RIGHT +2	LEFT +2

16bit

RIGHT	LEFT
RIGHT +1	LEFT+1

24 bit

	LEFT
	RIGHT

32 bit

LEFT
RIGHT

16.6 I2S REGISTERS

Base Address: 0x4001 A000 (I2S0)
0x4001 4000 (I2S1)

16.6.1 I2S n Control register (I2Sn_CTRL) (n=0,1)

Address Offset: 0x00

✷ ***Note: START bit shall be set at last.***

Bit	Name	Description	Attribute	Reset
31	I2SEN	I2S enable bit 0: Disable 1: Enable	R/W	0
30:25	Reserved		R	0
24:20	CHLENGTH[4:0]	Bit number of single channel = CHLENGTH[4:0]+1. 0~6: Reserved 7: 8 bits 8: 9 bits … … 31: 32bits (Max)	R/W	0x1F
19	Reserved		R	0
18:16	RXFIFOTH[2:0]	RX FIFO Threshold level 0: RX FIFO threshold level = 0 1: RX FIFO threshold level = 1 … … n: RX FIFO threshold level = n	R/W	0x3
15	Reserved		R	0
14:12	TXFIFOTH[2:0]	TX FIFO Threshold level 0: TX FIFO threshold level = 0 1: TX FIFO threshold level = 1 … … n: TX FIFO threshold level = n	R/W	0x3
11:10	DL[1:0]	Data Length 00: 8 bit 01: 16 bits 10: 24 bits 11: 32 bits	R/W	0x1
9	CLRRXFIFO	Clear I2S RX FIFO 0: No effect. 1: Reset RX FIFO (RXFIFOLV bit becomes 0, RXFIFOEMPTY bit becomes 1, Data in RX FIFO will be cleared). This bit returns “0” automatically	W	0
8	CLRTXFIFO	Clear I2S TX FIFO 0: No effect. 1: Reset TX FIFO (TXFIFOLV bit becomes 0, TXFIFOEMPTY bit becomes 1, Data in TX FIFO will be cleared). This bit returns “0” automatically	W	0
7	RXEN	Receiver enable bit 0: Disable 1: Enable	R/W	0
6	TXEN	Transmit enable bit 0: Disable 1: Enable	R/W	0

5:4	FORMAT[1:0]	I2S operation format. 00: Standard I2S format 01: Left-justified format 10: Right(MSB)-justified format 11: Reserved	R/W	0
3	MS	Master/Slave selection bit 0: Act as Master using internally generated BCLK and WS signals. 1: Act as Slave using externally BCLK and WS signals.	R/W	0
2	MONO	Mono/Stereo selection bit 0: Stereo 1: Mono	R/W	0
1	MUTE	Mute enable bit 0: Disable Mute 1: Enable. I2SSDA Output = 0	R/W	0
0	START	Start Transmit/Receive bit. 0: Disable 1: Start Transmit/Receive	R/W	0

16.6.2 I2S n Clock register (I2Sn_CLK) (n=0,1)

Address Offset: 0x04

Bit	Name	Description	Attribute	Reset
31:17	Reserved		R	0
16	CLKSEL	I2S clock source selection 0: HCLK 1: EHS XTAL	R/W	0
15:8	BCLKDIV[7:0]	BCLK divider 0: BCLK = MCLK / 2 1: BCLK = MCLK / 4 2: BCLK = MCLK / 6 3: BCLK = MCLK / 8 … … n: BCLK = MCLK / (2*n +2)	R/W	1
7:5	Reserved		R	0
4	MCLKSEL	MCLK source selection bit 0: MCLK source of master is from I2S_PCLK 1: MCLK source of master is from GPIO	R/W	0
3	MCLKOEN	MCLK output enable bit 0: Disable 1: Enable	R/W	0
2:0	MCLKDIV[2:0]	MCLK divider 0: MCLK = MCLK source 1: MCLK = MCLK source / 2 2: MCLK = MCLK source / 4 … … n: MCLK = MCLK source / (2*n), n>0	R/W	0

16.6.3 I2S n Status register (I2Sn_STATUS) (n=0,1)

Address Offset: 0x08

Bit	Name	Description	Attribute	Reset
31:21	Reserved		R	0
20:17	RXFIFOLV[3:0]	RX FIFO used level 0000: 0/8 RX FIFO is used (Empty) 0001: 1/8 RX FIFO is used 0010: 2/8 RX FIFO is used	R	0

		… … 1000: 8/8 RX FIFO is used (Full) Other: Reserved		
16	Reserved		R	0
15:12	TXFIFOLV[3:0]	TX FIFO used level 0000: 0/8 TX FIFO is used (Empty) 0001: 1/8 TX FIFO is used 0010: 2/8 TX FIFO is used … … 1000: 8/8 TX FIFO is used (Full) Other: Reserved	R	0
11	RXFIFOEMPTY	RX FIFO empty flag 0: RX FIFO is not empty. 1: RX FIFO is empty. Data read from RX FIFO will be zero.	R	1
10	TXFIFOEMPTY	TX FIFO empty flag 0: TX FIFO is not empty. 1: TX FIFO is empty.	R	1
9	RXFIFOFULL	RX FIFO full flag 0: RX FIFO is not full. 1: RX FIFO is full.	R	0
8	TXFIFOFULL	TX FIFO full flag 0: TX FIFO is not full. 1: TX FIFO is full. Write operation to TX FIFO will be ignored.	R	0
7	RXFIFOTHF	RX FIFO threshold flag 0: RXFIFOLV ≦ RXFIFOTH 1: RXFIFOLV > RXFIFOTH	R	0
6	TXFIFOTHF	TX FIFO threshold flag 0: TXFIFOLV ≧ TXFIFOTH 1: TXFIFOLV < TXFIFOTH	R	1
5:2	Reserved		R	0
1	RIGHTCH	Current channel status 0: Current channel is Left channel 1: Current channel is Right channel	R	1
0	I2SINT	I2S interrupt flag 0: No I2S interrupt 1: I2S interrupt occurs.	R	0

16.6.4 I2S n Interrupt Enable register (I2S_IE) (n=0,1)

Address Offset: 0x0C

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7	RXFIFOTHIEN	RX FIFO threshold interrupt enable bit 0: Disable 1: Enable	R/W	0
6	TXFIFOTHIEN	TX FIFO threshold interrupt enable bit 0: Disable 1: Enable	R/W	0
5	RXFIFOUDFIEN	RX FIFO underflow interrupt enable bit 0: Disable 1: Enable	R/W	0
4	TXFIFOOVFIEN	TX FIFO overflow interrupt enable bit 0: Disable 1: Enable	R/W	0
3:0	Reserved		R	0

16.6.5 I2S n Raw Interrupt Status register (I2S_RIS) (n=0,1)

Address Offset: 0x10

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7	RXFIFOTHIF	RX FIFO threshold interrupt flag 0: No RX FIFO threshold interrupt 1: RX FIFO threshold triggered.	R	0
6	TXFIFOTHIF	TX FIFO threshold interrupt flag 0: No TX FIFO threshold interrupt 1: TX FIFO threshold triggered.	R	0
5	RXFIFOUDIF	RX FIFO underflow interrupt flag 0: No RX FIFO underflow 1: RX FIFO underflow (RX FIFO is empty and still being read).	R	0
4	TXFIFOOVIF	TX FIFO overflow interrupt flag 0: No TX FIFO overflow 1: TX FIFO overflow (TX FIFO is full and still being written).	R	0
3:0	Reserved		R	0

16.6.6 I2S n Interrupt Clear register (I2S_IC) (n=0,1)

Address Offset: 0x14

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7	RXFIFOTHIC	0: No effect 1: Clear RXFIFOTHIF bit	W	0
6	TXFIFOTHIC	0: No effect 1: Clear TXFIFOTHIF bit	W	0
5	RXFIFOUDIC	0: No effect 1: Clear RXFIFOOUDIF bit	W	0
4	TXFIFOOVIC	0: No effect 1: Clear TXFIFOOVIF bit	W	0
3:0	Reserved		R	0

16.6.7 I2S n RXFIFO register (I2S_RXFIFO) (n=0,1)

Address Offset: 0x18

Bit	Name	Description	Attribute	Reset
31:0	RXFIFO[31:0]	8 x 32-bit RX FIFO	R/W	0

16.6.8 I2S n TXFIFO register (I2S_TXFIFO) (n=0,1)

Address Offset: 0x1C

Bit	Name	Description	Attribute	Reset
31:0	TXFIFO[31:0]	8 x 32-bit TX FIFO	R/W	0

17 4x40/6x38/7x37/8x36 LCD DRIVER

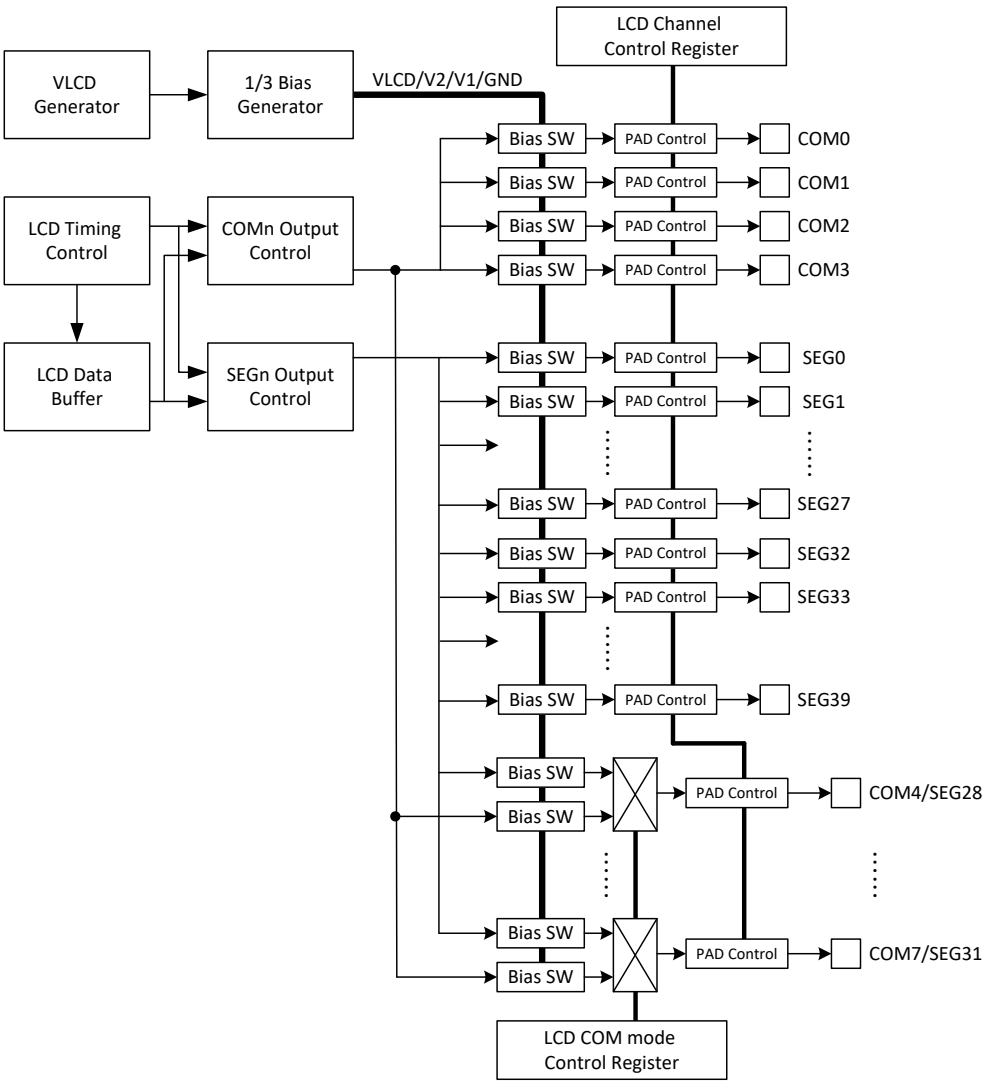
17.1 OVERVIEW

The MCU builds in R type structures with 4x40 or 6x38 or 7x37 or 8x36 dots. The LCD scan timing can support 1/4 duty, 1/6 duty, 1/7 duty, and 1/8 duty. Besides, 1/3 bias structure is also supported. Of these pins, all common and segment pins are shared with GPIO, and can be selected by programming LCD_CTRL register. R type is using internal or external bias circuit to adjust LCD power and bias voltage.

The LCD driver supports a static mode controlled by LSTC control bit. If LSTC=0, the LCD driver is 1/3 bias, 1/4(or 1/6, 1/7, 1/8) duty LCD mode. If LSTC=1, the LCD driver is selected to static mode.

The LCD has two clock source and four clock rates to decide LCD frame rate from 15.625Hz to 256Hz. The clock source is from internal 32KHz RC or external 32.768kHz oscillator crystal or RC type and controlled by LCDCKS bit.

In LCD mode, the LCD builds in one internal bias circuit to adjust LCD power and bias voltage. There are 40-pin GPIO shared with COM pins and SEG pins which controlled by LCD_SEGSEL1 and LCD_SEGSEL2 registers and LCDCOM[1:0] bits. After setup LCDEN bit, the LCD starts to output analog data. In static mode, the selected COM/SEG pins switch to be GPIO output mode and only output 0V and VDD voltage.
After LCD operating, the system would be waked up from deep sleep mode to normal mode if the LCD interrupt is enabled.



17.2 FEATURES

1. Support R/C-type
2. Support up to 288 (8 x 36) dots
3. Common 0~7 and Segment 0~39 are all shared with GPI/O pins, and unused segment and common pins can be used as GPIO pins.
4. Support 1/3 bias voltage
5. Support 1/4 duty, 1/6 duty, 1/7 duty, and 1/8 duty
6. Configurable frame frequency
7. Embedded LCD bias reference ladder
8. Blinking capability
9. LCD frame interrupt

17.3 PIN DESCRIPTION

Pin Name	Type	Description	GPIO Configuration
SEGx	O	LCD driver segment pins	
COMx	O	LCD driver common pins	

17.4 LCD CHANNEL CONTROL

The LCD includes 4-COM pins, 40-SEG pins and 4-COM/SEG share pins. Each of the LCD channels is shared with GPIO. If the LCD driver is enabled (LCDEN=1), the 4-COM pins are controlled to LCD COM pin mode, but the 40-SEG pins are controlled by SEGSEL1 and SEGSEL2 registers.

The COM/SEG share pin will follow the mode selection, to switch the COM or SEG functions. When the COM mode is selected, the pin will switch to common function, and the segment function will be ignored. Conversely, the segment function is enabled according to the segment control bit setting.

Each of the LCD channels has a bias switch circuit to select a bias voltage for COM or SEG driving waveform. The bias voltage is from the LCD bias generator. The bias switch is controlled by LCD COM and SEG output control.

In LCD static mode, the bias switch of COM and SEG pins is disabled. The selected COM and SEG pins switch to be GPIO output mode and only output 0V and VDD voltage. The LCD COM and SEG output control circuits control the GPIO output latch of COM and SEG pins directly.

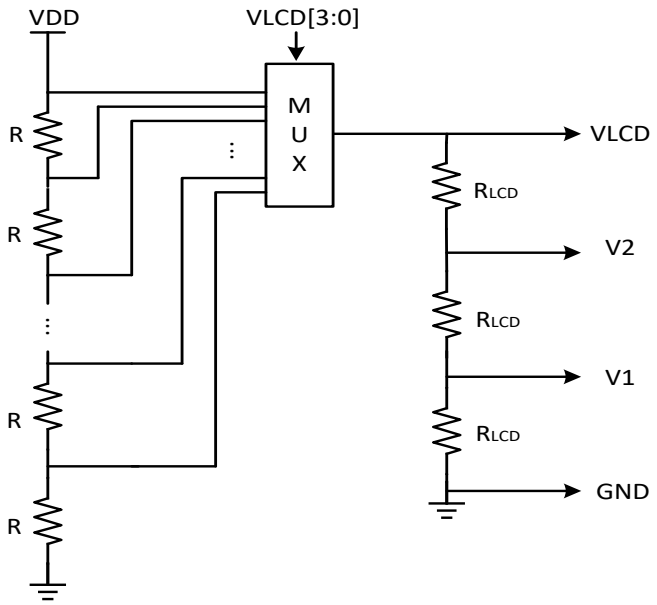
<table>
<tr><th rowspan="2">LCDEN</th><th rowspan="2">COM mode</th><th>LCD COM</th><th colspan="5">LCD SEG</th><th colspan="4">LCD COM/SEG share</th></tr>
<tr><th>COM0~COM3</th><th>SEG0</th><th>SEG1</th><th>…</th><th>SEG30</th><th>SEG31</th><th>SEG31/ COM7</th><th>SEG30/ COM6</th><th>SEG29/ COM5</th><th>SEG28/ COM4</th></tr>
<tr><td>0</td><td>X</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td></tr>
<tr><td rowspan="4">1</td><td>4</td><td rowspan="4">COM</td><td colspan="6" rowspan="4">Control by SEGSEL1[31:0]</td><td rowspan="3">Control by SEGSEL1[31]</td><td rowspan="2">Control by SEGSEL1[30]</td><td>Control by SEGSEL1[29]</td><td>Control by SEGSEL1[28]</td></tr>
<tr><td>6</td><td rowspan="3">COM5</td><td rowspan="3">COM4</td></tr>
<tr><td>7</td><td rowspan="2">COM6</td></tr>
<tr><td>8</td><td>COM7</td></tr>
</table>

When LCDIDLE bit is set, If the LCD driver is disabled (LCDEN=0), all COM pins are controlled to V1 or VDD by LSTC bit.

LCDEN	LSTC	LCDIDLE	COMn pin	SEGn pin	
				SEGn enable	COM share
0	0	0	GPIO	GPIO	GPIO
0	0	1	V1	GPIO	V1
0	1	0	GPIO	GPIO	GPIO
0	1	1	VDD	GPIO	VDD
1	0	N/A	LCD COM	LCD SEG	LCD COM
1	1	N/A	LED COM	LED SEG	LED COM

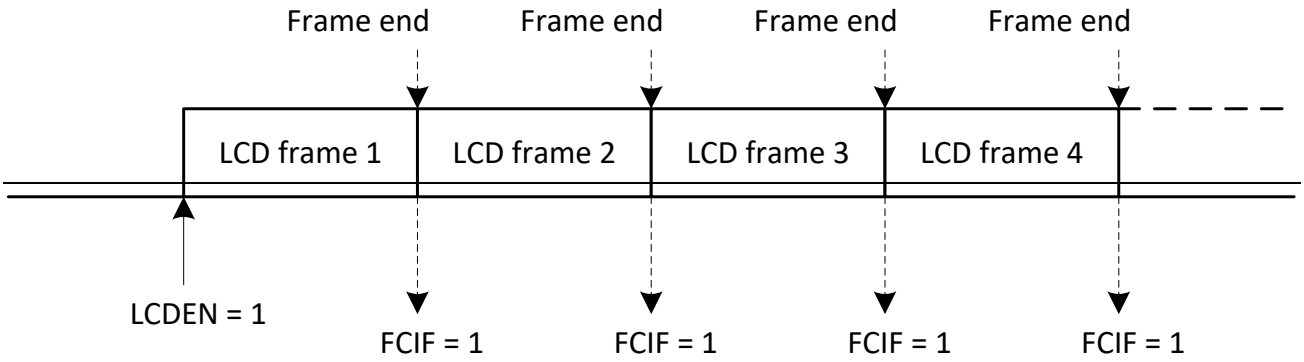
17.5 LCD BIAS GENERATOR

The LCD bias generator include LCD contrast control and 1/3 bias control. The LCD contrast control is used to set the voltage of VLCD. There are 16-stage VLCD voltage from VDD to VDD*0.5 and is controlled by VLCD[3:0] bits. The 1/3 bias control circuit has three resistances (R_{LCD}) for difference VLCD controlled by LCDBIA[2:0] bits. The R_{LCD} is from 17.65KΩ to 300KΩ. The final 4-level LCD bias voltage source is VLCD/V2/V1/GND and supply to LCD COM and SEG pins. When the static mode is active (LSTC=1), both LCD contrast control and 1/3 bias control will be turned off.



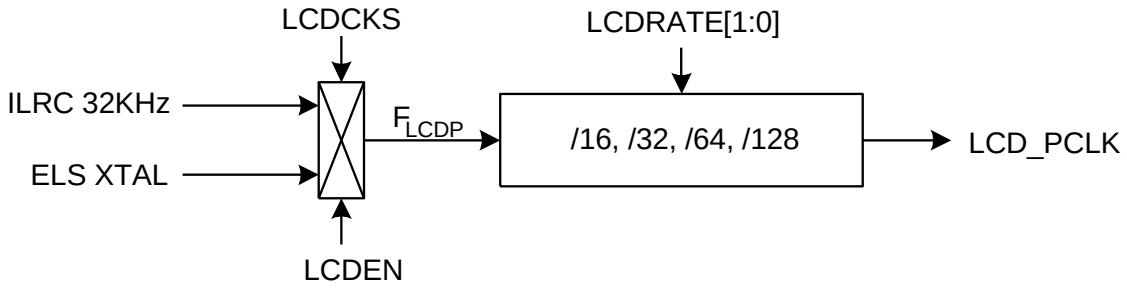
17.6 LCD INTERRUPT

The FCIF bit will be set after one LCD frame finishes and will triggers LCD interrupt when FCIE = 1.



17.7 LCD TIMING CONTROL

The LCD timing control generates the clock for LCD frame rate. The LCD has two clock sources (flcdp): internal 16KHz RC and external 32.768KHz crystal, controlled by LCDCKS bit. There are 4-level pre-scaler to divide the flcdp to obtain LCD frame clock source F_{LCD}. Each LCD frame length is 2*COM mode*F_{LCD}. (COM mode = 4 ~ 8)

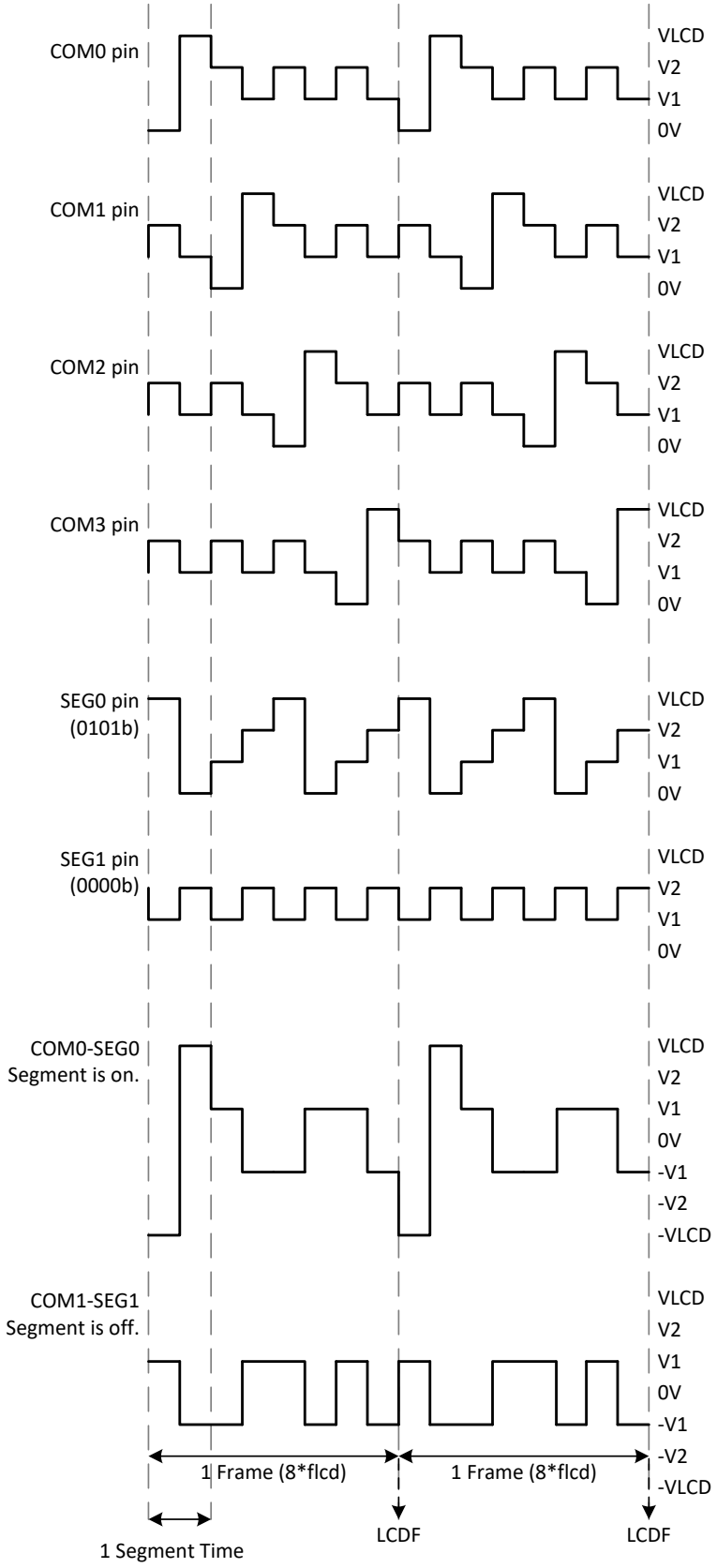


LCD Clock Rate (Hz) = LCD_PCLK	LCDRATE[1:0]			
	00 (/16)	01 (/32)	10 (/64)	11 (/128)
ILRC 32000Hz	2000	1000	500	250
ELS XTAL 32768Hz	2048	1024	512	256

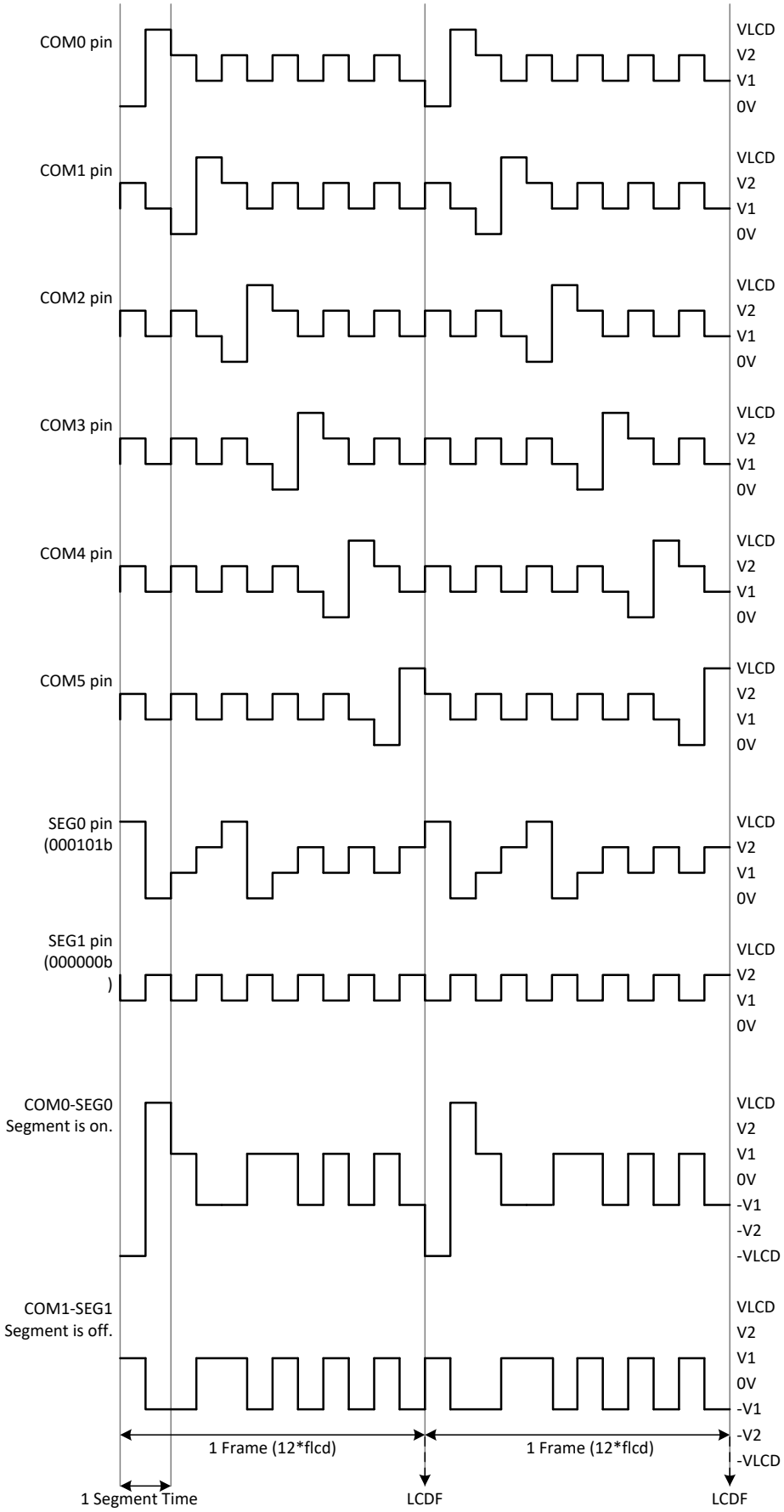
LCD Frame rate (Hz)		LCDRATE[1:0]			
		00 (/16)	01 (/32)	10 (/64)	11 (/128)
ILRC 32000Hz	4 COM mode	250 Hz	125 Hz	62.5 Hz	31.25 Hz
ELS XTAL 32768Hz		256 Hz	128 Hz	64 Hz	32 Hz
ILRC 32000Hz	6 COM mode	166.667 Hz	83.333 Hz	41.667 Hz	20.833 Hz
ELS XTAL 32768Hz		170.667 Hz	85.333 Hz	42.667 Hz	21.333 Hz
ILRC 32000Hz	7 COM mode	142.857 Hz	71.429 Hz	35.714 Hz	17.857 Hz
ELS XTAL 32768Hz		146.286 Hz	73.143 Hz	36.571 Hz	18.286 Hz
ILRC 32000Hz	8 COM mode	125 Hz	62.5 Hz	31.25 Hz	15.625 Hz
ELS XTAL 32768Hz		128 Hz	64 Hz	32 Hz	16 Hz

17.8 LCD WAVEFORM

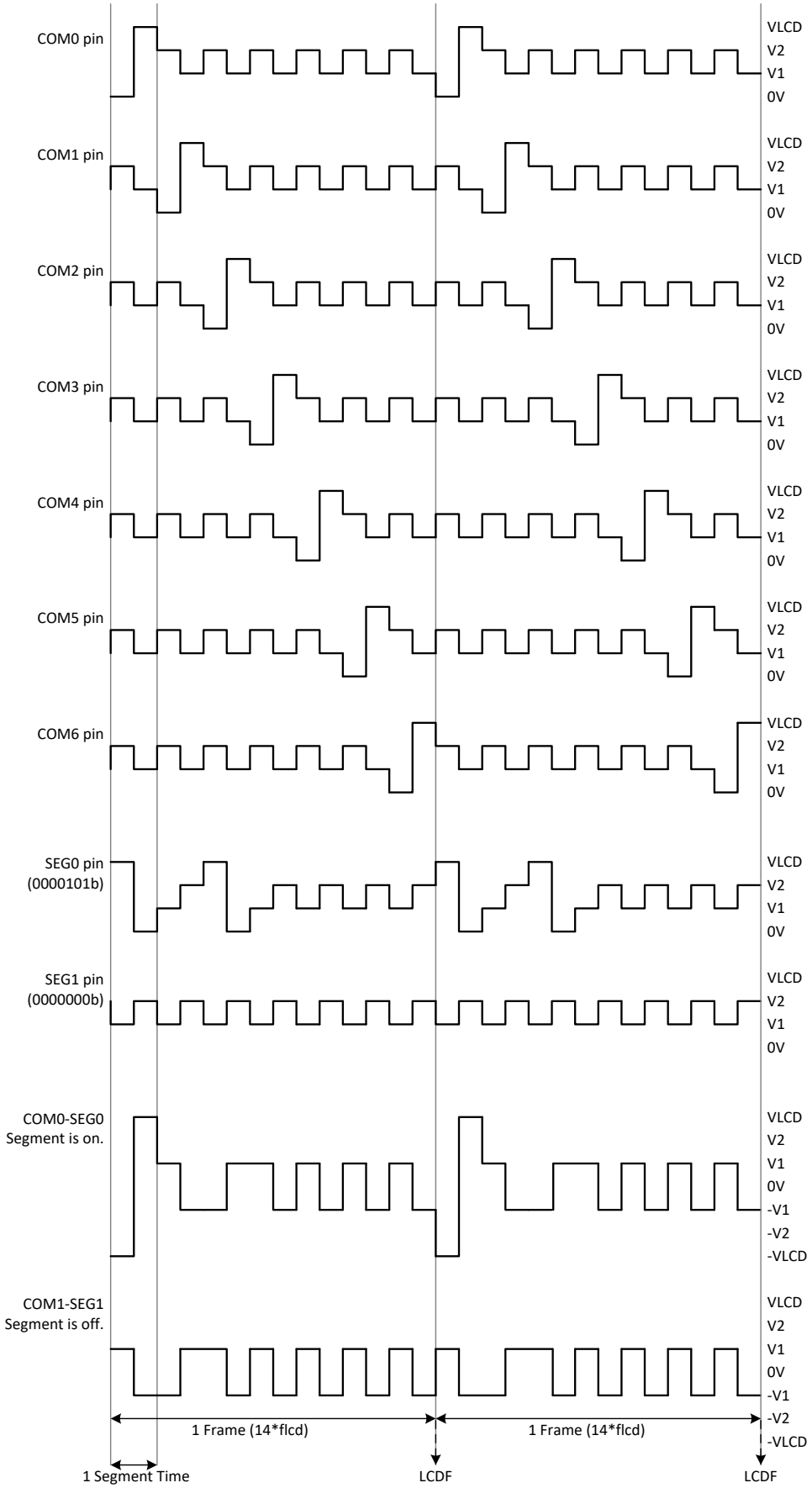
Waveform in LCD mode with 4 COM mode:



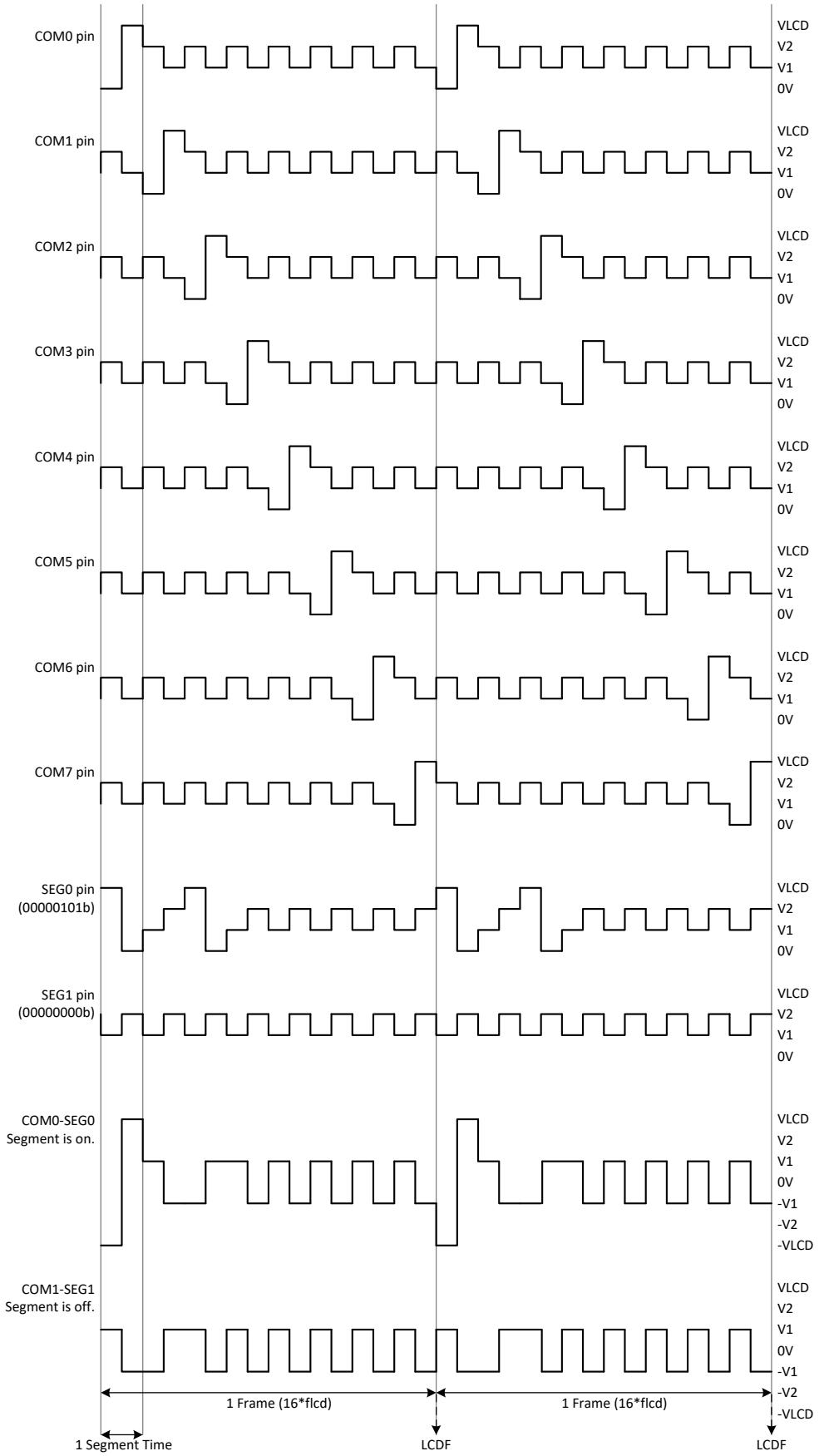
Waveform in LCD mode with 6 COM mode:



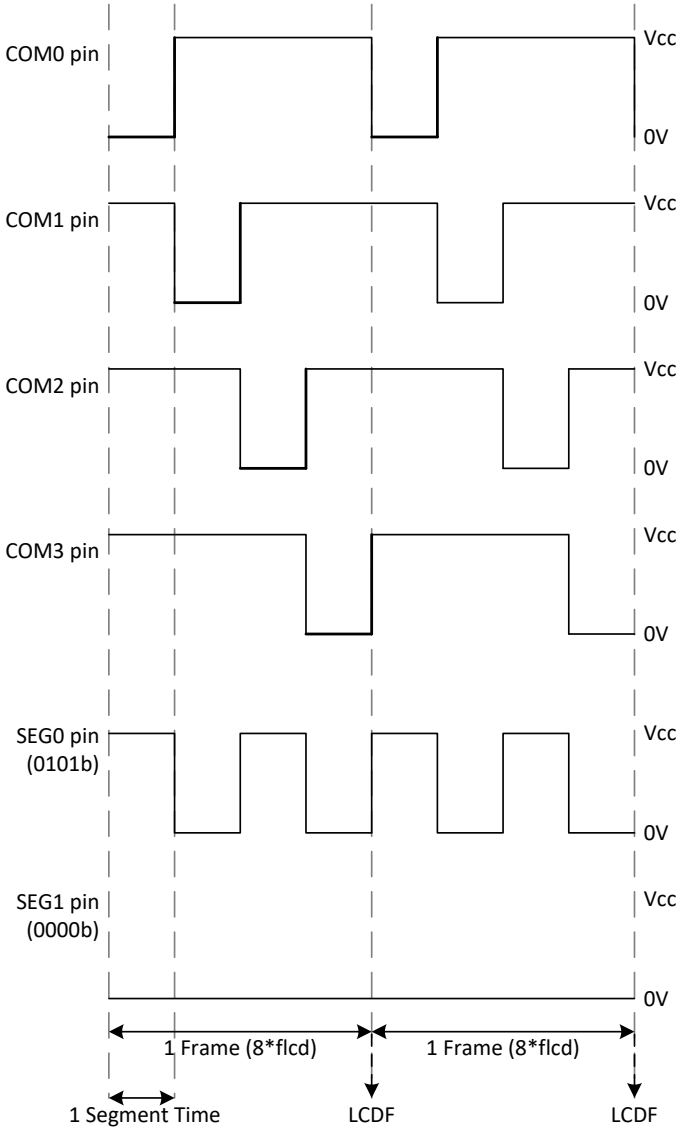
Waveform in LCD mode with 7 COM mode:



Waveform in LCD mode with 8 COM mode:

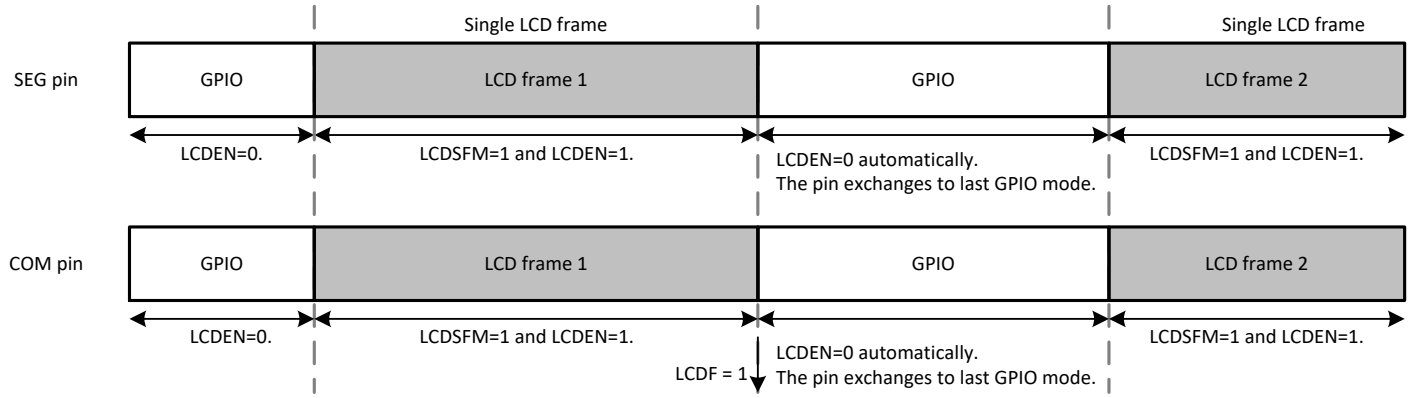


Waveform in static mode with 4 COM mode:



17.9 SINGLE LCD FRAME FUNCTION

When LCDSFM = 0, LCD frame will continuously output until LCD is disabled. When LCDSFM = 1 and LCDEN = 1, LCD will output single LCD frame and the FCIF is issued as LCD frame finished. LCDEN bit is cleared automatically and LCD pin returns to GPIO mode (or idle status by LCDIDLE bit). To output next frame is to set LCDEN bit by program again.



✸ ***Note: If LCDIDLE =1, the COM pins will be controlled to Idle status when LCDEN=0, the Idle status is V1 or VDD controlled by LSTC bit.***

17.10 LCD DISPLAY MEMORY MAP

Bit	SEGM9	SEGM8	SEGM7	SEGM6	SEGM5	SEGM4	SEGM3	SEGM2	SEGM1	SEGM0	
31	SEG39	SEG35	SEG31	SEG27	SEG23	SEG19	SEG15	SEG11	SEG7	SEG3	COM7
30											COM6
29											COM5
28											COM4
27											COM3
26											COM2
25											COM1
24											COM0
23	SEG38	SEG34	SEG30	SEG26	SEG22	SEG18	SEG14	SEG10	SEG6	SEG2	COM7
22											COM6
21											COM5
20											COM4
19											COM3
18											COM2
17											COM1
16											COM0
15	SEG37	SEG33	SEG29	SEG25	SEG21	SEG17	SEG13	SEG9	SEG5	SEG1	COM7
14											COM6
13											COM5
12											COM4
11											COM3
10											COM2
9											COM1
8											COM0
7	SEG36	SEG32	SEG28	SEG24	SEG20	SEG16	SEG12	SEG8	SEG4	SEG0	COM7
6											COM6
5											COM5
4											COM4
3											COM3
2											COM2
1											COM1
0											COM0

17.11 LCD REGISTERS

Base Address: 0x4003 4000

17.11.1 LCD Control register (LCD_CTRL)

Address Offset: 0x00

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th><th>Attribute</th><th>Reset</th></tr>
<tr><td>31:17</td><td>Reserved</td><td></td><td>R/W</td><td>0</td></tr>
<tr><td>16:14</td><td>LCDBIA[2:0]</td><td>LCD bias resistance selection bit
<table>
<tr><th>LCDBIA[2:0]</th><th>Total Resistance (ohm)</th></tr>
<tr><td>000</td><td>Disable</td></tr>
<tr><td>001</td><td>75.00 K</td></tr>
<tr><td>010</td><td>225.00 K</td></tr>
<tr><td>011</td><td>56.25 K</td></tr>
<tr><td>100</td><td>900.00 K</td></tr>
<tr><td>101</td><td>69.23 K</td></tr>
<tr><td>110</td><td>180.00 K</td></tr>
<tr><td>111</td><td>52.94 K</td></tr>
</table></td><td>R/W</td><td>0</td></tr>
<tr><td>13:12</td><td>LCDRATE[1:0]</td><td>LCD clock rate (LCD_PCLK)
00: LCD clock source / 16
01: LCD clock source / 32
10: LCD clock source / 64
11: LCD clock source / 128</td><td>R/W</td><td>0</td></tr>
<tr><td>11</td><td>LCDBNK</td><td>LCD blank control bit
0: Normal display
1: All LCD dots off.</td><td>R/W</td><td>0</td></tr>
<tr><td>10</td><td>LCDCKS</td><td>LCD clock source selection
0: ILRC
1: ELS XTAL</td><td>R/W</td><td>0</td></tr>
<tr><td>9:8</td><td>LCDCOM[1:0]</td><td>Duty selection
00: 1/4 duty → COM0, COM1, COM2, and COM3 organize 1 frame. HW will assign COM0~3 as LCD pins instead of GPIO automatically.
01: 1/6 duty → COM0, COM1, COM2, COM3, COM4, and COM5 organize 1 frame. HW will assign COM0~5 as LCD pins instead of GPIO automatically.
10: 1/7 duty → COM0, COM1, COM2, COM3, COM4, COM5, and COM6 organize 1 frame. HW will assign COM0~6 as LCD pins instead of GPIO automatically.
11: 1/8 duty → COM0, COM1, COM2, COM3, COM4, COM5, COM6, and COM7 organize 1 frame. HW will assign COM0~7 as LCD pins instead of GPIO automatically.</td><td>R/W</td><td>00b</td></tr>
<tr><td>7</td><td>LSTC</td><td>LCD static mode control bit.
0: LCD driver is 1/3 bias (1/4, 1/6, 1/7, 1/8 duty by LCDCOM bits).
1: LCD driver is static mode.</td><td>R/W</td><td>0</td></tr>
</table>

		<table><tr><th rowspan="2">LCDEN</th><th rowspan="2">LSTC</th><th rowspan="2">LCDIDLE</th><th rowspan="2">COMn pin</th><th colspan="2">SEGn pin</th></tr><tr><th>SEGn enable</th><th>COM share</th></tr><tr><td>0</td><td>0</td><td>0</td><td>GPIO</td><td>GPIO</td><td>GPIO</td></tr><tr><td>0</td><td>0</td><td>1</td><td>V1</td><td>GPIO</td><td>V1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>GPIO</td><td>GPIO</td><td>GPIO</td></tr><tr><td>0</td><td>1</td><td>1</td><td>VDD</td><td>GPIO</td><td>VDD</td></tr><tr><td>1</td><td>0</td><td>N/A</td><td>LCD COM</td><td>LCD SEG</td><td>LCD COM</td></tr><tr><td>1</td><td>1</td><td>N/A</td><td>LED COM</td><td>LED SEG</td><td>LED COM</td></tr></table>		
6	LCDSFM	LCD single frame function control bit. 0: Disable 1: Enable	R/W	0
5	LCDIDLE	LCD idle state enable bit. (Required when sharing with TK, ONLY available when LCDENB=0) 0: Disable (When LCD is disabled, COM0~7 pins are GPIO.) 1: Enable (When LCD is disabled, COM0~7 pins which are used are V1 or VDD depends on LSTC bit. SEG0~SEG39 are GPIO)	R/W	0
4:1	VLCD[3:0]	VLCD adjustment 0000: VLCD = VCC 0001: VLCD = 0.97*VCC 0010: VLCD = 0.93*VCC 0011: VLCD = 0.90*VCC 0100: VLCD = 0.87*VCC 0101: VLCD = 0.83*VCC 0110: VLCD = 0.80*VCC 0111: VLCD = 0.77*VCC 1000: VLCD = 0.73*VCC 1001: VLCD = 0.70*VCC 1010: VLCD = 0.67*VCC 1011: VLCD = 0.63*VCC 1100: VLCD = 0.60*VCC 1101: VLCD = 0.57*VCC 1110: VLCD = 0.53*VCC 1111: VLCD = 0.50*VCC	R/W	0
0	LCDENB	LCD driver enable bit. 0: Disable 1: Enable.	R/W	0

17.11.2 LCD Frame Counter Control register (LCD_FCC)

Address Offset: 0x04

The frame counter (FC) will start to count up from 0x0 when FCENB = 1, and add 1 when a frame is updated. When the counter value reaches FCT[5:0], FC will reset as 0x0 by HW, the LCD frame interrupt flag will become 1. If LCD frame interrupt is enabled (FCIE =1), the LCD frame interrupt is generated and sent to the interrupt controller.

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7	FCIE	LCD frame interrupt enable bit 0: Disable 1: Enable	R/W	0
6:1	FCT[5:0]	LCD frame counter threshold value	R/W	00001b
0	FCENB	LCD frame counter enable bit 0: Disable 1: Enable	R/W	0

17.11.3 LCD Raw Interrupt Status register (LCD_RIS)

Address offset: 0x08

Bit	Name	Description	Attribute	Reset
31:1	Reserved		R	0
0	FCIF	LCD frame interrupt flag. 0: Read→No interrupt Write→Write "0" to clear this bit and reset the interrupt if FCIE=1. 1: FC interrupt requirements met.	R/W	0

17.11.4 LCD SEG Select register (LCD_SEGSEL1)

Address offset: 0x0C

Bit	Name	Description	Attribute	Reset
31:0	SEGxEN[31:0]	SEGx enable bit (x=0~31) 0: Disable SEGx 1: Enable SEGx	R/W	0

17.11.5 LCD SEG Select register (LCD_SEGSEL2)

Address offset: 0x10

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7	SEG39EN	SEG39 enable bit 0: Disable SEG39 1: Enable SEG39	R/W	0
6	SEG38EN	SEG38 enable bit 0: Disable SEG38 1: Enable SEG38	R/W	0
5	SEG37EN	SEG37 enable bit 0: Disable SEG37 1: Enable SEG37	R/W	0
4	SEG36EN	SEG36 enable bit 0: Disable SEG36 1: Enable SEG36	R/W	0
3	SEG35EN	SEG35 enable bit 0: Disable SEG35 1: Enable SEG35	R/W	0
2	SEG34EN	SEG34 enable bit 0: Disable SEG34 1: Enable SEG34	R/W	0
1	SEG33EN	SEG33 enable bit 0: Disable SEG33 1: Enable SEG33	R/W	0
0	SEG32EN	SEG32 enable bit 0: Disable SEG32 1: Enable SEG32	R/W	0

17.11.6 LCD SEG Memory register 0 (LCD_SEGM0)

Address Offset: 0x14

Bit	Name	Description	Attribute	Reset
31:24	SEG3[7:0]	SEG3 data for COM0~COM7	R/W	0
23:16	SEG2[7:0]	SEG2 data for COM0~COM7	R/W	0
15:8	SEG1[7:0]	SEG1 data for COM0~COM7	R/W	0
7:0	SEG0[7:0]	SEG0 data for COM0~COM7	R/W	0

17.11.7 LCD SEG Memory register 1 (LCD_SEGM1)

Address Offset: 0x18

Bit	Name	Description	Attribute	Reset
31:24	SEG7[7:0]	SEG7 data for COM0~COM7	R/W	0
23:16	SEG6[7:0]	SEG6 data for COM0~COM7	R/W	0
15:8	SEG5[7:0]	SEG5 data for COM0~COM7	R/W	0
7:0	SEG4[7:0]	SEG4 data for COM0~COM7	R/W	0

17.11.8 LCD SEG Memory register 2 (LCD_SEGM2)

Address Offset: 0x1C

Bit	Name	Description	Attribute	Reset
31:24	SEG11[7:0]	SEG11 data for COM0~COM7	R/W	0
23:16	SEG10[7:0]	SEG10 data for COM0~COM7	R/W	0
15:8	SEG9[7:0]	SEG9 data for COM0~COM7	R/W	0
7:0	SEG8[7:0]	SEG8 data for COM0~COM7	R/W	0

17.11.9 LCD SEG Memory register 3 (LCD_SEGM3)

Address Offset: 0x20

Bit	Name	Description	Attribute	Reset
31:24	SEG15[7:0]	SEG15 data for COM0~COM7	R/W	0
23:16	SEG14[7:0]	SEG14 data for COM0~COM7	R/W	0
15:8	SEG13[7:0]	SEG13 data for COM0~COM7	R/W	0

7:0	SEG12[7:0]	SEG12 data for COM0~COM7	R/W	0

17.11.10 LCD SEG Memory register 3 (LCD_SEGM4)

Address Offset: 0x24

Bit	Name	Description	Attribute	Reset
31:24	SEG19[7:0]	SEG19 data for COM0~COM7	R/W	0
23:16	SEG18[7:0]	SEG18 data for COM0~COM7	R/W	0
15:8	SEG17[7:0]	SEG17 data for COM0~COM7	R/W	0
7:0	SEG16[7:0]	SEG16 data for COM0~COM7	R/W	0

17.11.11 LCD SEG Memory register 3 (LCD_SEGM5)

Address Offset: 0x28

Bit	Name	Description	Attribute	Reset
31:24	SEG23[7:0]	SEG23 data for COM0~COM7	R/W	0
23:16	SEG22[7:0]	SEG22 data for COM0~COM7	R/W	0
15:8	SEG21[7:0]	SEG21 data for COM0~COM7	R/W	0
7:0	SEG20[7:0]	SEG20 data for COM0~COM7	R/W	0

17.11.12 LCD SEG Memory register 3 (LCD_SEGM6)

Address Offset: 0x2C

Bit	Name	Description	Attribute	Reset
31:24	SEG27[7:0]	SEG27 data for COM0~COM7	R/W	0
23:16	SEG26[7:0]	SEG26 data for COM0~COM7	R/W	0
15:8	SEG25[7:0]	SEG25 data for COM0~COM7	R/W	0
7:0	SEG24[7:0]	SEG24 data for COM0~COM7	R/W	0

17.11.13 LCD SEG Memory register 3 (LCD_SEGM7)

Address Offset: 0x30

Bit	Name	Description	Attribute	Reset
31:24	SEG31[7:0]	SEG31 data for COM0~COM7	R/W	0

23:16	SEG30[7:0]	SEG30 data for COM0~COM7	R/W	0
15:8	SEG29[7:0]	SEG29 data for COM0~COM7	R/W	0
7:0	SEG28[7:0]	SEG28 data for COM0~COM7	R/W	0

17.11.14 LCD SEG Memory register 3 (LCD_SEGM8)

Address Offset: 0x34

Bit	Name	Description	Attribute	Reset
31:24	SEG35[7:0]	SEG35 data for COM0~COM7	R/W	0
23:16	SEG34[7:0]	SEG34 data for COM0~COM7	R/W	0
15:8	SEG33[7:0]	SEG33 data for COM0~COM7	R/W	0
7:0	SEG32[7:0]	SEG32 data for COM0~COM7	R/W	0

17.11.15 LCD SEG Memory register 3 (LCD_SEGM9)

Address Offset: 0x38

Bit	Name	Description	Attribute	Reset
31:24	SEG39[7:0]	SEG39 data for COM0~COM7	R/W	0
23:16	SEG38[7:0]	SEG38 data for COM0~COM7	R/W	0
15:8	SEG37[7:0]	SEG37 data for COM0~COM7	R/W	0
7:0	SEG36[7:0]	SEG36 data for COM0~COM7	R/W	0

18 EXTERNAL BUS INTERFACE (EBI)

18.1 OVERVIEW

The external bus interface (EBI) provides access to external parallel interface devices such as SRAM, Flash, and LCD modules. The interface is memory mapped into the internal address bus of the Cortex-M0. The data and address lines can be multiplexed to reduce the number of pins required to connect to external devices. The bus read/write timing can be adjusted to meet the timing specifications of the external devices.

The EBI only supports asynchronous 8 or 16-bit bus interfaces, and translates the internal AHB transactions into the external device protocol automatically. If the selected external memory is 16 or 8 bits width, then 32-bit wide transactions on the AHB are auto split into consecutive 16 or 8-bit accesses.

The EBI supports multiplexed and non-multiplexed addressing modes. The non-multiplexed addressing mode can be operated more efficiently and faster but it requires more pins. The multiplexed addressing modes are slower and require an external address latch device and a lower number of pins. The functionality of the 16 AD pins depends on what kind of the multiplexed addressing mode is used. They are used for both address and data in the multiplexed modes. However, for the non-multiplexed 8-bit address mode, both the address and data uses these 16 AD pins. If more address bits or data bits are needed, an external latch can be used to support up to 26-bit addresses or 16-bit data in the multiplexed addressing modes using only the 16 EBI AD pins. Furthermore, independent of the addressing mode, up to 26 non-multiplexed address lines can be enabled on the EBI_A pin connections.

18.2 FEATURES

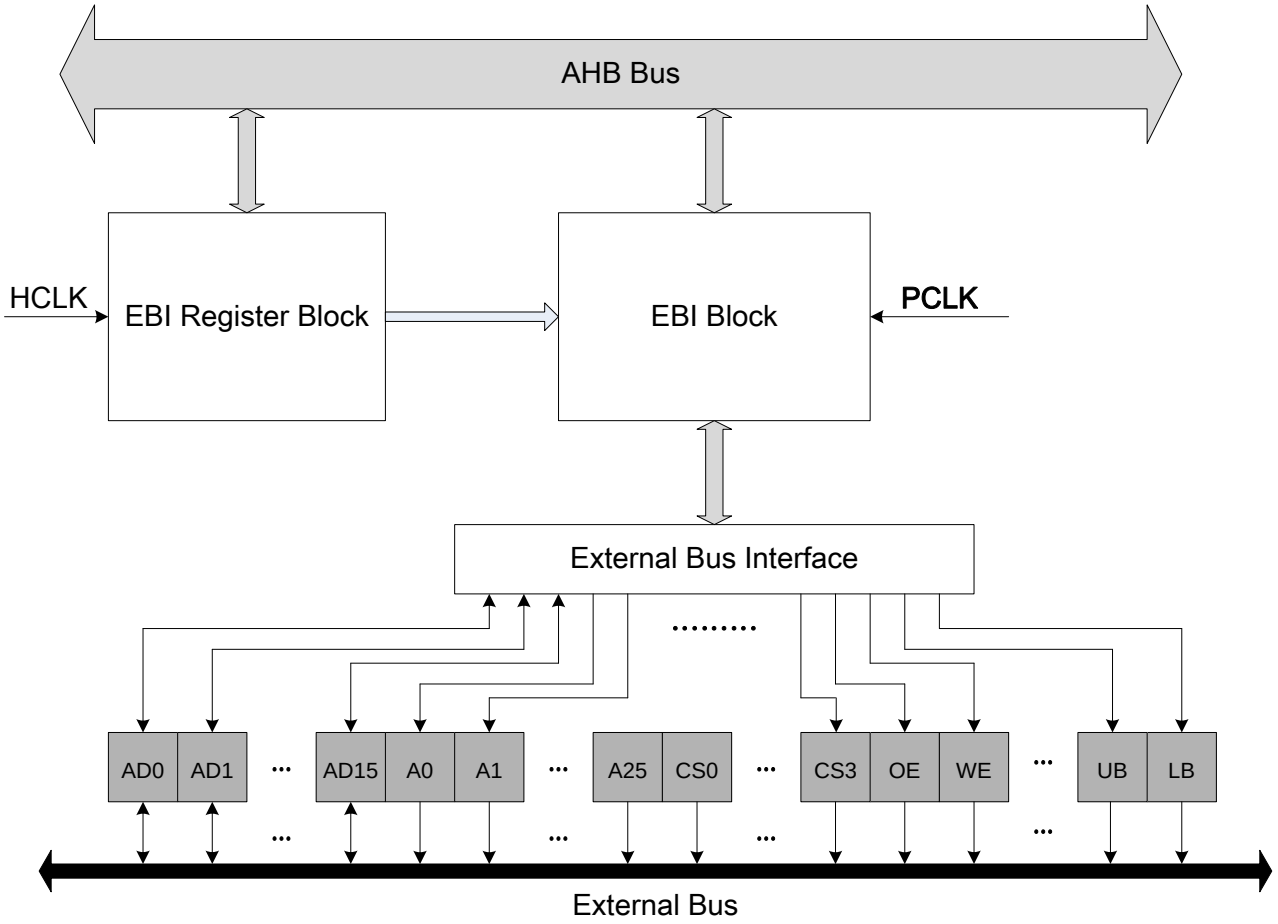
- Programmable interface for various memory types
    1. Asynchronous static random access memory – SRAM
    2. Read-only memory – ROM
    3. NOR Flash memory
    4. 8-bit or 16-bit parallel bus CPU interface device
- Translates AHB transactions into appropriate external device protocol
- 4 memory bank regions and independent chip select control for each memory bank
- Programmable timings to support a wide range of devices
    1. Programmable wait states or external asynchronous ready signal control
    2. Programmable bus turnaround cycles
    3. Programmable output enable and write enable cycles extension for each memory bank
    4. Individual active high or low setting of interface control signal for each memory bank
- Automatic translation when AHB transaction width and external memory interface width is different
- Supports multiplexed and non-multiplexed address and data line configurations
    1. Up to 26 address lines
    2. Up to 16-bit data bus width

18.3 PIN DESCRIPTION

Pin Name	Type	Description	GPIO Configuration
AD[15:0]	I/O	Addresses & Data	
A[25:0]	O	Addresses	
CS[3:0]	O	Chip select	
OE	O	Output enable	
WE	O	Write enable	

ALE	O	Addresses latch enable	
ARDY	I	Ready/Busy pin	Depends on GPIOn_CFG
UB	O	Upper byte enable	
LB	O	Lower byte enable	

18.4 BLOCK DIAGRAM

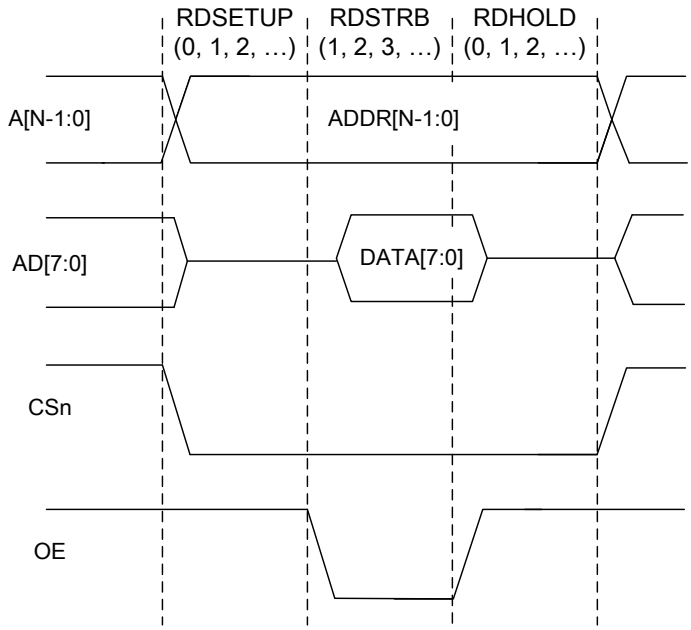


18.5 INTERFACE DESCRIPTION

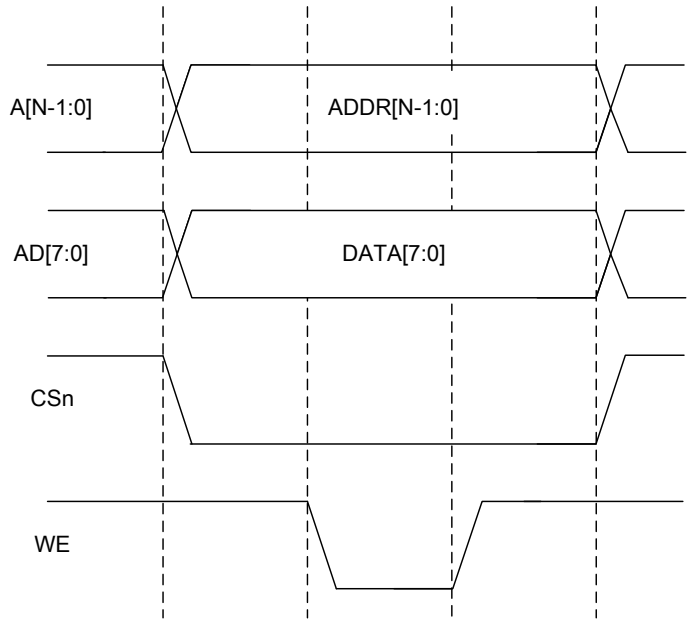
18.5.1 Non-multiplexed N-bit Address 8-bit Data Mode (A_ND8)

N-bit address and 8-bit data is supported. The address is located on the N bits of the A lines and the data uses the lower 8 bits AD lines. A1D8 Mode is also called 8080 8-bit mode.

- Read timing waveform in the A_ND8 mode:



- Write timing waveform in the A_ND8 mode:

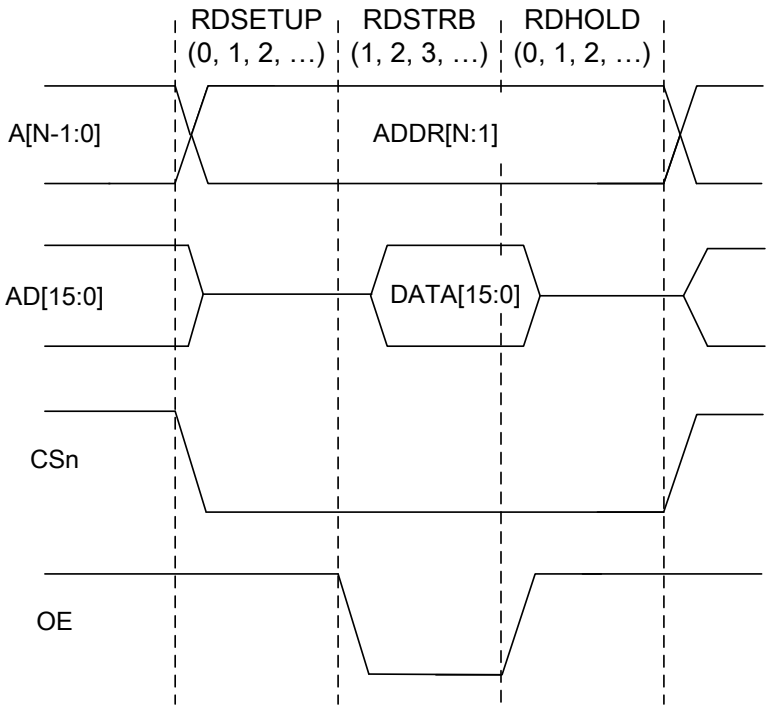


18.5.2 Non-multiplexed N-bit Address 16-bit Data Mode (A_ND16)

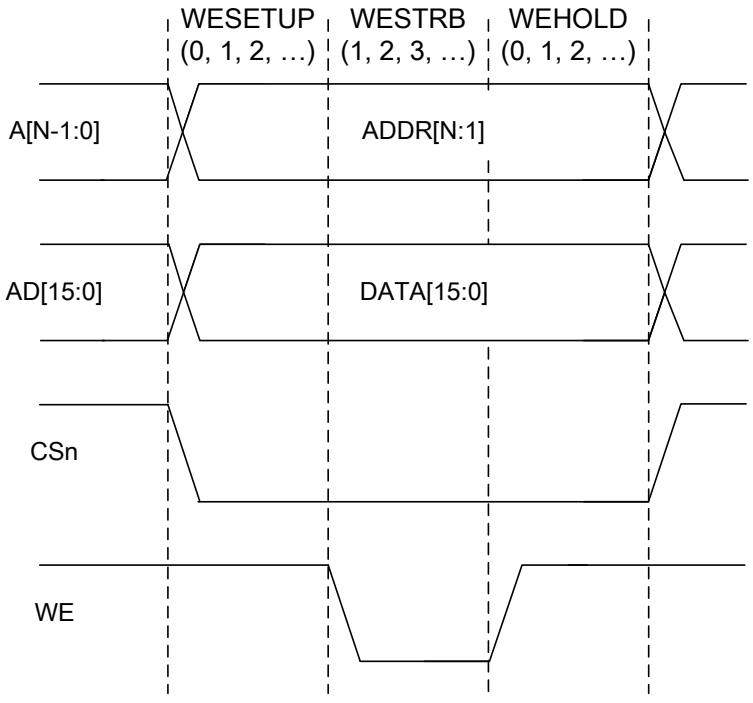
N-bit address and 16-bit data is supported, 16-bit data is located on the 16 AD lines. The addresses are located on the A lines. A1D16 Mode is also called 8080 16-bit mode.

Since the internal AHB address (HADDR) is a byte (8-bit) address whereas the 16-bit width of external device is addressed in words (16-bit), in case of a 16-bit external device width, the EBI will internally use HADDR[N:1] to generate the address EBI_A[N-1:0] for external device.

- Read timing waveform in the A_ND16 mode for the case in which N address lines on EBI_A have been enabled:



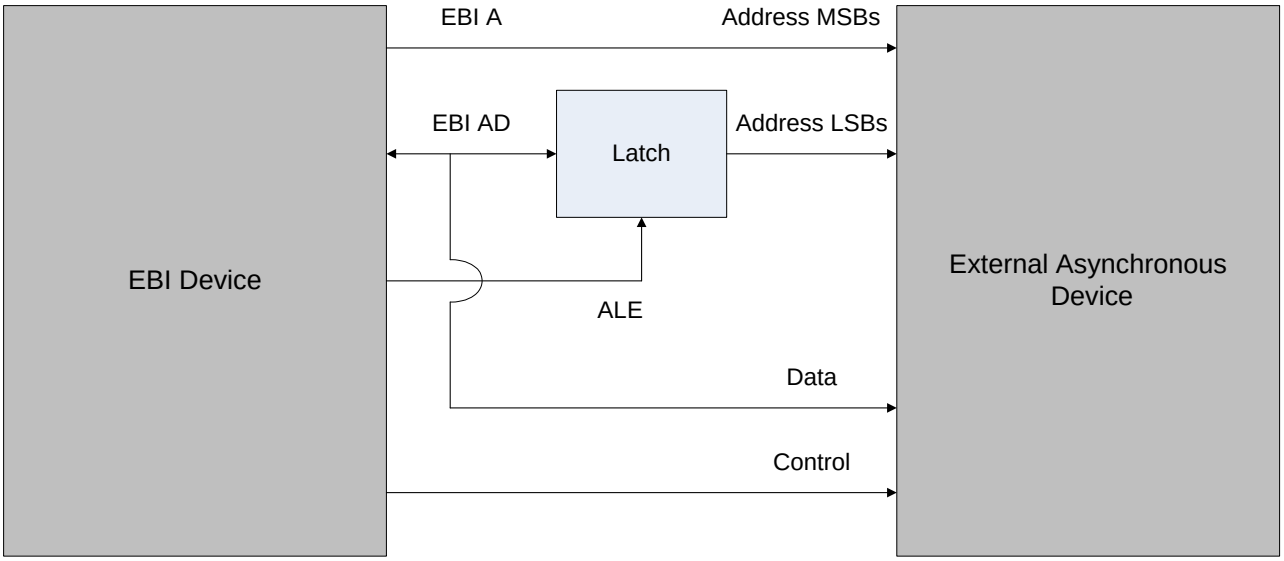
- Write timing waveform in the A_ND16 mode for the case in which N address lines on EBI_A have been enabled:



18.5.3 Multiplexed N-bit Address 16-bit Data Mode (A_ND16ALE)

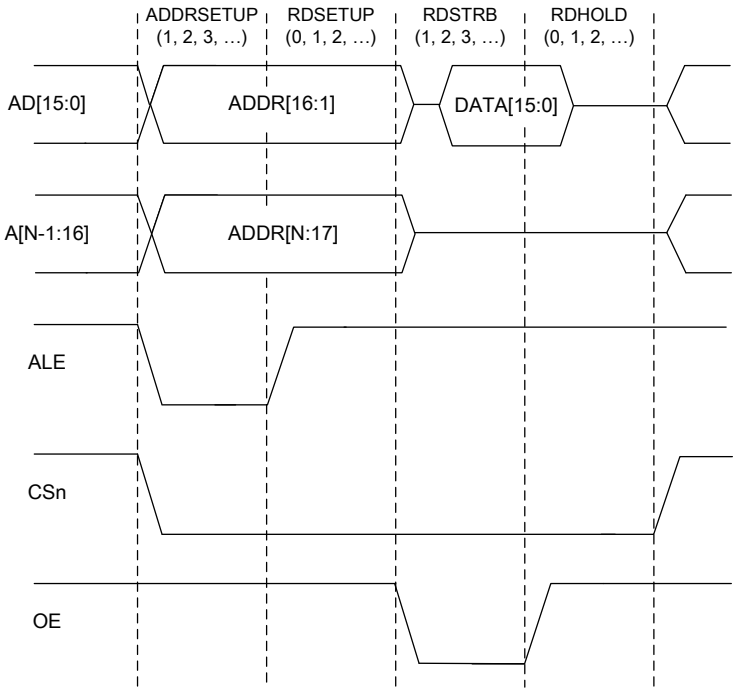
N-bit address and 16-bit data is supported, but an external latch is needed and an extra signal ALE is required to control the latch. The N-bit address and 16-bit data bits are multiplexed on the AD and A pins.

An EBI address latch setup diagram is shown as below:

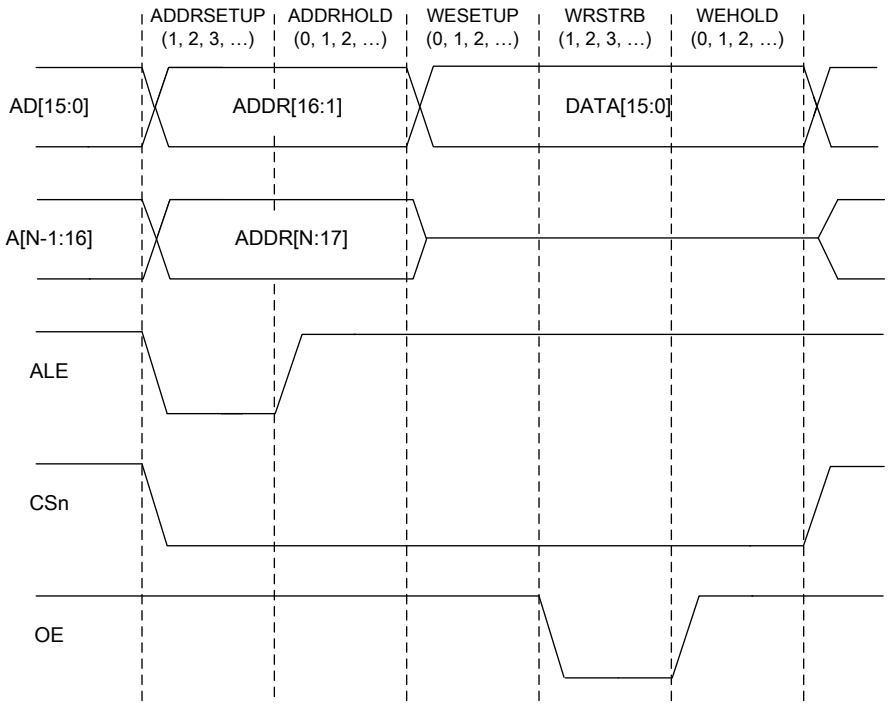


At the start of the transaction the address is output on the AD and A lines. The external address latch is controlled by the ALE signal and stores the address. Then the data is read or written according to operation.

- Read timing waveform in the A_ND16ALE mode:



- Write timing waveform in the ANd16ALE mode:



18.5.4 Write Buffer and EBI Status

The EBI has a 32-bit wide write buffer. The write buffer can be used to limit stalling of an AHB write burst transaction which comes from the Cortex-M0 to a potentially slow external device.

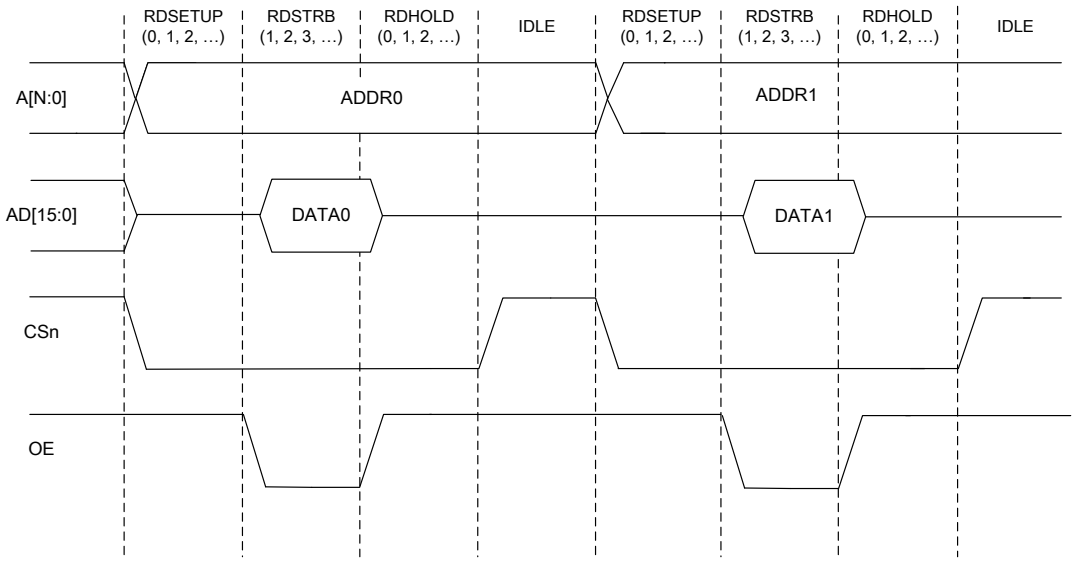
The EBIBUSY status bit in the EBI_STATUS register indicates whether an AHB transaction is still active in the EBI or not. When performing an AHB read or write, the EBIBUSY bit stays 1 until the required transaction(s) with the external device has finished.

18.5.5 Bus Turn-around and Idle Cycles

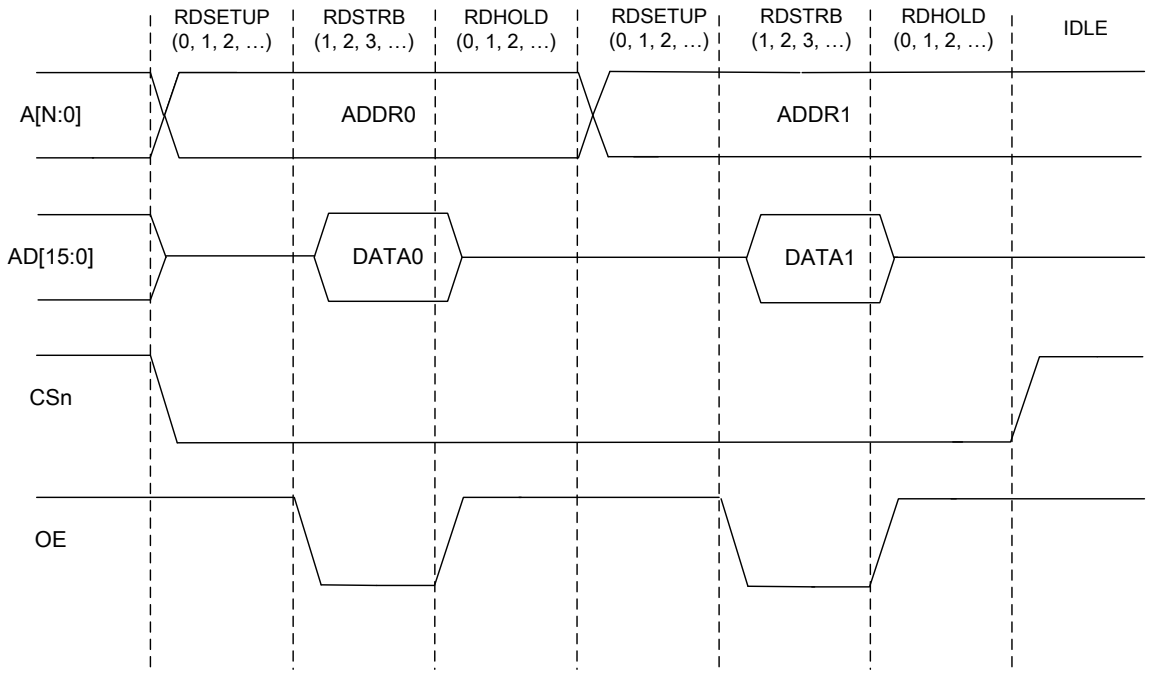
The EBI_AD lines can be driven by either the EBI or the external device depending on the cycle state of EBI bus. The RDHOLD timing parameter is for the bus turn-around time and should be programmed to ensure enough time for the characteristics of an external device.
The default setting for the EBI is to insert an IDLE cycle between EBI transactions to the same bank. The IDLE cycle insertion is shown for two back-to-back read transactions in Figure 185. For cases where the IDLE state can also provide the required bus turn-around time, the RDHOLD parameter can be programmed to 0. For increased EBI access performance, the automatic IDLE state insertion can be disabled by setting the NOIDLEn bits in the EBICR register to 1. This example is shown in Figure 186 for two back-to-back reads in a non-multiplexed address mode.

An IDLE cycle will automatically be inserted for the following cases:
- Between two external device transactions to the same bank when the NOIDLEn bit is 0.
- Between two external device transactions to different banks.
- Between a read and a subsequent write on the EBI_AD lines.
- When no request for an external transaction is available in the EBI.

- NOIDLE = 0:



- NOIDLE = 1:



18.5.6 AHB Transaction Width Conversion

The mapping of AHB transactions to an external device depends on the data width of the external device and whether the byte lanes of the external device are supported or not. The EBI will automatically translate the different AHB transaction width to external device transactions which matches the external bus capabilities of the device.

- If the AHB master (CPU) transaction width is larger than the external bus transaction width. The EBI will split and translate the AHB transaction into consecutive multiple external transactions which have consecutively incrementing the address and start with the least significant data from AHB transaction.

- If the AHB master (CPU) transaction width is smaller than the external bus transaction width. The EBI behaviour depends on whether the byte lanes are available or not. Reads either use byte lanes to select the required data

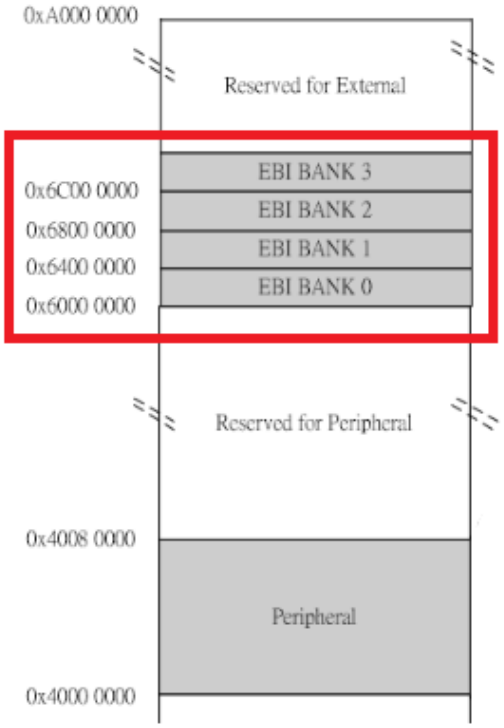
when it is available, or read according to the full data bus width of the external device and ignore the superfluous data when a byte lane is not available. Writes either use a byte lane to select the required data when it is available, or EBI automatically perform a read-modify-write sequence when a byte lane is not available.

AHB Transaction	8-bit External Device Transaction	16-bit External Device Transaction (Enable Byte Control)	16-bit External Device Transaction (Disable Byte Control)
8-bit Read	1 x 8-bit Read	1 x 8-bit Read (using Byte Control)	1 x 16-bit Read (EBI ignores the redundant data)
8-bit Write	1 x 8-bit Write	1 x 8-bit Write (using Byte Control)	1 x 16-bit Read (modify) 1 x 16-bit Write
16-bit Read	2 x 8-bit Read	1 x 16-bit Read	1 x 16-bit Read
16-bit Write	2 x 8-bit Write	1 x 16-bit Write	1 x 16-bit Write
32-bit Read	4 x 8-bit Read	2 x 16-bit Read	2 x 16-bit Read
32-bit Write	4 x 8-bit Write	2 x 16-bit Write	2 x 16-bit Write

External Bus Width	Access from AHB Master		Access to EBI				
	Type	HADDR[1:0]	Access split	Output data on EBI A[1:0]	Valid data on EBI AD[15:0]	Output data on EBI UB	Output data on EBI LB
8-bit	8-bit	00b	No	00b	EBI AD[7:0]	1	0
		01b	No	01b			
		10b	No	10b			
		11b	No	11b			
	16-bit	00b	1/2 access	00b			
			2/2 access	01b			
		10b	1/2 access	10b			
			2/2 access	11b			
	32-bit	00b	1/4 access	00b			
			2/4 access	01b			
			3/4 access	10b			
			4/4 access	11b			
16-bit	8-bit	00b	No	x0b	EBI AD[7:0]	1	0
		01b	No	x0b	EBI AD[15:8]	0	1
		10b	No	x1b	EBI AD[7:0]	1	0
		11b	No	x1b	EBI AD[15:8]	0	1
	16-bit	00b	No	x0b	EBI AD[15:0]	0	0
		10b	No	x1b	EBI AD[15:0]	0	0
	32-bit	00b	1/2 access	x0b	EBI AD[15:0]	0	0
			2/2 access	x1b	EBI AD[15:0]	0	0

18.5.7 EBI Bank Access

The EBI is split into 4 different address regions and each owns an individual CSn line. When accessing one of the memory regions, the corresponding CSn line is asserted. Up to 4 separate devices can share the EBI lines and is identified by the CSn line. Each bank can individually be enabled or disabled in the EBI_CTRL register. And each bank can individually define the external device behavior, including the data width, the timing definitions, and the pin polarities. The data space of each bank can be accessed up to 64MB, and the EBI regions address starts at 0x60000000 in the memory map. When running code via EBI regions starting at this address, the Cortex-M0 uses the System bus interface to fetch instructions.



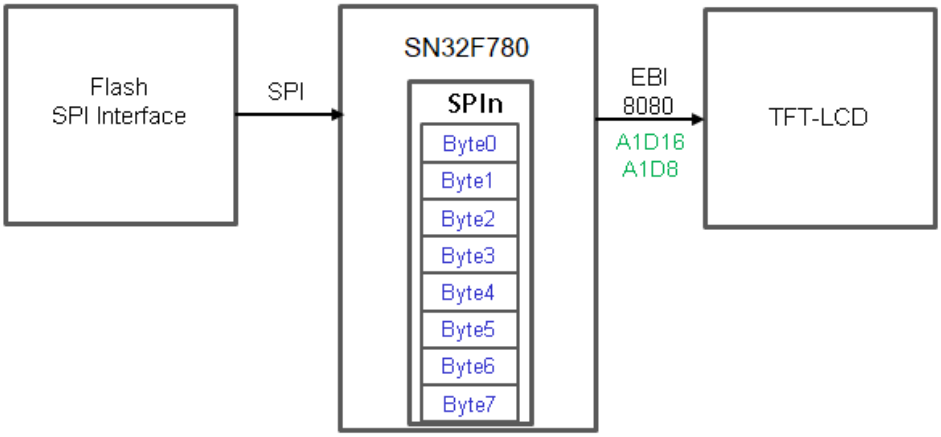
18.5.8 EBI Ready

Some external devices are able to indicate that they have not finished the write or read operation by asserting the wait signal. The EBI_ARDY input signal is used to extend the read or write cycles for slow external devices when it is enabled ARDY$_N$EN bit = 1 in the EBI_CTRL register. EBI_ARDY can be configured by the polarity of this signal with the ARDYPOL bit in the EBIPR register. If the ARDYPOL bit is set to active low, then the read or write cycle is extended while the EBI_ARDY line is kept high. It also provides a timeout check to prevent a system lock up condition in case where the external device does not de-assert the EBI_ARDY signal. It will generate a bus asynchronous ready time-out interrupt if EBI_ARDY is not deasserted within the timeout period. This timeout period has a default value of 32 HLCK clock cycles. Its functionality can be disabled by setting the ARDYTDIS bit in the EBI_CTRL register. Note that each memory bank can individually set its wait behavior definition.

18.6 8080 MODE DMA-CONTROLLED TFT-LCD

Direct memory access (DMA) is used in order to provide high-speed data transfer between external SPI-flash and TFT-LCD. Data can be moved from SPI FIFOs to TFT-LCD by DMA without any CPU actions. This keeps CPU resources free for other operations.

The 8080 MODE DMA only supports RGB565 (65536 colors) format, and the data length of SPIn is 8 bits. Set the total bytes of the SPI FLASH which DMA transferred in EBI_DMACNT register



18.6.1 DMA TIMING FLOW

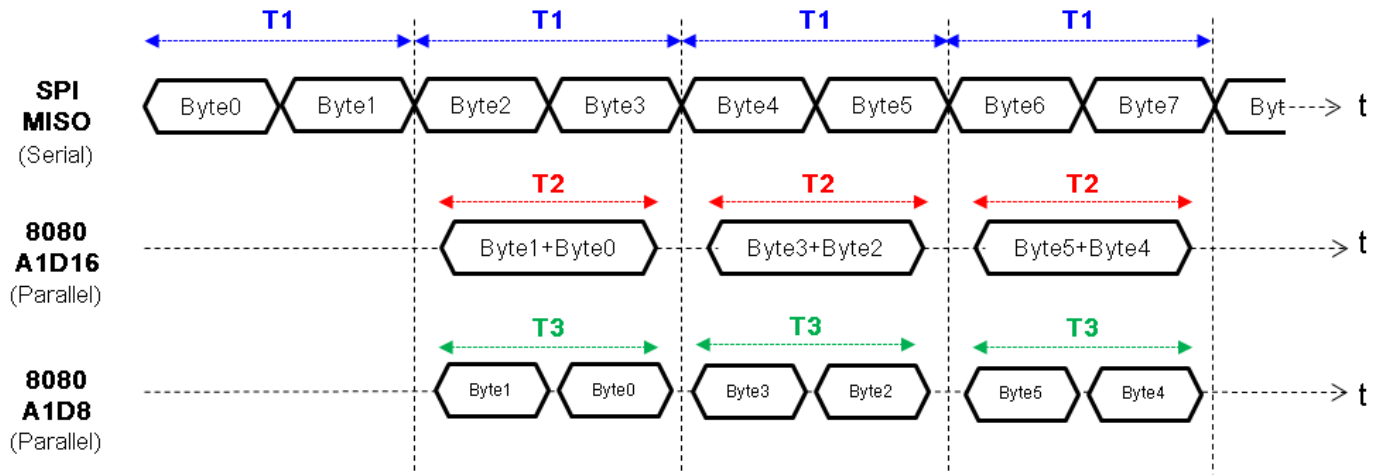
In A1D16 mode, the MCU will receive 2 8-bit data from SPI Flash and transmit 1 16-bit data to panel directly, and the time for MCU to receive 2 8-bit data from SPI Flash (T1) SHALL be more than or equal to the time for MCU to transmit data via A1D16 (T2).

In A1D8 mode, the MCU will receive 2 8-bit data from SPI Flash and transmit 2 8-bit data to panel directly , and the time for MCU to receive 2 8-bit data from SPI Flash (T1) SHALL be more than or equal to the time for MCU to transmit data via A1D8 (T3).

✷ ***Note:***

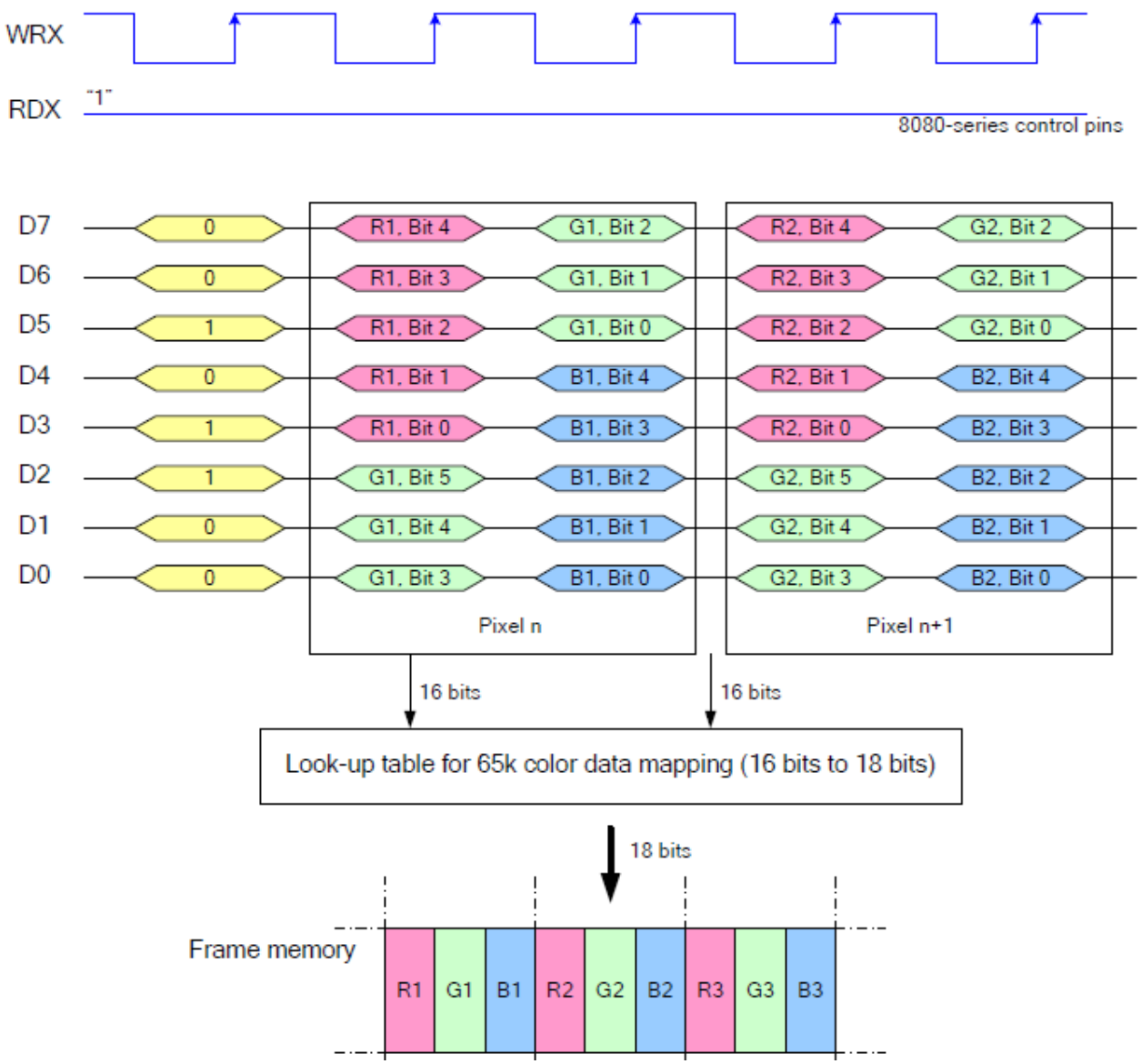
1. The speed of SPIn SHALL be less than or equal to the speed of EBI 8080 Mode.

2. The 8080 Mode DMA only supports RGB565 (65536 colors) format.

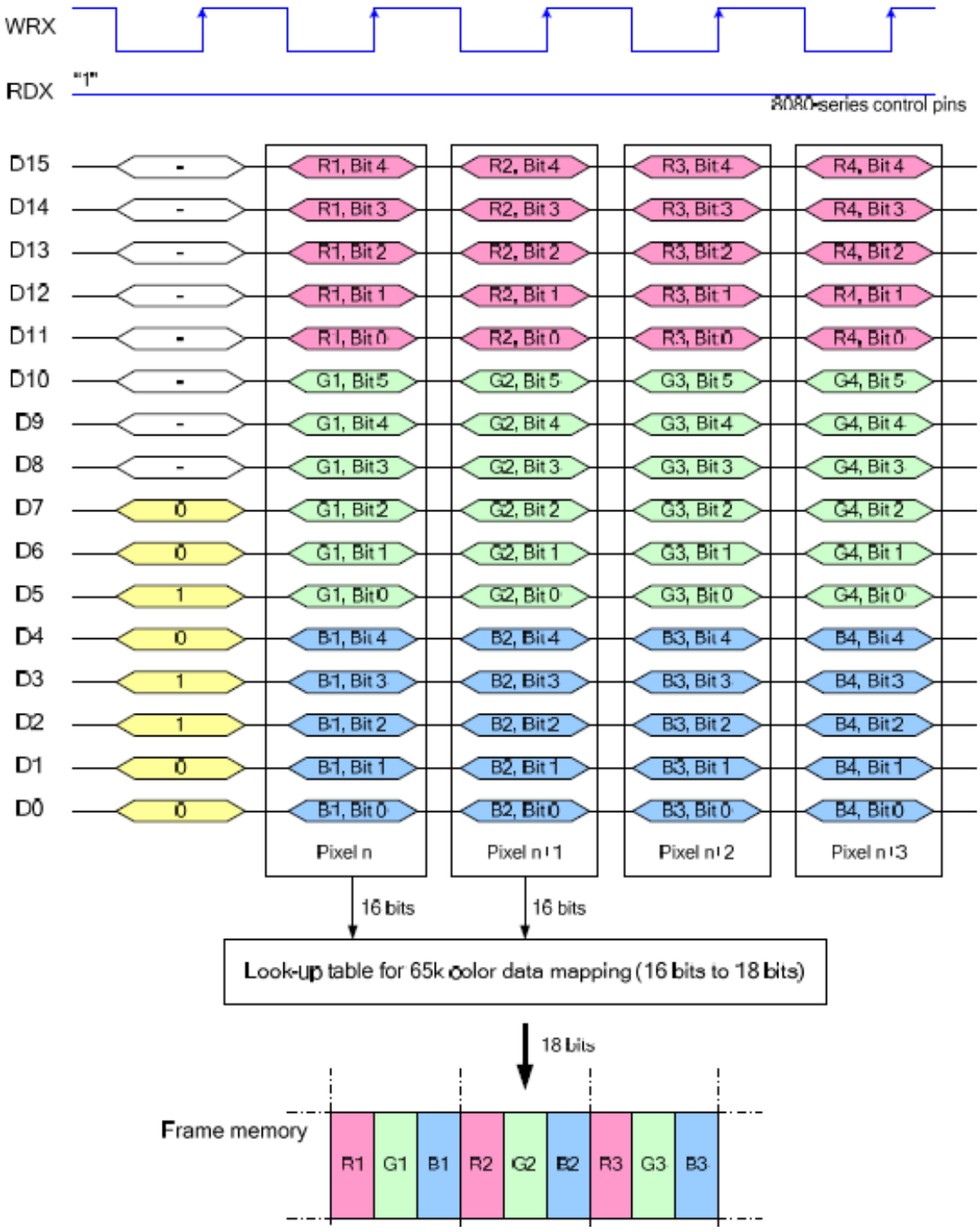


18.6.2 DMA DATA FORMAT

- A1D8:



- A1D16:


WRX
RDX
"1"
R/W series control pins
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
R1, Bit 4
R1, Bit 3
R1, Bit 2
R1, Bit 1
R1, Bit 0
G1, Bit 5
G1, Bit 4
G1, Bit 3
G1, Bit 2
G1, Bit 1
G1, Bit 0
B1, Bit 4
B1, Bit 3
B1, Bit 2
B1, Bit 1
B1, Bit 0
R2, Bit 4
R2, Bit 3
R2, Bit 2
R2, Bit 1
R2, Bit 0
G2, Bit 5
G2, Bit 4
G2, Bit 3
G2, Bit 2
G2, Bit 1
G2, Bit 0
B2, Bit 4
B2, Bit 3
B2, Bit 2
B2, Bit 1
B2, Bit 0
R3, Bit 4
R3, Bit 3
R3, Bit 2
R3, Bit 1
R3, Bit 0
G3, Bit 5
G3, Bit 4
G3, Bit 3
G3, Bit 2
G3, Bit 1
G3, Bit 0
B3, Bit 4
B3, Bit 3
B3, Bit 2
B3, Bit 1
B3, Bit 0
R4, Bit 4
R4, Bit 3
R4, Bit 2
R4, Bit 1
R4, Bit 0
G4, Bit 5
G4, Bit 4
G4, Bit 3
G4, Bit 2
G4, Bit 1
G4, Bit 0
B4, Bit 4
B4, Bit 3
B4, Bit 2
B4, Bit 1
B4, Bit 0
Pixel n
Pixel n+1
Pixel n+2
Pixel n+3
16 bits
16 bits
Look-up table for 65k color data mapping (16 bits to 18 bits)
18 bits
Frame memory
R1
G1
B1
R2
G2
B2
R3
G3
B3

18.7 EBI REGISTERS

Base Address: 0x4003 6000

18.7.1 EBI Control register (EBI_CTRL)

Address offset: 0x00

Bit	Name	Description	Attribute	Reset
31:28	Reserved		R	0
27	BK8080MODE3	Bank 3 8080 mode (Only available when MODE3[1:0]=0x11) 0: A1D16 1: A1D8	R/W	0
26	BK8080MODE2	Bank 2 8080 mode (Only available when MODE3[1:0]=0x11) 0: A1D16 1: A1D8	R/W	0
25	BK8080MODE1	Bank 1 8080 mode (Only available when MODE3[1:0]=0x11) 0: A1D16 1: A1D8	R/W	0
24	BK8080MODE0	Bank 0 8080 mode (Only available when MODE3[1:0]=0x11) 0: A1D16 1: A1D8	R/W	0
23:20	IDLETIME[3:0]	Counts for Bus idle time. Bus idle time = IDLETIME[3:0] * EBI_PCLK	R/W	0xF
19	ARDY3EN	ARDY of Bank 3 enable bit. 0: Disable EBI bank 3 ARDY function. 1: Enable EBI bank 3 ARDY function.	R/W	0
18	ARDY2EN	ARDY of Bank 2 enable bit. 0: Disable EBI bank 2 ARDY function. 1: Enable EBI bank 2 ARDY function.	R/W	0
17	ARDY1EN	ARDY of Bank 1 enable bit. 0: Disable EBI bank 1 ARDY function. 1: Enable EBI bank 1 ARDY function.	R/W	0
16	ARDY0EN	ARDY of Bank 0 enable bit. 0: Disable EBI bank 0 ARDY function. 1: Enable EBI bank 0 ARDY function.	R/W	0
15	BC3EN	Byte control of Bank 3 enable bit. 0: Disable EBI bank 3 byte control function. 1: Enable EBI bank 3 byte control function.	R/W	0
14	BC1EN	Byte control of Bank 2 enable bit. 0: Disable EBI bank 2 byte control function. 1: Enable EBI bank 2 byte control function.	R/W	0
13	BC1EN	Byte control of Bank 1 enable bit. 0: Disable EBI bank 1 byte control function. 1: Enable EBI bank 1 byte control function.	R/W	0
12	BC0EN	Byte control of Bank 0 enable bit. 0: Disable EBI bank 0 byte control function. 1: Enable EBI bank 0 byte control function.	R/W	0
11	BANK3EN	Bank 3 enable bit 0: Disable 1: Enable	R/W	0
10	BANK2EN	Bank 2 enable bit 0: Disable 1: Enable	R/W	0
9	BANK1EN	Bank 1 enable bit 0: Disable 1: Enable	R/W	0
8	BANK0EN	Bank 0 enable bit 0: Disable 1: Enable	R/W	0
7:6	MODE3[1:0]	EBI bank 3 access mode 00: A_ND8 (Also need to set AL3[3:0]) 01: A_ND16 (Also need to set AL3[3:0])	R/W	0

		10: AND16ALE (Also need to set AL3[3:0]) 11: 8080 (Also need to set BK8080MODE3)		
5:4	MODE2[1:0]	EBI bank 2 access mode 00: AND8 (Also need to set AL2[3:0]) 01: AND16 (Also need to set AL2[3:0]) 10: AND16ALE (Also need to set AL2[3:0]) 11: 8080 (Also need to set BK8080MODE2)	R/W	0
3:2	MODE1[1:0]	EBI bank 1 access mode 00: AND8 (Also need to set AL1[3:0]) 01: AND16 (Also need to set AL1[3:0]) 10: AND16ALE (Also need to set AL1[3:0]) 11: 8080 (Also need to set BK8080MODE1)	R/W	0
1:0	MODE0[1:0]	EBI bank 0 access mode 00: AND8 (Also need to set AL0[3:0]) 01: AND16 (Also need to set AL0[3:0]) 10: AND16ALE (Also need to set AL0[3:0]) 11: 8080 (Also need to set BK8080MODE0)	R/W	0

18.7.2 EBI Address Length Control register (EBI_ALCTRL)

Address offset: 0x04

Bit	Name	Description	Attribute	Reset
31:16	Reserved		R	0
15:12	AL3[3:0]	EBI bank 3 address length = AL3 + 16 0000: AL3 = 0 0001: AL3 = 1 …….. 1010: AL3 = 10 Other: AL3 = 10	R/W	0
11:8	AL2[3:0]	EBI bank 2 address length = AL2 + 16 0000: AL2 = 0 0001: AL2 = 1 …….. 1010: AL2 = 10 Other: AL2 = 10	R/W	0
7:4	AL1[3:0]	EBI bank 1 address length = AL1 + 16 0000: AL1 = 0 0001: AL1 = 1 …….. 1010: AL1 = 10 Other: AL1 = 10	R/W	0
3:0	AL0[3:0]	EBI bank 0 address length = AL0 + 16 0000: AL0 = 0 0001: AL0 = 1 …….. 1010: AL0 = 10 Other: AL0 = 10	R/W	0

18.7.3 EBI Status register (EBI_STATUS)

Address offset: 0x08

Bit	Name	Description	Attribute	Reset
31:9	Reserved		R	0
8	EBISMRST	EBI State Machine Reset 0: Normal 1: Reset EBI state machine	R/W	0

7:5	Reserved		R	0
4	EBIARDY	EBI Asynchronous Ready Status 0: EBI_ARDY is inactive/busy 1: EBI_ARDY is active/ready	R	1
3:1	Reserved		R	0
0	EBIBUSY	EBI BUSY 0: EBI is idle 1: EBI is busy	R	0

18.7.4 EBI Address Timing register n (EBI_TADDRn) n=0~3

Address offset: 0x10, 0x14, 0x18, 0x1C

ADDRSETUP[3:0] is the number of cycles the EBI_AD bus is driven before EBI_ALE is asserted.
ADDRHOLD[3:0] is the number of cycles the EBI_AD bus is held after EBI_ALE is asserted.

Bit	Name	Description	Attribute	Reset
31:12	Reserved		R	0
11:8	ADDRHOLD[3:0]	Counts for Address Hold Time Address Hold Time = ADDRHOLD[3:0] * EBI_PCLK	R/W	0xF
7:4	Reserved		R	0
3:0	ADDRSETUP[3:0]	Counts for Address Setup Time 0: Address Hold Time = 1 * EBI_PCLK N: Address Hold Time = N * EBI_PCLK	R/W	0xF

18.7.5 EBI Read Timing register n (EBI_TREADn) n=0~3

Address offset: 0x20, 0x24, 0x28, 0x2C

RDSETUP[3:0] is the number of cycles for the address setup before EBI_OE is asserted.
RDSTRB [5:0] is the number of cycles the EBI_OE is held active, after the specified number of cycles, the data is read.
RDHOLD[3:0] is the number of cycles that the EBI_CSn is held active after EBI_OE is de-asserted. This interval is used for bus turnaround.

Bit	Name	Description	Attribute	Reset
31:20	Reserved		R	0
19:16	RDHOLD[3:0]	Counts for Read Hold Time Read Hold Time = RDHOLD[3:0] * EBI_PCLK	R/W	0xF
15:14	Reserved		R	0
13:8	RDSTRB[5:0]	Counts for Read Strobe Time 0: Read Strobe Time = 1 * EBI_PCLK N: Read Strobe Time = N * EBI_PCLK	R/W	0x3F
7:4	Reserved		R	0
3:0	RDSETUP[3:0]	Counts for Read Setup Time Read Setup Time = RDSETUP[3:0] * EBI_PCLK	R/W	0xF

18.7.6 EBI Write Timing register n (EBI_TWRITEn) n=0~3

Address offset: 0x30, 0x34, 0x38, 0x3C

WESETUP[3:0] is the number of cycles for the address setup before EBI_WE is asserted.
WESTRB [5:0] is the number of cycles the EBI_WE is held active.
WEHOLD[3:0] is the number of cycles that the EBI_CSn is held active after EBI_WE is de-asserted.

Bit	Name	Description	Attribute	Reset
31:20	Reserved		R	0
19:16	WEHOLD[3:0]	Counts for Write Hold Time Write Hold Time = WEHOLD[3:0] * EBI_PCLK	R/W	0xF
15:14	Reserved		R	0
13:8	WESTRB[5:0]	Counts for Write Strobe Time 0: Write Strobe Time = 1 * EBI_PCLK N: Write Strobe Time = N * EBI_PCLK	R/W	0x3F
7:4	Reserved		R	0
3:0	WESETUP[3:0]	Counts for Write Setup Time Write Setup Time = WESETUP[3:0] * EBI_PCLK	R/W	0xF

18.7.7 EBI Polarity register n (EBI_PRn) n=0~3

Address offset: 0x40, 0x44, 0x48, 0x4C

Bit	Name	Description	Attribute	Reset
31:6	Reserved		R	0
5	UBLBPOL	Upper Byte and Lower Byte Polarity 0: UB and LB are active low/idle high 1: Reserved	R	0
4	ARDYPOL	Asynchronous Ready Polarity 0: ARDY is active low 1: ARDY is active high	R/W	0
3	ALEPOL	Address Latch Polarity 0: ALE is active low/idle high 1: Reserved	R	0
2	WEPOL	Write Enable Polarity 0: WE is active low/idle high 1: Reserved	R	0
1	OEPOL	Output Enable Polarity 0: OE is active low/idle high 1: Reserved	R	0
0	CSPOL	Chip Selection Polarity 0: CS is active low/idle high 1: Reserved	R	0

18.7.8 EBI Interrupt Enable register (EBI_IE)

Address offset: 0x50

Bit	Name	Description	Attribute	Reset
31:6	Reserved		R	0
5	DMATCIE	DMA transfer complete interrupt enable bit 0: Disable 1: Enable	R/W	0
4	DMAHTIE	DMA half-transfer interrupt enable bit 0: Disable 1: Enable	R/W	0

3	RWERREN	Interrupt for read/write error enable bit Ex: Read/Write during EBIARDY is busy 0: Disable 1: Enable	R/W	0
2	SMRSTEN	Interrupt for issuing a transaction during EBI state machine reset period enable bit. 0: Disable 1: Enable	R/W	0
1	ACCDISEN	Interrupt for accessing the disabled bank enable bit. 0: Disable 1: Enable	R/W	0
0	ARDYTOEN	EBI asynchronous ready time-out (32T*HCLK) interrupt enable bit 0: Disable 1: Enable	R/W	0

18.7.9 EBI Interrupt Flag register (EBI_RIS)

Address offset: 0x54

EBI_RIS shall indicate the status whether the corresponding IE bit is set or not.

Bit	Name	Description	Attribute	Reset
31:6	Reserved		R	0
5	DMATCIF	DMA transfer complete flag 0: No transfer completion 1: A transfer complete event occurs (when DMA transmitting times is equal to DMACNT)	R	0
4	DMAHTIF	DMA half-transfer flag 0: No half-transfer event 1: A half-transfer event occurs (when DMA transmitting times is equal to DMAHTCNT)	R	0
3	RWERRIF	EBI read/write error flag 0: Nor error 1: Read Write error	R	0
2	SMRSTIF	EBI state machine resetting flag 0: Not resetting. 1: EBI is resetting the state machine.	R	0
1	ACCDISIF	EBI accessing the disabled bank flag. 0: Not accessing 1: EBI is accessing the disabled bank.	R	0
0	ARDYTOIF	EBI asynchronous ready time-out (32T*HCLK) flag 0: Not time-out. 1: The EBI asynchronous ready time-out.	R	0

18.7.10 EBI Interrupt Clear register (EBI_IC)

Address offset: 0x58

Bit	Name	Description	Attribute	Reset
31:6	Reserved		R	0
5	DMATCIC	Select the DMATCIF flag to be cleared 0: No effect 1: Clear DMATCIF flag	W	0
4	DMAHTIC	Select the DMAHTIF flag to be cleared 0: No effect 1: Clear DMAHTIF flag	W	0
3	RWERRIC	Select the RWERRIF flag to be cleared 0: No effect	W	0

		1: Clear RWERRIF flag		
2	SMRSTIC	Select the SMRSTIF flag to be cleared 0: No effect 1: Clear SMRSTIF flag	W	0
1	ACCDISIC	Select the ACCDISIF flag to be cleared 0: No effect 1: Clear ACCDISIF flag	W	0
0	ARDYTOIC	Select the ARDYTOIF flag to be cleared 0: No effect 1: Clear ARDYTOIF flag	W	0

18.7.11 EBI DMA Control register (EBI_DMACTRL)

Address offset: 0x5C

✷ ***Note: The speed of SPIn SHALL be greater or equal to the speed of EBI.***

Bit	Name	Description	Attribute	Reset
31:4	Reserved		R	0
3:2	BANKSELECT[1:0]	EBI bank n select bits 00b: BANK 0 01b: BANK 1 10b: BANK 2 11b: BANK 3	R/W	0
1	SPISELECT	SPIn select bit (Only 8-bit data length is supported) 0: SPI0 1: SPI1	R/W	0
0	DMAEN	SPIn to EBI DMA enable bit (Only supported when MODEx[1:0] =0x11) 0: Disable (Set by HW when DMATCIF becomes 1) 1: Enable (Set by FW)	R/W	0

18.7.12 EBI DMA Number of Data Transfer register (EBI_DMACNT)

Address offset: 0x64

This register can only be written when the DMA is disabled. Once the DMA is enabled, this register is read-only, indicating the remaining bytes to be transmitted.

Once the transfer is completed (CURCNT=CNT), HW will trigger DMATC interrupt if DMATCIE = 1.

Bit	Name	Description	Attribute	Reset
31:28	Reserved		R	0
27:0	CNT[27:0]	Number of data bytes (CNT+1) to be transferred.	R/W	0

18.7.13 EBI DMA Number of Half Data Transfer register (EBI_DMAHTCNT)

Address offset: 0x68

This register can only be written when the DMA is disabled. Once the DMA is enabled, this register is read-only, indicating the remaining bytes to be transmitted.

Once the half transfer is completed (CURCNT=HTCNT), HW will trigger DMATC interrupt if DMAHTIE = 1.

Bit	Name	Description	Attribute	Reset
31:28	Reserved		R	0
27:0	HTCNT[27:0]	Half number of data bytes (HTCNT+1) to be transferred.	R/W	0xFFFFFFF

18.7.14 EBI DMA Current Transfer Data Counter register (EBI_CURCNT)

Address offset: 0x6C

Bit	Name	Description	Attribute	Reset
31:28	Reserved		R	0
27:0	CURCNT[27:0]	This field indicates the DMA current transfer data counter. Count from 0 to DMACNT.	R	0

19 CYCLIC REDUNDANCY CHECK (CRC)

19.1 OVERVIEW

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from 16- or 32-bit data word and a generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. The CRC calculation circuit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

19.2 FEATURES

1. Support

CRC-32 polynomial: $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X+1$

CRC-16 polynomial: $X^{16}+X^{15}+X^2+1$

CRC-16-CCITT polynomial: $X^{16}+X^{12}+X^5+1$

	CRC-16-CCITT $X^{16}+X^{12}+X^5+1$	CRC-16 $X^{16}+X^{15}+X^2+1$	CRC-32(-IEEE802.3) $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X+1$
Poly	0x1021	0x8005	0x04C11DB7
Seed(Init)	0xFFFF	0x0000	0xFFFFFFFF
XOROut	0x0000	0x0000	0xFFFFFFFF
RefIn	No	Yes	Yes
RefOut	No	Yes	Yes

2. Handles 16-, 32-bit data size

3. Single input/output 32-bit data register

4. Input buffer to avoid bus stall during calculation

5. CRC computation done in 4T IHRC clock cycles for the 32-bit data size

6. Polynomial representations of cyclic redundancy checks

19.3 CRC REGISTERS

Base Address: 0x4003 8000

19.3.1 CRC Control register (CRC_CTRL)

Address offset: 0x00

Bit	Name	Description	Attribute	Reset
31:5	Reserved	Reserved	R/W	0
4	BUSY	CRC calculation busy flag. 0: CRC calculation Idle/Finished. 1: CRC calculation is in process.	R	0
3	URCRCEN	Enable bit of the CRC calculation for the User ROM, except the last page. 1: Start the CRC operation for the User ROM, except the last page. This bit is set only by SW and reset by HW. 0: Stop/Finish operation.	R/W	0
2	RESET	Reset bit 0: No effect. 1: Reset the CRC calculation circuit. (Reset the initial seed value and BUSY bit to 0). Clear this bit when the reset operation had finished by HW.	R/W	0
1:0	CRC[1:0]	CRC Polynomial 00: CRC-16-CCITT 01: CRC-16 10: CRC-32 11: Reserved	R/W	0

19.3.2 CRC Data register (CRC_DATA)

Address offset: 0x04

✸ ***Note: Support 8-bit (Byte) Write ONLY!***

Bit	Name	Description	Attribute	Reset
31:0	DATA[31:0]	Data to be input or read. Write: Input 8-bit data to the CRC calculator and start to calculation process. Read: Output the previous CRC calculation result depends on the CRC Polynomial.	R/W	0

20 USB FS DEVICE INTERFACE

20.1 OVERVIEW

The USB is the answer to connectivity for the PC architecture. A fast, bi-directional interrupt pipe, low-cost, dynamically attachable serial interface is consistent with the requirements of the PC platform of today and tomorrow. The SONIX USB microcontrollers are optimized for human-interface computer peripherals such as a mouse, keyboard, joystick, and game pad.

USB Specification Compliance

— Conforms to USB specifications, Version 2.0.

— Supports 1 Full-speed USB device address.

— Supports 1 control endpoint and 6 configurable endpoints for interrupt/bulk transfer.

— Integrated USB transceiver.

— 5V to 3.3V regulator output for D+ 1.5K ohm internal resistor pull up.

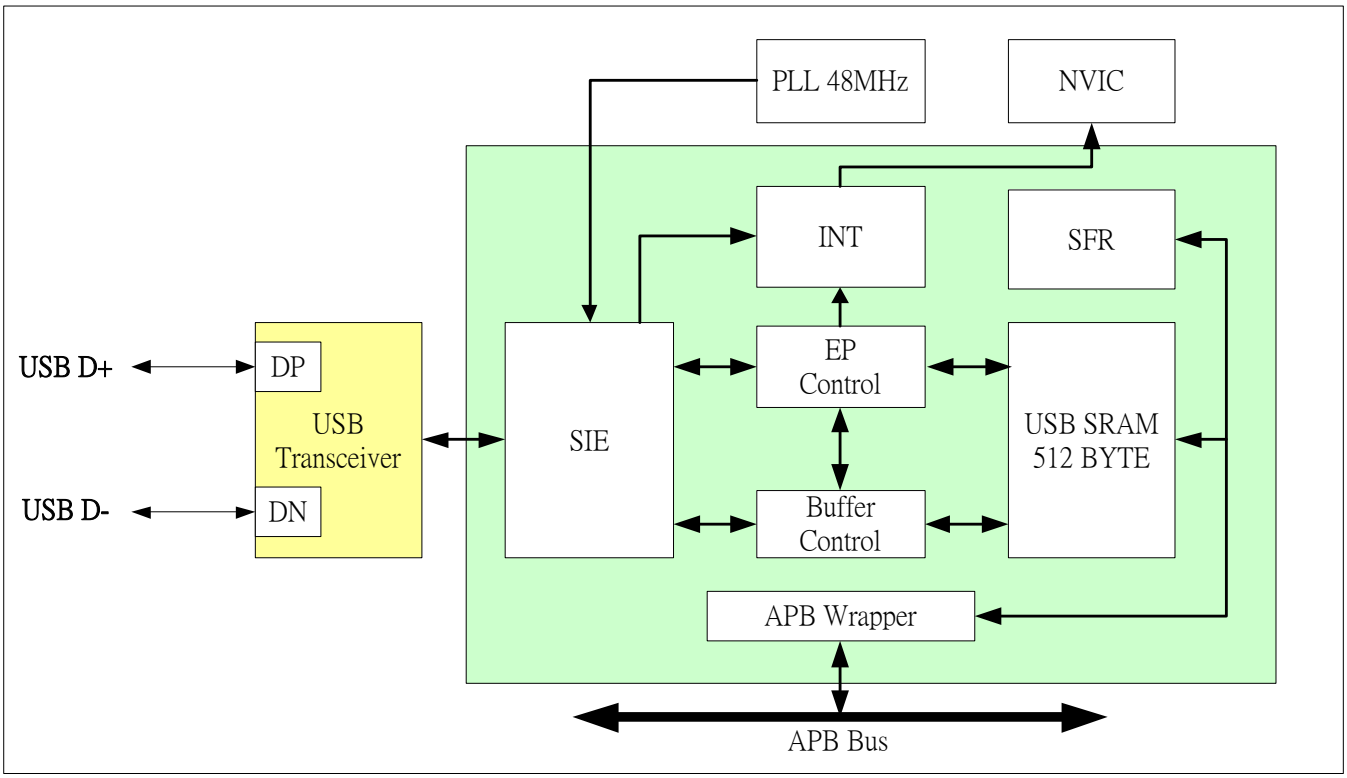
20.2 FEATURES

1. Conforms to USB specifications, Version 2.0.
2. Supports 1 Full-speed USB device address.
3. Supports 1 control endpoint with maximum packet size 8 bytes, 16 bytes, 32 bytes, or 64 bytes.
4. Supports 4 endpoints configurable for interrupt/bulk transfer.
5. Supports USB SRAM size 512 bytes shared by all 7 endpoints.
6. Flexible data FIFO offset setting for endpoints except endpoint 0.
7. 5V to 3.3V regulator output for D+ 1.5K ohm internal resistor pull up.
8. Integrated USB transceiver.
9. FS USB function work under system clock SYSCLK/1, SYSCLK/2, SYSCLK/4.

20.3 PIN DESCRIPTION

Pin Name	Type	Description	GPIO Configuration
D+	I/O	USB differential signal D+	N/A
D-	I/O	USB differential signal D-	N/A

20.4 BLOCK DIAGRAM

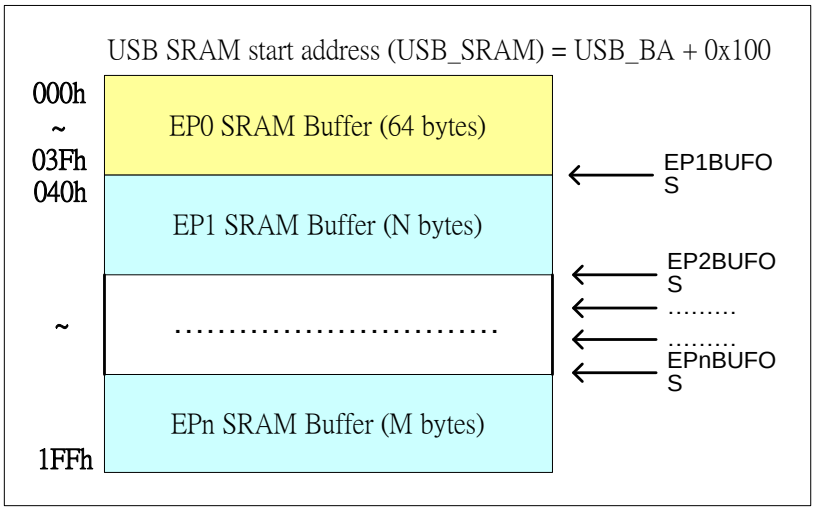


20.5 USB SRAM ACCESS

There is 512 bytes SRAM in the controller and the 7 endpoints share this buffer. The user shall configure each endpoint's effective starting address in the buffer offset register before the USB function active. The USB_EPnBUFOS block is used to control each endpoint's effective starting address.

The principles to access USB SRAM are as below.

1. Each EPnBUFOS setting must be word-aligned, with 2 LSB bits equal to '0'.
2. The maximum length of EPn SRAM buffer is defined by user. However, each endpoint should have its own EPn SRAM buffer without overlapping each other.



20.6 USB MACHINE

The USB machine allows the microcontroller to communicate with the USB host. The hardware handles the following

USB bus activity independently of the microcontroller.

The USB machine will do:

1. Translate the encoded received data and format the data to be transmitted on the bus.
2. CRC checking and generation by hardware. If CRC is not correct, hardware will not send any response to USB host.
3. Send and update the data toggle bit (Data1/0) automatically by hardware.
4. Send appropriate ACK/NAK/STALL handshakes.
5. SETUP, IN, or OUT Token type identification. Set the appropriate bit once a valid token is received.
6. Place valid received data in the appropriate endpoint FIFOs.
7. Bit stuffing/unstuffing.
8. Address checking. Ignore the transactions not addressed to the device.
9. Endpoint checking. Check the endpoint's request from USB host, and set the appropriate bit of registers.

Firmware is required to handle the rest of the following tasks:

1. Coordinate enumeration by decoding USB device requests.
2. Fill and empty the FIFOs.
3. Reset/Suspend/Resume coordination.
4. Remote wake up function.
5. Determine the right interrupt request of USB communication

20.7 USB INTERRUPT

The USB function will accept the USB host command and generate the relative interrupts, and enter USB_IRQ_Handler.

Firmware is required to check the USB status bit to realize what request comes from the USB host.

The USB function interrupt is generated when:

1. The endpoint 0 is set to accept a SETUP token.
2. The device receives an ACK handshake after a successful read transaction (IN) from the host.
3. If the endpoint is in ACK OUT modes, an interrupt is generated when data is received.
4. The USB host sends USB suspend request to the device.
5. USB bus reset/resume event occurs.
6. The USB endpoints interrupt after a USB transaction complete is on the bus.
7. The NAK handshaking when the NAK interrupt enables.

20.8 USB ENUMERATION

A typical USB enumeration sequence is shown below.

1. The host computer sends a SETUP packet followed by a DATA packet to USB address 0 requesting the Device descriptor.
2. Firmware decodes the request and retrieves its Device descriptor from the program memory tables.
3. The host computer performs a control read sequence and firmware responds by sending the Device descriptor over the USB bus, via the on-chip USB SRAM.
4. After receiving the descriptor, the host sends a SETUP packet followed by a DATA packet to address 0 assigning a new USB address to the device.
5. Firmware stores the new address in its USB Device Address Register after the no-data control sequence completes.
6. The host sends a request for the Device descriptor using the new USB address.
7. Firmware decodes the request and retrieves the Device descriptor from program memory tables.
8. The host performs a control read sequence and firmware responds by sending its Device descriptor over the USB bus.
9. The host generates control reads from the device to request the Configuration and Report descriptors.
10. Once the device receives a Set Configuration request, its functions may now be used.
11. Firmware should take appropriate action for Endpoint 0~N transactions, which may occur from this point.

20.9 USB REGISTERS

Base Address: 0x4005 C000

R: read only, W: write only, R/W: both read and write

Register	Offset	R/W	Description	Reset Value
USB_INTEN	0x00	R/W	USB Interrupt Enable Register.	0x0000_0000
USB_INSTS	0x04	R	USB Interrupt Event Status Register.	0x0000_0000
USB_INSTSC	0x08	W	USB Interrupt Event Status Clear Register.	0x0000_0000
USB_ADDR	0x0C	R/W	USB Device Address Register.	0x0000_0000
USB_CFG	0x10	R/W	USB Configuration Register.	0x8000_0000
USB_SGCTL	0x14	R/W	USB Signal Control Register.	0x0000_0000
USB_EP0CTL	0x18	R/W	USB Endpoint 0 Control Register.	0x0000_0000
USB_EP1CTL	0x1C	R/W	USB Endpoint 1 Control Register.	0x0000_0000
USB_EP2CTL	0x20	R/W	USB Endpoint 2 Control Register.	0x0000_0000
USB_EP3CTL	0x24	R/W	USB Endpoint 3 Control Register.	0x0000_0000
USB_EP4CTL	0x28	R/W	USB Endpoint 4 Control Register.	0x0000_0000
USB_EP5CTL	0x2C	R/W	USB Endpoint 5 Control Register.	0x0000_0000
USB_EP6CTL	0x30	R/W	USB Endpoint 6 Control Register.	0x0000_0000
USB_EPTOGGLE	0x3C	R/W	USB Endpoint Data Toggle Register.	0x0000_003F
USB_EP1BUFOS	0x48	R/W	USB Endpoint 1 Buffer Offset Register.	0x0000_0040
USB_EP2BUFOS	0x4C	R/W	USB Endpoint 2 Buffer Offset Register.	0x0000_0080
USB_EP3BUFOS	0x50	R/W	USB Endpoint 3 Buffer Offset Register.	0x0000_00C0
USB_EP4BUFOS	0x54	R/W	USB Endpoint 4 Buffer Offset Register.	0x0000_0100
USB_EP5BUFOS	0x58	R/W	USB Endpoint 5 Buffer Offset Register.	0x0000_0140
USB_EP6BUFOS	0x5C	R/W	USB Endpoint 6 Buffer Offset Register.	0x0000_0180
USB_FRMNO	0x60	R	USB Frame Number Register.	0x0000_0000
USB_PHYPRM	0x64	R/W	USB PHY Parameter Register.	0x0000_0000
USB_PHYPRM2	0x6C	R/W	USB PHY Parameter Register 2.	0x0000_0000
USB_PS2CTL	0x70	R/W	USB PS/2 Control Register.	0x0000_0000
USB_RWADDR	0x78	R/W	USB FIFO Read/Write Address Register	0x0000_0000
USB_RWDATA	0x7C	R/W	USB FIFO Data Register	0x0000_0000
USB_RWSTATUS	0x80	R/W	USB FIFO Read/Write Status Register	0x0000_0000
USB_RWADDR2	0x84	R/W	USB FIFO Read/Write Address Register2	0x0000_0000
USB_RWDATA2	0x88	R/W	USB FIFO Data Register2	0x0000_0000
USB_RWSTATUS2	0x8C	R/W	USB FIFO Read/Write Status Register2	0x0000_0000
USB_SRAM	0x100	R/W	USB 512 byte SRAM	Undefined

20.9.1 USB Interrupt Enable Register (USB_INTEN)

Address Offset: 0x00

Reset value: 0x0000 0000

Bit	Name	Description	Attribute	Reset
31	BUS_IE	Bus Event Interrupt Enable. 0: Disable BUS event interrupt. 1: Enable Bus event interrupt. Any bus event including BUS_RESET, BUS_SUSPEND, and BUS_RESUME triggers USB interrupt.	R/W	0
30	USB_SOF_IE	USB SOF Interrupt Enable. 0: Disable USB SOF interrupt. 1: Enable USB SOF interrupt.	R/W	0
29	USB_IE	USB Event Interrupt Enable. 0: Disable USB event interrupt. 1: Enable USB event interrupt. Any USB event except EP1~EP6's NAK triggers USB interrupt.	R/W	0
28	BUSWK_IE	BUSWK_IE: Bus Wake Up Interrupt Enable. 0: Disable Wake Up event interrupt. 1: Enable Wake Up event interrupt.	R/W	0

27:7	Reserved		R	0
6	EPN_ACK_EN	Enable all of EP(1~6) ACK Interrupt 0: Disable EP1 to 6 ACK interrupt function. 1: Enable EP1 to 6 ACK interrupt function.	R/W	0
5	EP6_NAK_EN	EP6 NAK Interrupt Enable 0: Disable EP6 NAK interrupt function. 1: Enable EP6 NAK interrupt function.	R/W	0
4	EP5_NAK_EN	EP5 NAK Interrupt Enable 0: Disable EP5 NAK interrupt function. 1: Enable EP5 NAK interrupt function.	R/W	0
3	EP4_NAK_EN	EP4 NAK Interrupt Enable 0: Disable EP4 NAK interrupt function. 1: Enable EP4 NAK interrupt function.	R/W	0
2	EP3_NAK_EN	EP3 NAK Interrupt Enable 0: Disable EP3 NAK interrupt function. 1: Enable EP3 NAK interrupt function.	R/W	0
1	EP2_NAK_EN	EP2 NAK Interrupt Enable 0: Disable EP2 NAK interrupt function. 1: Enable EP2 NAK interrupt function.	R/W	0
0	EP1_NAK_EN	EP1 NAK Interrupt Enable 0: Disable EP1 NAK interrupt function. 1: Enable EP1 NAK interrupt function.	R/W	0

20.9.2 USB Interrupt Event Status Register (USB_INSTS)

Address Offset: 0x04

Reset value: 0x0000 0000

Bit	Name	Description	Attribute	Reset
31	BUS_RESET	USB Bus Reset signal (>2.5us SE0) flag 0: No bus reset signal is detected. 1: Bus reset signal is detected. Cleared by write 1 to USB_INSTSC[31].	R	0
30	BUS_SUSPEND	USB Bus Suspend signal (>3ms idle state) flag. 0: No bus suspend is detected. 1: Bus suspend is detected.	R	0
29	BUS_RESUME	USB Bus Resume signal flag 0: No bus resume signal is detected. 1: Bus resume signal from suspend mode is detected. Cleared by write 1 to USB_INSTSC[29].	R	0
28:27	Reserved		R	0
26	USB_SOF	USB SOF packet received flag. 0: No USB SOF packet. 1: USB SOF packet is received. Cleared by write 1 to USB_INSTSC[26].	R	0
25	BUS_WAKEUP	Bus Wake Up flag 0: No wakeup from suspend mode. 1: Wakeup from suspend mode. Cleared by write 1 to USB_INSTSC[25] *This flag will be set to '1'when wakeup from suspend mode under USB PLL 48MHz is off.	R	0
24	EP0_PRESETUP	EP0 Setup token packet flag. This flag will not trigger USB interrupt. 0: No EP0 Setup token packet. 1: EP0 Setup token packet is received. Cleared by write 1 to USB_INSTSC[24]	R	0
23	EP0_SETUP	EP0 Setup transaction flag. 0: No EP0 Setup transaction. 1: EP0 Setup transaction is completed. Cleared by write 1 to USB_INSTSC[23].	R	0
22	EP0_IN	EP0 IN ACK transaction flag. 0: No EP0 IN ACK Transaction.	R	0

		1: EP0 IN ACK transaction is completed. Cleared by write 1 to USB_INSTSC[22].		
21	EP0_OUT	EP0 OUT ACK transaction flag. 0: No EP0 OUT ACK transaction. 1: EP0 OUT ACK transaction is completed. Cleared by write 1 to USB_INSTSC[21].	R	0
20	EP0_IN_STALL	EP0 IN STALL transaction flag. 0: No EP0 IN STALL transaction. 1: EP0 IN STALL transaction is completed. Cleared by write 1 to USB_INSTSC[20].	R	0
19	EP0_OUT_STALL	EP0 OUT STALL transaction flag. 0: No EP0 OUT STALL transaction. 1: EP0 OUT STALL transaction is completed. Cleared by write 1 to USB_INSTSC[19].	R	0
18	ERR_SETUP	Wrong Setup data received. This flag will not trigger USB interrupt. 0: Normal 8-byte Setup DATA0 is received. 1: Setup data is not 8-byte or is not DATA0. Cleared by write 1 to USB_INSTSC[18].	R	0
17	ERR_TIMEOUT	Timeout status. This flag will not trigger USB interrupt. 0: No timeout. 1: Host ACK response timeout after IN data packet is sent. Cleared by write 1 to USB_INSTSC[17].	R	0
16:14	Reserved		R	0
13	EP6_ACK	Endpoint 6 ACK transaction flag. 0: No EP6 ACK transaction. 1: EP6 ACK transaction completes. Cleared by write 1 to USB_INSTSC[13].	R	0
12	EP5_ACK	Endpoint 5 ACK transaction flag. 0: No EP5 ACK transaction. 1: EP5 ACK transaction completes. Cleared by write 1 to USB_INSTSC[12].	R	0
11	EP4_ACK	Endpoint 4 ACK transaction flag. 0: No EP4 ACK transaction. 1: EP4 ACK transaction completes. Cleared by write 1 to USB_INSTSC[11].	R	0
10	EP3_ACK	Endpoint 3 ACK transaction flag. 0: No EP3 ACK transaction. 1: EP3 ACK transaction completes. Cleared by write 1 to USB_INSTSC[10].	R	0
9	EP2_ACK	Endpoint 2 ACK transaction flag. 0: No EP2 ACK transaction. 1: EP2 ACK transaction completes. Cleared by write 1 to USB_INSTSC[9].	R	0
8	EP1_ACK	Endpoint 1 ACK transaction flag. 0: No EP1 ACK transaction. 1: EP1 ACK transaction completes. Cleared by write 1 to USB_INSTSC[8].	R	0
7:6	Reserved		R	0
5	EP6_NAK	Endpoint 6 NAK transaction flag. 0: No EP6 NAK transaction. 1: EP6 NAK transaction completes. Cleared by write 1 to USB_INSTSC[5].	R	0
4	EP5_NAK	Endpoint 5 NAK transaction flag. 0: No EP5 NAK transaction. 1: EP5 NAK transaction completes. Cleared by write 1 to USB_INSTSC[4].	R	0
3	EP4_NAK	Endpoint 4 NAK transaction flag. 0: No EP4 NAK transaction. 1: EP4 NAK transaction completes. Cleared by write 1 to USB_INSTSC[3].	R	0
2	EP3_NAK	Endpoint 3 NAK transaction flag. 0: No EP3 NAK transaction. 1: EP3 NAK transaction completes. Cleared by write 1 to USB_INSTSC[2].	R	0
1	EP2_NAK	Endpoint 2 NAK transaction flag. 0: No EP2 NAK transaction. 1: EP2 NAK transaction completes. Cleared by write 1 to USB_INSTSC[1].	R	0

0	EP1_NAK	Endpoint 1 NAK transaction flag. 0: No EP1 NAK transaction. 1: EP1 NAK transaction completes. Cleared by write 1 to USB_INSTSC[0].	R	0

20.9.3 USB Interrupt Event Status Clear Register (USB_INSTSC)

Address Offset: 0x08

Reset value: 0x0000 0000

Bit	Name	Description	Attribute	Reset
31	BUS_RESETC	0: No effect. 1: Clear BUS_RESET bit.	W	0
30	Reserved		R	-
29	BUS_RESUMEC	0: No effect. 1: Clear BUS_RESUME bit.	W	0
28:27	Reserved		R	-
26	USB_SOFC	0: No effect. 1: Clear USB_SOF bit.	W	0
25	BUS_WAKEUPC	0: No effect. 1: Clear BUS_WAKEUP bit.	W	0
24	EP0_PRESETUPC	0: No effect 1: Clear EP0_PRESETUP bit.	W	0
23	EP0_SETUPC	0: No effect 1: Clear EP0_SETUP bit.	W	0
22	EP0_INC	0: No effect. 1: Clear EP0_IN bit.	W	0
21	EP0_OUTC	0:.No effect. 1: Clear EP0_OUT bit.	W	0
20	EP0_IN_STALLC	0: No effect. 1: Clear EP0_IN_STALL bit.	W	0
19	EP0_OUT_STALLC	0: No effect. 1: Clear EP0_OUT_STALL bit.	W	0
18	ERR_SETUPC	0: No effect. 1: Clear ERR_SETUP bit.	W	0
17	ERR_TIMEOUTC	0: No effect. 1: Clear ERR_TIMEOUT bit.	W	0
16:14	Reserved		R	-
13	EP6_ACKC	0: No effect. 1: Clear EP6_ACK bit.	W	0
12	EP5_ACKC	0: No effect. 1: Clear EP5_ACK bit.	W	0
11	EP4_ACKC	0: No effect. 1: Clear EP4_ACK bit.	W	0
10	EP3_ACKC	0: No effect. 1: Clear EP3_ACK bit.	W	0
9	EP2_ACKC	0: No effect. 1: Clear EP2_ACK bit.	W	0
8	EP1_ACKC	0: No effect. 1: Clear EP1_ACK bit.	W	0
7:6	Reserved		R	-
5	EP6_NAKC	0: No effect. 1: Clear EP6_NAK bit.	W	0
4	EP5_NAKC	0: No effect. 1: Clear EP5_NAK bit.	W	0
3	EP4_NAKC	0: No effect. 1: Clear EP4_NAK bit.	W	0
2	EP3_NAKC	0: No effect. 1: Clear EP3_NAK bit.	W	0

1	EP2_NAKC	0: No effect. 1: Clear EP2_NAK bit.	W	0
0	EP1_NAKC	0: No effect. 1: Clear EP1_NAK bit.	W	0

20.9.4 USB Device Address Register (USB_ADDR)

Address Offset: 0x0C

Reset value: 0x0000 0000

Bit	Name	Description	Attribute	Reset
31:7	Reserved		R	0
6:0	UADDR	USB device's address.	R/W	0

20.9.5 USB Configuration Register (USB_CFG)

Address offset: 0x10

Reset value: 0x0000 0000

Bit	Name	Description	Attribute	Reset
31	VREG33_EN	Internal VREG33 output function. If VREG33_EN is disabled, VREG33 will be switched to IC_VDD. 0: Disable 1: Enable *If VREG33 is disabled, the VREG33 will be switched to IC_VDD.	R/W	1
30	PHY_EN	PHY transceiver function. PHY will be automatically disabled if entering sleep mode, deep-sleep mode. 0: Disable PHY transceiver function. 1: Enable PHY transceiver function.	R/W	0
29	DPPU_EN	Internal D+ 1.5k pull-up resistor function. 0: Disable internal D+ pull-up resistor. 1: Enable internal D+ pull-up resistor.	R/W	0
28	SIE_EN	USB serial interface engine enable. 0: Disable USB SIE function. 1: Enable USB SIE function.	R/W	0
27	ESD_EN	USB ESD protection enable. 0: Disable ESD protection. 1: Enable ESD protection.	R/W	0
26	DIS_PDEN	Enable internal D+ and D - 175k pull-down resistor. 0: Disable. 1: Enable.	R/W	0
25:6	Reserved		R	0
5	EP6_DIR	Endpoint 6 IN/OUT direction setting. 0: EP6 only handshakes to IN token packet. 1: EP6 only handshakes to OUT token packet.	R/W	0
4	EP5_DIR	Endpoint 5 IN/OUT direction setting. 0: EP5 only handshakes to IN token packet. 1: EP5 only handshakes to OUT token packet.	R/W	0
3	EP4_DIR	Endpoint 4 IN/OUT direction setting. 0: EP4 only handshakes to IN token packet. 1: EP4 only handshakes to OUT token packet.	R/W	0
2	EP3_DIR	Endpoint 3 IN/OUT direction setting. 0: EP3 only handshakes to IN token packet. 1: EP3 only handshakes to OUT token packet.	R/W	0
1	EP2_DIR	Endpoint 2 IN/OUT direction setting.	R/W	0

		0: EP2 only handshakes to IN token packet. 1: EP2 only handshakes to OUT token packet.		
0	EP1_DIR	Endpoint 1 IN/OUT direction setting. 0: EP1 only handshakes to IN token packet. 1: EP1 only handshakes to OUT token packet.	R/W	0

20.9.6 USB Signal Control Register (USB_SGCTL)

Address offset: 0x14

Reset value: 0x0000 0000

Bit	Name	Description	Attribute	Reset
31:3	Reserved		R	0
2	BUS_DRVEN	Enable to drive USB bus. 0: Not drive USB bus. Write operation to BUS_DP or BUS_DN has no effect. 1: Drive USB bus. The D+/D- bus state can be set by set BUS DP and BUS DN.	R/W	0
1	BUS_DP	USB D+ state 0: D+ state is low. 1: D+ state is high.	R/W	0
0	BUS_DN	USB D- state. 0: D- state is low. 1: D- state is high.	R/W	0

20.9.7 USB Endpoint 0 Control Register (USB_EP0CTL)

Address Offset: 0x18

Reset value: 0x0000 0000

Bit	Name	Description	Attribute	Reset
31	ENDP_EN	Enable Endpoint 0 function. 0: Disable endpoint 0 function. No handshake to endpoint0 SETUP/IN/ OUT token. 1: Enable endpoint 0 function.	R/W	0
30:29	ENDP_STATE[1:0]	Endpoint Handshake State 00: NAK. 01: ACK. For IN transaction, device will handshake data0/1 to IN transaction. For OUT transaction, device will handshake ACK to OUT token and the following data0/1. After IN/OUT ACK transaction completes, the ENDP_STATE will automatically return to NAK state. 10/11: INOUT_STALL: Device will handshake STALL to both IN or OUT token. ENDP_STATE will automatically return to NAK state after USB Setup transaction has completed.	R/W	00
28	IN_STALL_EN	Enable EP0 to handshake STALL to EP0 IN transaction. 0: Disable 1: Enable IN_STALL_EN enable is only effective to EP0 IN token. The EP0 handshake for EP0 OUT transaction depends on OUT_STALL_EN and ENDP_STATE setting. This bit will be automatically cleared to '0' after USB setup transaction has completed.	R/W	0
27	OUT_STALL_EN	Enable EP0 to handshake STALL to EP0 OUT transaction. 0: Disable 1: Enable OUT_STALL_EN enable is only effective to EP0 OUT token. The EP0	R/W	0

		handshake state to EP0 IN transaction depends on IN_STALL_EN and ENDP_STATE setting. This bit will be automatically cleared to '0' after USB setup transaction has completed.		
26:7	Reserved	-	R	0
6:0	ENDP_CNT[6:0]	Endpoint Byte Count For IN transaction, the ENDP_CNT indicates the byte count to be uploaded to host. The maximum count for IN transaction should depend on the bMaximumPacketSize0 declaration in USB Device Descriptor and cannot exceed 64 bytes for USB FS device. For OUT transaction, the ENDP_CNT indicates the byte count received from host.	R/W	0

20.9.8 USB Endpoint n Control Register (USB_EPnCTL, n = 1 ~ 6)

Address Offset: 0x1C, 0x20, 0x24, 0x28, 0x2C, 0x30

Reset value: 0x0000 0000

Bit	Name	Description	Attribute	Reset
31	ENDP_EN	EPn function enable bit 0: Disable EPn function. No handshake to EPn IN/OUT token. 1: Enable EPn function.	R/W	0
30:29	ENDP_STATE[1:0]	Endpoint Handshake State 00: NAK For IN direction usage, device will handshake NAK to IN token. For OUT direction usage, device will handshake NAK to OUT token. 01: ACK: For IN direction usage, device will handshake data0/1 to IN token. For OUT direction usage, device will handshake ACK to OUT token and the following data0/1. After IN/OUT ACK transaction completes, the ENDP_STATE will automatically return to NAK state. 10/11: STALL For IN direction usage, device will handshake STALL to IN token. For OUT direction usage, device will handshake STALL to OUT token and the following data0/1.	R/W	0
28:7	Reserved	-	-	0
6:0	ENDP_CNT[6:0]	Endpoint Byte Count For IN direction usage, the ENDP_CNT indicates the byte count to be uploaded to host. For OUT direction usage, the ENDP_CNT indicates the byte count received from host.	R/W	0

20.9.9 USB Endpoint Data Toggle Register (USB_EPTOGGLE)

Address Offset: 0x3C

Reset value: 0x0000 003F

Bit	Name	Description	Attribute	Reset
31:6	Reserved		R	0
5	EP6_DATA01	0: Clear EP6's toggle bit to DATA0. 1: HW sets toggle bit automatically.	R/W	1
4	EP5_DATA01	0: Clear EP5's toggle bit to DATA0. 1: HW sets toggle bit automatically.	R/W	1
3	EP4_DATA01	0: Clear EP4's toggle bit to DATA0. 1: HW sets toggle bit automatically.	R/W	1

2	EP3_DATA01	0: Clear EP3's toggle bit to DATA0. 1: HW sets toggle bit automatically.	R/W	1
1	EP2_DATA01	0: Clear EP2's toggle bit to DATA0. 1: HW sets toggle bit automatically.	R/W	1
0	EP1_DATA01	0: Clear EP1's toggle bit to DATA0. 1: HW sets toggle bit automatically.	R/W	1

20.9.10 USB Endpoint n Buffer Offset Register (USB_EPnBUFOS, n = 1 ~ 6)

Address Offset: 0x48, 0x4C, 0x50, 0x54, 0x58, 0x5C

Reset value: 0x0000 0000

Bit	Name	Description	Attribute	Reset
31:9	Reserved		R	0
8:2	OFFSET[6:0]	The offset address for each endpoint data buffer. The effective offset address is: USB_SRAM address + {EPnBUFOS[8:2], 2'b00} Where USB_SRAM address = USB_BA + 0x100 For endpoint 0, the offset address is fixed as USB_SRAM address.	R/W	40, 80, C0, 100 140 180
1:0	Reserved		R	0

20.9.11 USB Frame Number Register (USB_FRMNO)

Address Offset: 0x60

Reset value: 0x0000 0000

Bit	Name	Description	Attribute	Reset
31:11	Reserved		R	0
10:0	FRAME_NO[10:0]	The 11-bit frame number of the Start-Of-Frame(SOF) packet. This number is updated by H/W automatically when SOF packet is received.	R	0

20.9.12 USB PHY Parameter Register (USB_PHYPRM)

Address Offset: 0x64

Reset value: 0x0000 0000

Bit	Name	Description	Attribute	Reset
31:26	PHY_PARAM[5:0]	The USB PHY parameter value. The suggested settings would be 0x20.	R/W	0
25:0	Reserved		R	0

20.9.13 USB PHY Parameter Register 2(USB_PHYPRM2)

Address Offset: 0x6C

Reset value: 0x0000 0000

Bit	Name	Description	Attribute	Reset
31:15	Reserved		R	0
14:0	PHY_PARAM2[14:0]	The USB PHY parameter value.	R/W	0

20.9.14 PS/2 Control Register (USB_PS2CTL)

Address Offset: 0x70

Reset value: 0x0000 0000

Bit	Name	Description	Attribute	Reset
31	PS2ENB	PS/2 internal 5kohm pull-up resistor control bit.	R/W	0
30:4	Reserved		R	0
3	SDA	PS/2 SDA data buffer.	R/W	0
2	SCK	PS/2 SCK data buffer	R/W	0
1	SDAM	PS/2 SDA mode control bit.	R/W	0
0	SCKM	PS/2 SCK mode control bit.	R/W	0

20.9.15 USB Read/Write Address Register (USB_RWADDR)

Address Offset: 0x78

Reset value: 0x0000 0000

Bit	Name	Description	Attribute	Reset
31:9	Reserved		R	0
8:2	RWADDR[6:0]	USB FIFO address to be read or written from/to USB FIFO.	R/W	0
1:0	Reserved		R	0

20.9.16 USB Read/Write Data Register (USB_RWDATA)

Address Offset: 0x7C

Reset value: 0x0000 0000

Bit	Name	Description	Attribute	Reset
31:0	RWDATA[31:0]	Data to be read or written from/to USB FIFO.	R/W	0

20.9.17 USB Read/Write Status Register (USB_RWSTATUS)

Address Offset: 0x80

Reset value: 0x0000 0000

Bit	Name	Description	Attribute	Reset
31:2	Reserved		R	0
1	R_STATUS	Read status of USB FIFO. *If F/W is to read the data from USB FIFO, set this bit as '1 '. When hardware has completed the read action (RWDATA content has been written by the new data read from USB FIFO with address RWADDR.), this bit is automatically cleared as '0' by hardware.	R/W	0
0	W_STATUS	Write status of USB FIFO. *If F/W is to write data into USB FIFO, set this bit as '1 '. When hardware has completed the write action (RWDATA content has been read as the new data, and the new data is written into USB FIFO with address RWADDR.), this bit is automatically cleared as '0' by hardware.	R/W	0

20.9.18 USB Read/Write Address Register2 (USB_RWADDR2)

Address Offset: 0x84

Reset value: 0x0000 0000

Bit	Name	Description	Attribute	Reset
31:9	Reserved		R	0
8:2	RWADDR[6:0]	USB FIFO address to be read or written from/to USB FIFO.	R/W	0
1:0	Reserved		R	0

20.9.19 USB Read/Write Data Register2 (USB_RWDATA2)

Address Offset: 0x88

Reset value: 0x0000 0000

Bit	Name	Description	Attribute	Reset
31:0	RWDATA[31:0]	Data to be read or written from/to USB FIFO.	R/W	0

20.9.20 USB Read/Write Status Register 2(USB_RWSTATUS2)

Address Offset: 0x8C

Reset value: 0x0000 0000

Bit	Name	Description	Attribute	Reset
31:2	Reserved		R	0
1	R_STATUS	Read status of USB FIFO. *If F/W is to read the data from USB FIFO, set this bit as '1 '. When hardware has completed the read action (RWDATA content has been written by the new data read from USB FIFO with address RWADDR.), this bit is automatically cleared as '0' by hardware.	R/W	0
0	W_STATUS	Write status of USB FIFO. *If F/W is to write data into USB FIFO, set this bit as '1 '. When hardware has completed the write action (RWDATA content has been read as the new data, and the new data is written into USB FIFO with address RWADDR.), this bit is automatically cleared as '0' by hardware.	R/W	0

21 FLASH

21.1 OVERVIEW

SONiX 32-bit MCU integrated device feature in-system programmable (ISP) FLASH memory for convenient, upgradeable code storage. The FLASH memory may be programmed via the SONiX 32-bit MCU programming interface or by application code for maximum flexibility. SONiX 32-bit MCU provides security options at the disposal of the designer to prevent unauthorized access to information stored in FLASH memory.

- The MCU is stalled during Flash program and erase operations, although peripherals (Timers, WDT, I/O, PWM, etc.) remain active.
- Watchdog timer should be cleared if enabled before the Flash write or erase operation.
- The erase operation sets all the bits in the Flash page to logic 1.
- HW will hold system clock and automatically move out data from RAM and do programming, after programming finished, HW will release system clock and let MCU execute the next instruction.

21.2 EMBEDDED FLASH MEMORY

The Flash memory is organized as 32-bit wide memory cells that can be used for storing both code and data constants, and is located at a specific base address in the memory map of chip.

The high-performance Flash memory module in chip has the following key features:

- Memory organization: the Flash memory is organized as a User ROM, Boot ROM.

User ROM	Up to 256K Bytes divided into 256 pages of 1024 Bytes
Boot ROM	Up to 4K Bytes divided into 4 pages of 1024 Bytes

The Flash interface implements instruction access and data access based on the AHB protocol. It implements the logic necessary to carry out Flash memory operations (Program/Erase). Program/Erase operations can be performed over the whole product voltage range.

21.3 FEATURES

- Read interface (32-bit)
- Flash Program / Erase operation
- Code Option includes Code Security (CS)

Write operations to the main memory block and the code options are managed by an embedded Flash Memory Controller (FMC). The high voltage needed for Program/Erase operations is internally generated. The main Flash memory can be read/write protected against different levels of Code Security (CS).

During a write operation to the Flash memory, any attempt to read the Flash memory will stall the bus. The read operation will proceed correctly once the write operation has completed. This means that code or data fetches cannot be made while a write/erase operation is ongoing.

For write and erase operations on the Flash memory, the IHRC will be turn ON by FMC. The Flash memory can be programmed and erased using ICP and ISP.

21.4 ORGANIZATION

Block	Name	Base Address	Size (Byte)
User ROM	Page 0	0x00000000 ~ 0x000003FF	1024
	Page 1	0x00000400 ~ 0x000007FF	1024
	. . .	. . .	. . .
	Page 255	0x0003FC00 ~ 0x0003FFFF	1024
Boot Loader	Page 0	0x1FFF0000 ~ 0x1FFF03FF	1024
	Page 1	0x1FFF0400 ~ 0x1FFF07FF	1024
	Page 2	0x1FFF0800 ~ 0x1FFF0BFF	1024
	Page 3	0x1FFF0C00 ~ 0x1FFF0FFF	1024

21.5 READ

The embedded Flash module can be addressed directly, as a common memory space. Any data read operation accesses the content of the Flash module through dedicated read senses and provides the requested data.

The read interface consists of a read controller on one side to access the Flash memory, and an AHB interface on the other side to interface with the CPU. The main task of the read interface is to generate the control signals to read from the Flash memory as required by the CPU.

21.6 PROGRAM/ERASE

The Flash memory erase operation can be performed at page level.

To ensure that there is no over-programming, the Flash programming and erase controller blocks are clocked by IHRC.

21.7 EMBEDDED BOOT LOADER

The embedded boot loader is used to reprogram the Flash memory using the UART0 serial interface. This program is located in the Boot ROM and is programmed by SONiX during production.

21.8 FLASH MEMORY CONTROLLER (FMC)

The FMC handles the program and erase operations of the Flash memory.

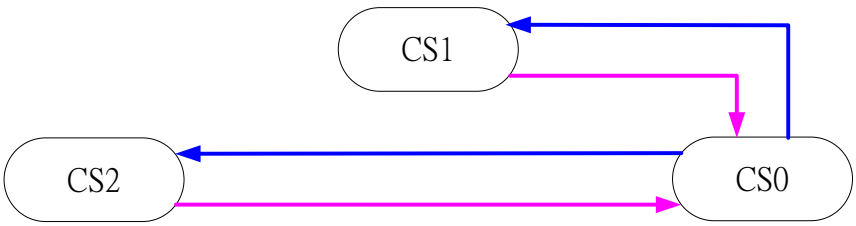
21.8.1 CODE SECURITY (CS)

Code Security is a mechanism that allows the user to enable different levels of security in the system so that access to the on-chip Flash and use of the ISP can be restricted.

> ✷ ***Note: Any Code Security change becomes effective only after the MCU has been Reboot.***

User ROM		CS0	CS1	CS2	Description
WRITER	Read	O	X	X	
	Erase	O	O(*)	O(*)	(*) WRITER will change the CS level to CS0.
	Program	O	O	O	
FW (EEPROM emulation)	Read	O	O	O	
	Erase	O	O	O	
	Program	O	O	O	
SWD	Read	O	X	X	
	Erase	O	X	X	
	Program	O	X	X	

> ✷ ***Note: User may try to change security level from CS3 to CS0, from CS2 to CS0, or from CS1 to CS0. HW shall:***
> ***1. Mass erase the User ROM first. User shall NOT execute this operation in debug mode, since the SWD communication may fail during the mass erase procedure.***
> ***2. Update security level.***



——— includes:
- New option byte programming

——— includes:
- Option byte erase
- Mass Erase

21.8.2 PROGRAM FLASH MEMORY

The Flash memory can be programmed 32 bits at a time. CPU can program the main Flash memory by performing standard word write operations. The PG bit in the FLASH_CTRL register must be set. FMC preliminarily reads the value at the addressed main Flash memory location and checks that it has been erased. If not, the program operation is skipped and a warning is issued by the PGERR bit in FLASH_STATUS register. The end of the program operation is indicated by the EOP bit in the FLASH_STATUS register.

The main Flash memory programming sequence in standard mode is as follows:
1. Set the PG bit in the FLASH_CTRL register.
2. Perform the data write at the desired address.
3. Wait for the BUSY bit to be reset.
4. (Optional) Read the programmed value and verify.

✷ ***Note: User SHALL fill in more or equal to 8 bytes to FLASH_DATA register when programming the ROM.***

21.8.3 ERASE

The Flash memory can be erased page by page or completely (Mass Erase).

21.8.3.1 PAGE ERASE

A page of the Flash memory can be erased using the Page Erase feature of the FMC. To erase a page, the procedure below should be followed:
1. Set the PER bit in the FLASH_CTRL register
2. Program the FLASH_ADDR register to select a page to be erased
3. Set the STARTE bit in the FLASH_CTRL register
4. Wait for the BUSY bit to be reset
5. (Optional) Read the erased page and verify

21.8.3.2 MASS ERASE

When the Flash memory read protection is changed from protected to unprotected, a Mass Erase of the User ROM is performed by HW before reprogramming the read protection option.

21.9 READ PROTECTION

The read protection is activated by setting the Code Security bytes in Code option.

When the Flash memory read protection is changed from protected to unprotected, a Mass Erase of the User ROM is performed by HW before reprogramming the read protection option.

21.10 HW CHECKSUM

HW checksum is the checksum of User ROM/Boot ROM. If the read protection is enabled, the users can still readout the HW checksum through Writer or ISP AP.

21.11 FMC REGISTERS

Base Address: 0x4006 2000

21.11.1 Flash Low Power Control register (FLASH_LPCTRL)

Address offset: 0x00

Bit	Name	Description	Attribute	Reset
31:16	FMCKEY	FMC verify key. Read as 0. When writing to the register you must write 0x5AFA to FMCKEY, otherwise behavior of writing to the register is ignored.	W	0
15:6	Reserved		R	0
5:0	LPMODE[5:0]	Flash Low Power mode enable bit 000000b: HCLK≦24MHz 101001b: 24MHz<HCLK≦48MHz 111001b: HCLK>48MHz Other: Reserved (May cause unexpected error to force MCU enter Hard fault handler)	R/W	0

21.11.2 Flash Status register (FLASH_STATUS)

Address offset: 0x04

Bit	Name	Description	Attribute	Reset
31:3	Reserved		R	0
2	ERR	Error flag 0: Read→No error. Write→Clear this flag. 1: Set by HW when ✸ Start to Erase/Program and find that the address is over page boundary. ✸ Start to Erase/Program and find that the address is illegal. ✸ The address to be programmed contains a value different from 0xFFFFFFFF before programming.	R/W	0
1	Reserved		R	0
0	BUSY	Busy flag 0: Flash operation is not busy. 1: Flash operation is in progress. This is set on the beginning of a Flash operation and reset when the operation finishes or when an error occurs by HW.	R	0

21.11.3 Flash Control register (FLASH_CTRL)

Address offset: 0x08

Bit	Name	Description	Attribute	Reset
31:8	Reserved		R	0
7	CHK	Checksum calculation chosen This bit is set only by SW and reset when the BUSY bit resets. 1: Triggers Checksum calculation. 0: Checksum calculation is done.	R/W	0
6	START	Start Erase/Program operation 1: Triggers an Erase/Program operation when set. This bit is set only by SW and resets when the BUSY bit resets. 0: Erase process is done.	R/W	0
5:3	Reserved		R	0

2	MER	Mass erase chosen mode bit Erase of all user pages chosen. This bit is set only by SW and reset when the BUSY bit resets.	R/W	0
1	PER	Page Erase chosen. This bit is set only by SW and reset when the BUSY bit resets.	R/W	0
0	PG	Flash Programming chosen. This bit is set only by SW and reset when the BUSY bit resets.	R/W	0

21.11.4 Flash Data register (FLASH_DATA)

Address offset: 0x0C

For Page Program operations, this should be updated by SW to indicate the data to be programmed.

Bit	Name	Description	Attribute	Reset
31:0	DATA[31:0]	Data to be programmed.	R/W	0

21.11.5 Flash Address register (FLASH_ADDR)

Address offset: 0x10

The Flash address to be erased or programmed should be updated by SW, and the PG bit or PER bit shall be set before filling in the Flash address.

✸ ***Note:***
1. Write access to this register is blocked when the BUSY bit in the FLASH_STATUS register is set.
2. Value must be multiples of 8 in the FLASH_ADDR register.

Bit	Name	Description	Attribute	Reset
31:0	FAR[31:0]	Flash Address Choose the Flash address to erase when Page Erase is selected, or to program when Page Program is selected.	R/W	0

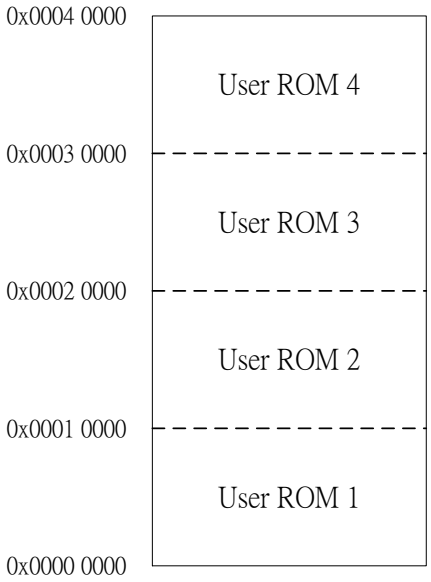
21.11.6 Flash Checksum register (FLASH_CHKSUM)

Address offset: 0x14

Bit	Name	Description	Attribute	Reset
31:16	BRCHKSUM[15:0]	Checksum of Boot ROM.	R	0
15:0	URCHKSUM[15:0]	Checksum of User ROM.	R	0

21.11.7 Flash Checksum register 1 (FLASH_CHKSUM1)

Address offset: 0x18



Bit	Name	Description	Attribute	Reset
31:16	UR2CHKSUM[15:0]	Checksum of User ROM 2.	R	0
15:0	UR1CHKSUM[15:0]	Checksum of User ROM 1.	R	0

21.11.8 Flash Checksum register 2 (FLASH_CHKSUM2)

Address offset: 0x1C

Bit	Name	Description	Attribute	Reset
31:16	UR4CHKSUM[15:0]	Checksum of User ROM 4.	R	0
15:0	UR3CHKSUM[15:0]	Checksum of User ROM 3.	R	0

22 SERIAL-WIRE DEBUG (SWD)

22.1 OVERVIEW

SWD functions are integrated into the ARM Cortex-M0. The ARM Cortex-M0 is configured to support up to four breakpoints and two watch points.

22.2 FEATURES

- Supports ARM Serial Wire Debug (SWD) mode.
- Direct debug access to all memories, registers, and peripherals.
- No target resources are required for the debugging session.
- Up to four breakpoints.
- Up to two data watch points that can also be used as triggers.

22.3 PIN DESCRIPTION

Pin Name	Type	Description	GPIO Configuration
SWCLK	I	Serial Wire Clock pin in SWD mode.	
SWDIO	I/O	Serial Wire Data Input/Output pin in SWD mode.	

22.4 DEBUG NOTE

22.4.1 LIMITATIONS

Debug mode changes the way in which reduced power modes work internal to the ARM Cortex-M0 CPU, and this ripples through the entire system. These differences mean that power measurements should not be made while debugging, the results will be higher than during normal operation in an application.

During a debugging session, the SysTick Timer is automatically stopped whenever the CPU is stopped. Other peripherals are not affected.

22.4.2 DEBUG RECOVERY

User code may disable SWD function in order to use P3.5 and P3.6 as GPIO, and may not debug by SWD function to debug or download FW any more.

SONiX provide Boot loader to check the status of P1.3 (BOOT pin) during boot procedure. If P1.3 is Low during Boot procedure, MCU will execute code in Boot loader instead of User code, so SWD function is not disabled.

Exit Boot loader, user code can still configure P1.3 as other functions such as GPIO.

✷ ***Note: We strongly recommanded NOT using BOOT pin as output pin to drive the LED, otherwise, the BOOT pin status may be low during boot procedure.***

22.4.3 INTERNAL PULL-UP/DOWN RESISTORS on SWD PINS

To avoid any uncontrolled IO levels, the device embeds internal pull-up and pull-down resistor on the SWD input pins:

- NJTRST: Internal pull-up
- SWDIO/JTMS: Internal pull-up
- SWCLK/JTCK: Internal pull-down

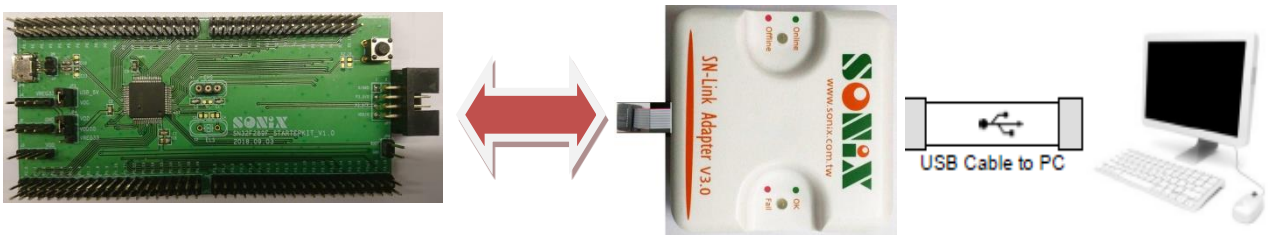
Once a SWD function is disabled by SW, the GPIO controller takes control again.

23 DEVELOPMENT TOOL

SONiX provides an Embedded ICE emulator system to offer 32-bit series MCU firmware development.

SONiX 32-bit series Embedded ICE Emulator System includes:

- SONiX 32-bit MCU Starter-Kit.
- SN-LINK-V3
- USB cable to provide communications between the SN-LINK-V3 and PC.
- IDE Tools (KEIL RVMDK)



SONiX 32-bit MCU Starter-Kit. SN-LINK-V3 IDE Tools

SONiX 32-bit series Embedded ICE Emulator Feature:

- Target's Operating Voltage: 2.5V~5.5V.
- Up to 4 hardware break points.
- System clock rate up to 48MHz.
- Oscillator supports IHRC, ILRC, EHS/ELS X'tal.

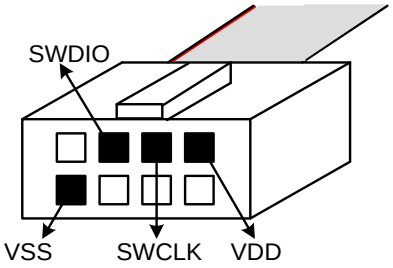
SONiX 32-bit series Embedded ICE Emulator Limitation:

- SWCLK and SWDIO pins are shared with GPIO pins. In embedded ICE mode, the shared GPIO function can't work.

23.1 SN-LINK-V3

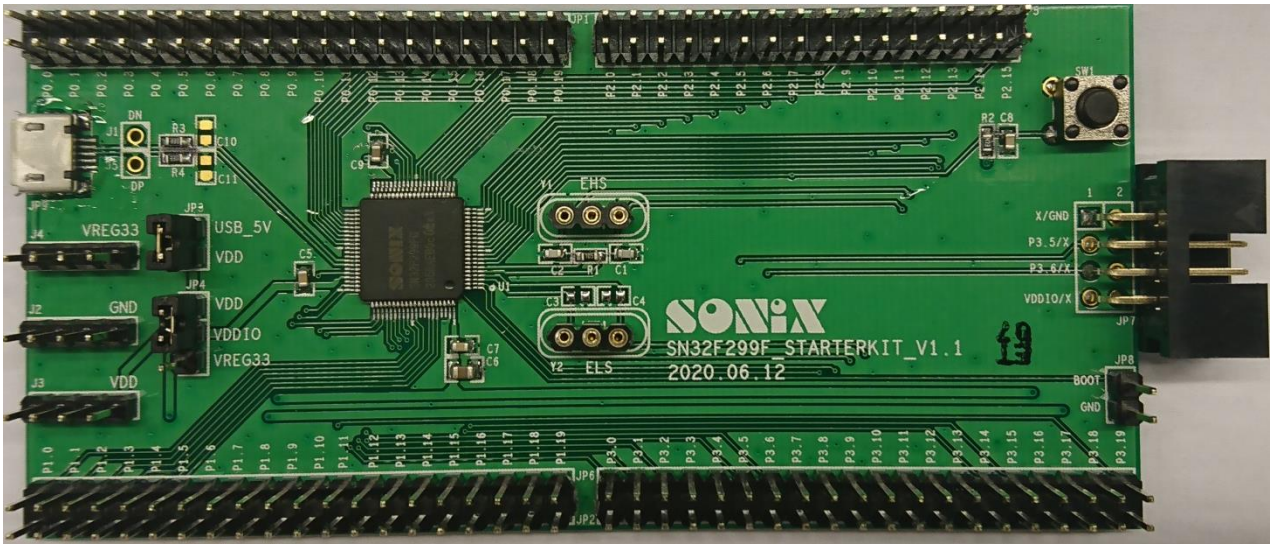
SN-LINK-V3 is a high speed emulator for SONiX 32-bit MCU. It debugs and programs based on SWD protocol. In addition to debugger functions, the SN-LINK-V3 also may be used as a programmer to load firmware from PC to MCU for engineering production, even mass production.

SN-LINK-V3 communicates with SONiX 32-bit MCU through SWD interface. The pin definition of the Modular cable is as following:



23.2 SN32F290 STARTER-KIT

SONiX 32-bit MCU Starter-kit is an easy-development platform. It includes real chip and I/O connectors to input signal or drive extra device of user's application. It is a simple platform to develop application as target board not ready. The starter-kit can be replaced by target board because of integrated SWD debugger circuitry.



- JP9 : Micro USB connector.
- JP3 : USB Power connector.
- JP4 : VDDIO1 power connector: Choose the source of VDDIO1(5.0V/3.3V on board).
- J2 : GND connector.
- J3 : VDD connector.
- J4 : VREG33 output connector.
- U1 : SN32F299F real chip.
- RESET button : External reset trigger source.
- JP7 : SN-LINK connector
- JP8 : Short to force MCU stay in Boot loader.

24 ELECTRICAL CHARACTERISTIC

24.1 ABSOLUTE MAXIMUM RATING

Supply voltage (Vdd)..... - 0.3V ~ 5.5V
Input in voltage (Vin).....Vss – 0.2V ~ Vdd + 0.2V
Operating ambient temperature (Topr)..... -40°C ~ + 85°C
Storage ambient temperature (Tstor) ..... –40°C ~ + 125°C

24.2 ELECTRICAL CHARACTERISTIC

Standard Operating Conditions (Typical temperature Ta = 25℃)
Operating Temperature -40℃ ≦ Ta ≦ +85℃ for Industrial Class
The below data covers process corner range (SS~TT~FF).

PARAMETER	SYM.	DESCRIPTION		MIN.	TYP.	MAX.	UNIT
Operating Voltage	Vdd	Supply voltage for core and external rail		2.5	3.3	5.5	V
	Vdd2	USB mode		3.1	5.0	5.25	V
VDD rise rate	V_{POR}	VDD rise rate to ensure internal power-on reset		0.05	-	-	V/ms
VDDIO1 Voltage	V_{DDIO1}	I/O driver power for P0.12~P0.15、P1.6~P1.11、P3.0~P3.2、P3.5~P3.6		1.8		Vdd	V
Power Consumption							
Supply Current	Idd1	Normal mode	System clock = 12MHz [1][2][3]	-	2.9	-	mA
			System clock = 24MHz [1][3][4]		5.9		mA
			System clock = 32MHz [1][3][4]		8.5		mA
			System clock = 48MHz [1][3][4]	-	11	-	mA
		Normal mode(USB mode)	System clock = IHRC 12MHz [3][6][7]	-	6.3	-	mA
			System clock = PLL 12MHz [3][6][7]		6.5		mA
			System clock = PLL 24MHz [3][6][7]		9		mA
			System clock = PLL 48MHz [3][6][7]	-	12	-	mA
	Idd2	Sleep Mode(USB mode)	System clock = 32KHz [3][6][8]	-	300	-	uA
	Idd3	Deep-sleep Mode	Vdd=3.3V [1][3][5]	-	2	-	uA
Port Pins, RESET pin							
High-level input voltage	V_{IH}			0.7Vdd	-	Vdd	V
Low-level input voltage	V_{IL}			Vss	-	0.3Vdd	V
Input voltage	V_i			0	-	Vdd	V
Output voltage	V_o			0	-	Vdd	V
I/O port pull-up resistor	R_{PU}	Vin = Vss , Vdd = 5.0V Vin = Vss , Vdd = 3.3V		40 50	50 75	60 100	KΩ

I/O port pull-down resistor	R_{PD}	Vin = 5.0V Vin = 3.3V		40 50	50 75	60 100	KΩ
I/O High-level output source current	I_{OH}	Standard port and RESET pins	V_{OP} = Vdd – 0.5V;	12	20	-	mA
I/O Low-level output sink current	I_{OL1}	Standard port and RESET pins, except P0.0, P0.1, P0.2, P0.3, P1.12, P1.13	V_{OP} = Vss + 0.5V	12	20	-	mA
	I_{OL2}	P0.0, P0.1, P0.2, P0.3, P1.12, P1.13	V_{OP} = Vss + 1.5V	80	100	-	mA
ADC							
ADC Operating Voltage	V_{ADC}			2.5		5.5	V
External reference voltage	V_{EREF}	Vdd=5V		2.5		Vdd	V
Internal VDD Reference Voltage	V_{IREF1}	Vdd=2.5V~5V			VDD		V
Internal 4.5V Reference Voltage	V_{IREF2}	Vdd=5V		4.41	4.5	4.59	V
Internal 3V Reference Voltage	V_{IREF3}	Vdd=3.5V~5V		2.94	3	3.06	V
Internal 2V Reference Voltage	V_{IREF4}	Vdd=2.5V~5V		1.96	2	2.04	V
AVREFH pin input voltage	V_{REFH}	Vdd=5V		2		VDD	V
ADC current consumption	I_{ADC}	Vdd=5V			100		uA
Resolution	Nr	No missing code.		10	11	12	bit
AIN0 ~ AIN15 input voltage	V_{AIN}			0	-	V_{REFH}	V
Integral Nonlinearity	INL	Vdd=5V		-1	-	+1	LSB
Differential Nonlinearity	DNL	Vdd=5V		-1	-	+1	LSB
ADC Clock Frequency	F_{ADCLK}	Vdd=5V				16M	Hz
ADC Offset Voltage	V_{OFFSET}	Non-trimmed		-10	0	+10	mV
		Trimmed		-2	0	+2	mV
ADC enable time	T_{ADEN}	Ready to start convert after set ADENB = “1”		100	-	-	us
ADC Conversion Cycle Time	F_{ADCYL}	Vdd=2.5V~5.5V		64			$1/F_{ADCLK}$
COMPARATOR							
CMP Operating Voltage	V_{CMP}			2.5		5.5	V
Supply Current	I_{CMP}	Normal mode, Vdd=5V (Internal Ref. regulator Off)			75	100	uA
Input Offset Voltage	V_{OFFSET}	Vdd=5V, V_{CM}=1/2*VDD		-5		+5	mV
Response Time	T_{RS}	Normal mode, Positive input voltage = 1/2*Vdd. Negative input voltage transitions from Vss to Vdd.			50	100	ns
Output Slew Rate Time	T_{OSR}	Vo=rising Vss~Vdd or falling Vdd~Vss. Vdd=5V.		-	20	-	ns
Internal 3V Reference Voltage	V_{IREF1}	Vdd=3.5V~5V		2.94	3	3.06	V
Internal 2V Reference Voltage	V_{IREF2}	Vdd=2.5V~5V		1.96	2	2.04	V
Internal 1.5V Reference Voltage	V_{IREF3}	Vdd=2.5V~5V		1.47	1.5	1.53	V
Common Mode Input Voltage Range	V_{CMR}	Vdd=5.0V		Vss+0.5		Vdd-0.5	V
OPA							
Power Supply Range	V_{OPA}			2.5		5.5	V
Supply Current	I_{OPA}	Vdd=5V. Unique gain buffer (Vin=Vss).			100	150	uA
Common Mode Input Voltage Range	V_{CM}	Vdd=5.0V		Vss-0.3		Vdd+0.3	V
Input Offset Voltage	V_{OFFSET}	V_{CM}=Vss		2		7	mV
Power Supply Rejection Ratio	PSRR	V_{CM}=Vss		70	85	95	dB
Common Mode Rejection Ratio	CMRR	V_{CM}=-0.3V~2.5V. Vdd=5V.		70	85	-	dB
		V_{CM}=-0.3V~5.3V. Vdd=5V.		65	80	-	dB
Phase Margin	Φm	C_L=100pF			60		deg
Gain Margin	Gm				10		dB
Unity Gain Bandwidth	B1	C_L=100pF			250		KHz
Output Slew Rate	T_{OSR}	Output voltage transitions from Vss to Vdd.			5		us
		Output voltage transitions from Vdd to Vss.			5		us
Open-Loop Gain (Large Signal)	A_{OL}	Vout=0.2V~Vdd-0.2V. V_{CM} =Vss.		90	110	-	dB
Maximum Output Voltage Swing	Vol, Voh			Vss+7		Vdd-7	mV
Output Short Current	I_{SC}				±15		mA
FLASH							
Supply Voltage	Vdd1			1.35	1.50	1.65	V
Endurance time	T_{EN}	Erase + Program		20K	100K	-	Cycle
Page Erase current	I_{PER}			-	3	5	mA
Program current	I_{PG}			-	3	5	mA
Page erase time	T_{PE}	1-Page (1024 bytes)		-	1	2	ms
Mass erase time	T_{MER}			-	7	10	ms

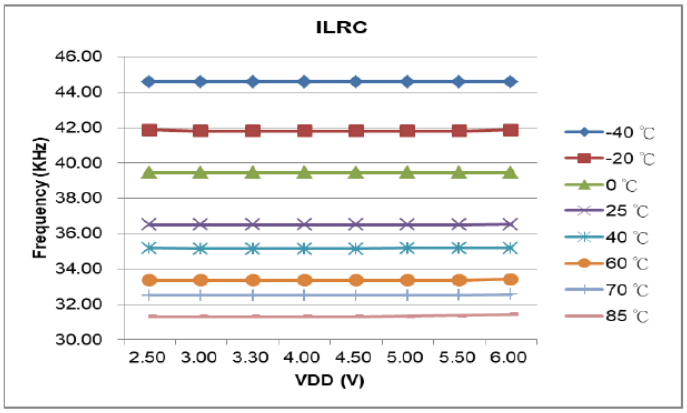
1-Word Programming time	T_{PG}	1-Word (64 bits)		-	10	20	us
MISC							
Low Voltage Detector	LVD	Interrupt/Reset	Level 0	2.60	2.70	2.80	V
			Level 1	2.90	3.00	3.10	V
			Level 2	3.50	3.60	3.70	V
IHRC Freq.	F_{IHRC}	*T=25℃*, Vdd=1.8V~ 5.5V		11.76	12	12.24	MHz
		T=-40℃~85℃, Vdd=1.8V~5.5V		11.70	12	12.30	MHz
3.3V Regulator Output voltage	V_{REG33}	Vcc ≧ 3.60V		3.0		3.4	V
ESD_HBM	V_{ESD_HBM}	ESD human body mode		5000			V
ESD_MM	V_{ESD_MM}	ESD machine mode		300			V
ESD_CDM	V_{ESD_CDM}	ESD charged device model		900			V

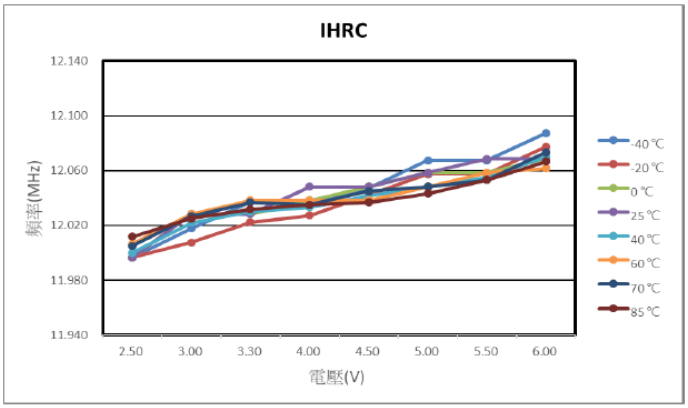
*** These parameters are for design reference, not tested.**

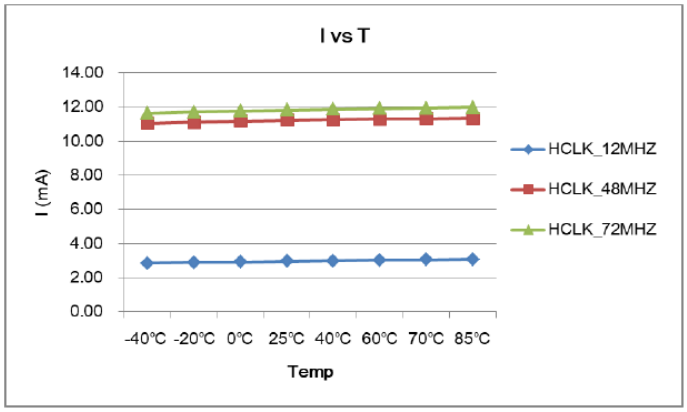
[1] IDD measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled and VDD=3.3V
[2] IHRC and ILRC are enabled, external X'tal is disabled, and PLL is disabled.
[3] LVD and all peripherals are disabled.
[4] IHRC is disabled, external high X'tal is enabled, and PLL is enabled.
[5] All oscillators and analog blocks are turned off.
[6] IDD measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled and VDD=5V
[7] IHRC and ILRC are enabled, external X'tal is disabled, and PLL is enabled.
[8] IHRC is disabled, ILRC is enabled, and PLL is disabled.

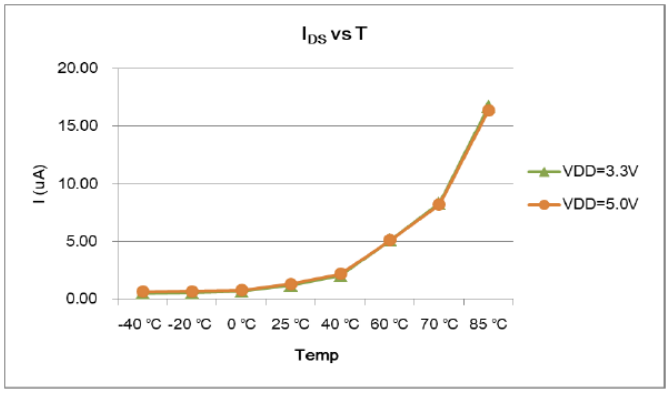
24.3 CHARACTERISTIC GRAPHS

The Graphs in this section are for design guidance, not tested or guaranteed. In some graphs, the data presented are outside specified operating range. This is for information only and devices are guaranteed to operate properly only within the specified range.









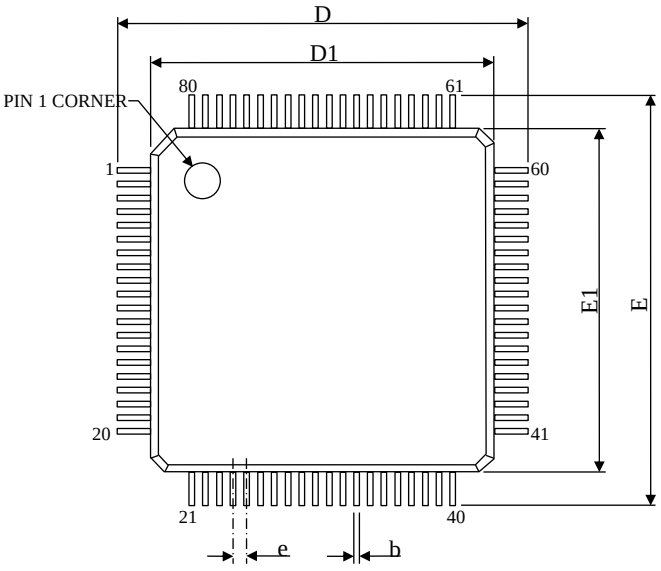
*Supply Current v.s. Temperature (Operating Conditions: All pins configured as GPIO outputs driven Low and pull-up resistors disabled)

25 FLASH ROM PROGRAMMING PIN

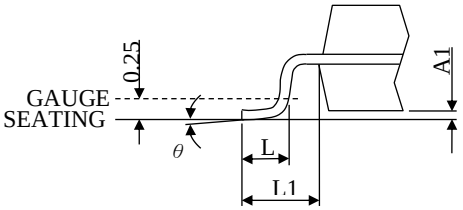
Programming Information of SN32F290 Series											
Chip Name		SN32F299F		SN32F298F		SN32F297F					
Writer Connector JP5		Flash IC / JP3 Pin Assignment									
Number	Name	Number	Pin	Number	Pin	Number	Pin	Number	Pin	Number	Pin
1	VDD	35 57 80	VDD	32 48 64	VDD	24 36 48	VDD				
2	GND	79	VSS	63	VSS	47	VSS				
3	CLK	51	P3.1	42	P3.1	30	P3.1				
4	CE										
5	PGM	58	P3.6	49	P3.6	37	P3.6				
6	OE	55	P3.5	46	P3.5	34	P3.5				
7	D1										
8	D0										
9	D3										
10	D2										
11	D5										
12	D4										
13	D7										
14	D6										
15	VDD										
16	-										
17	HLS										
18	RST										
19	-										
20	ALSB/PDB	52	P3.2	43	P3.2	31	P3.2				

26 PACKAGE INFORMATION

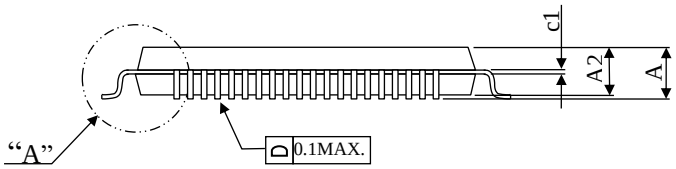
26.1 LQFP 80 PIN



TOP VIEW



DETAIL



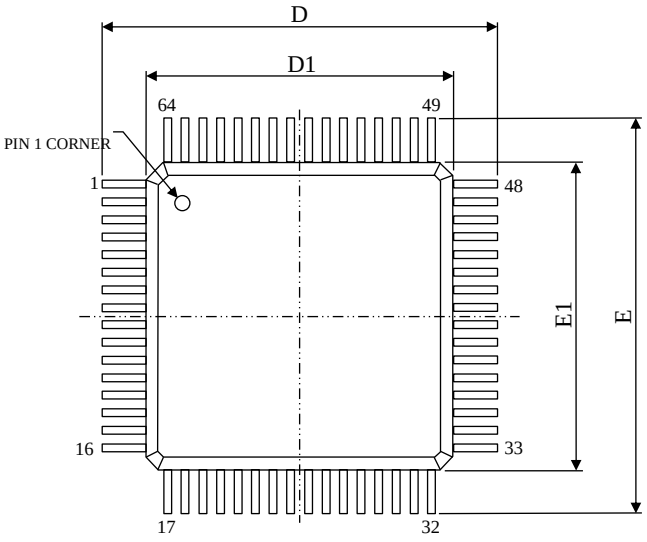
SIDE VIEW

SYMBOLS	Dimension in mm			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	--	--	1.60	--	--	0.063
A1	0.05	--	0.2	0.002	--	0.008
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
c1	0.09	--	0.18	0.004	--	0.007
D	12 BSC			0.472 BSC		
D1	10 BSC			0.394 BSC		
e	0.4 BSC			0.016 BSC		
E	12 BSC			0.472 BSC		
E1	10 BSC			0.394 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.0 REF			0.039 REF		
θ	0˚	3.5˚	7˚	0˚	3.5˚	7˚

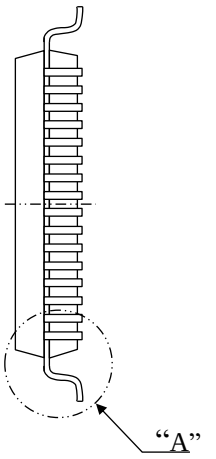
Notes：

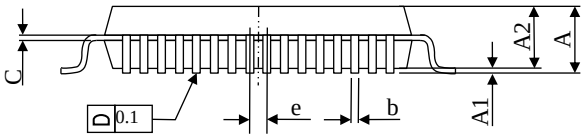
1. CONTROLLING DIMENSION：MILLIMETER (mm)
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

26.2 LQFP 64 PIN

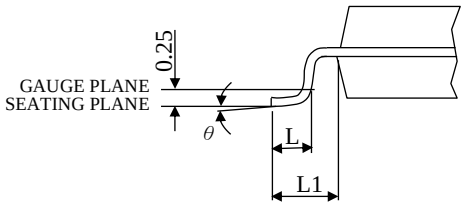


TOP VIEW





SIDE VIEW



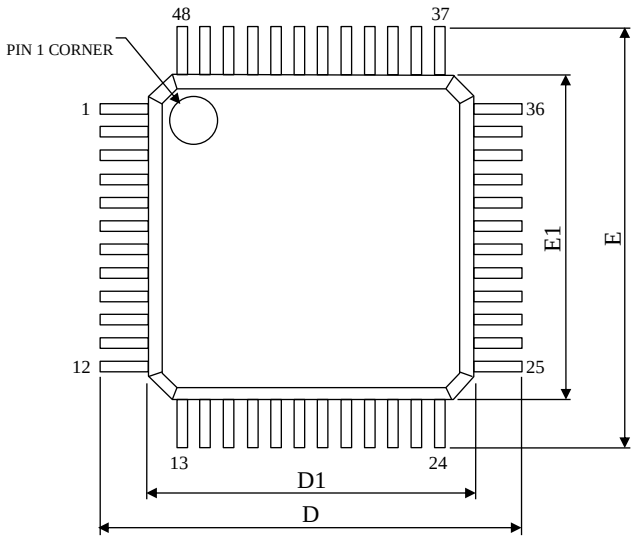
DETAIL "A"

SYMBOLS	Dimension in mm			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	--	--	1.60	--	--	0.063
A1	0.05	--	0.25	0.002	--	0.01
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.19	0.25	0.005	0.007	0.010
c	0.09	--	0.20	0.004	--	0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
e	0.40 BSC			0.016 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
L	0.4	0.60	0.8	0.016	0.024	0.032
L1	1.00 REF			0.039 REF		
θ	0˚	3.5˚	7˚	0˚	3.5˚	7˚

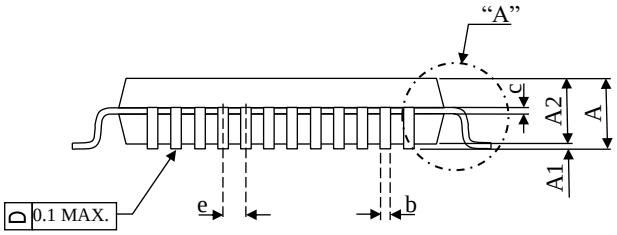
Notes：

1. CONTROLLING DIMENSION：MILLIMETER (mm)
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

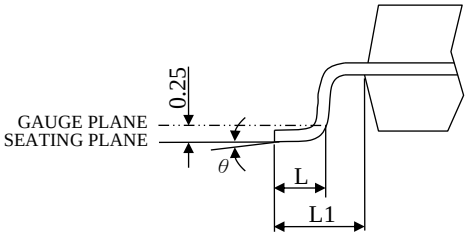
26.3 LQFP 48 PIN



TOP VIEW



SIDE VIEW



DETAIL "A"

SYMBOLS	Dimension in mm			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	--	--	1.60	--	--	0.063
A1	0.05	--	0.15	0.002	--	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09	--	0.20	0.004	--	0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
e	0.50 BSC			0.020 BSC		
L	0.40	0.60	0.80	0.016	0.024	0.031
L1	1.00 REF			0.039 REF		
θ	0˚	3.5˚	7˚	0˚	3.5˚	7˚

Notes：

1. CONTROLLING DIMENSION：MILLIMETER (mm)
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

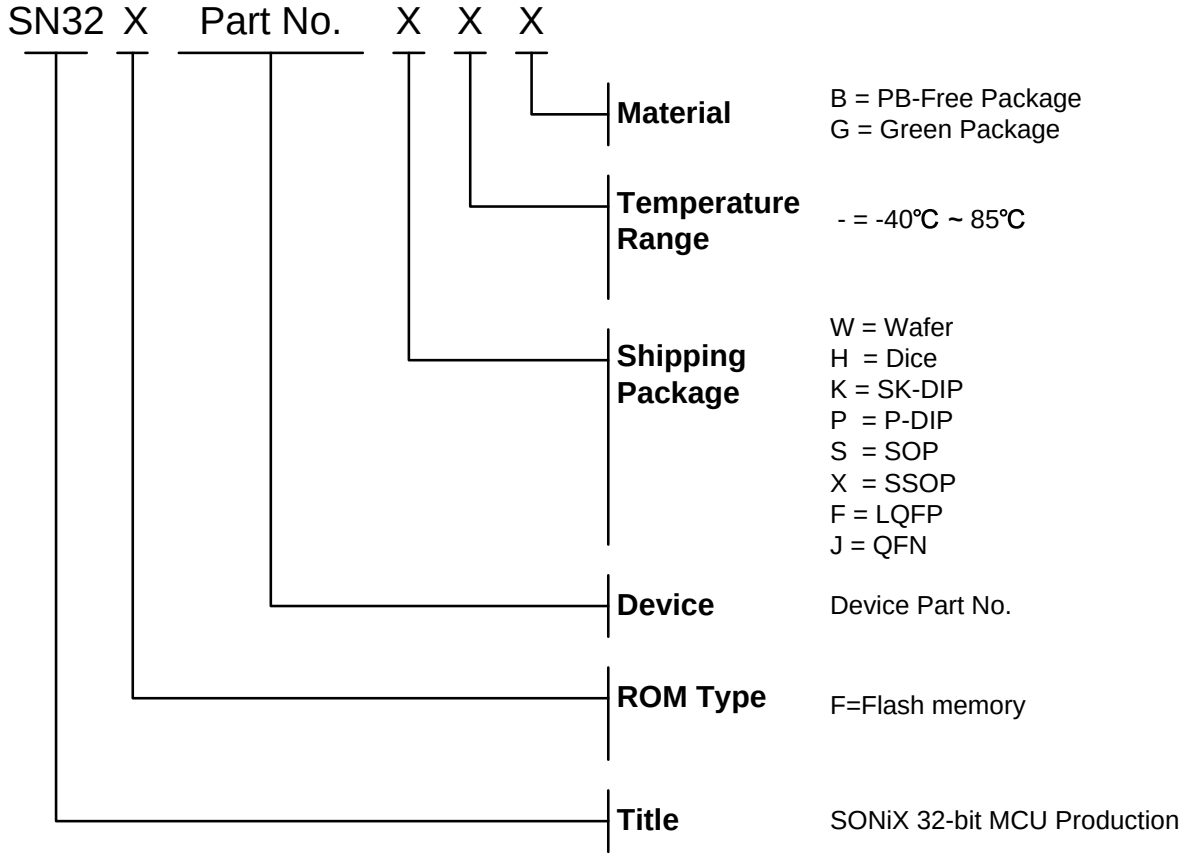
27 MARKING DEFINITION

27.1 INTRODUCTION

There are many different types in SONiX 32-bit MCU production line.

This note lists the marking definitions of all 32-bit MCU for order or obtaining information.

27.2 MARKING INDETIFICATION SYSTEM

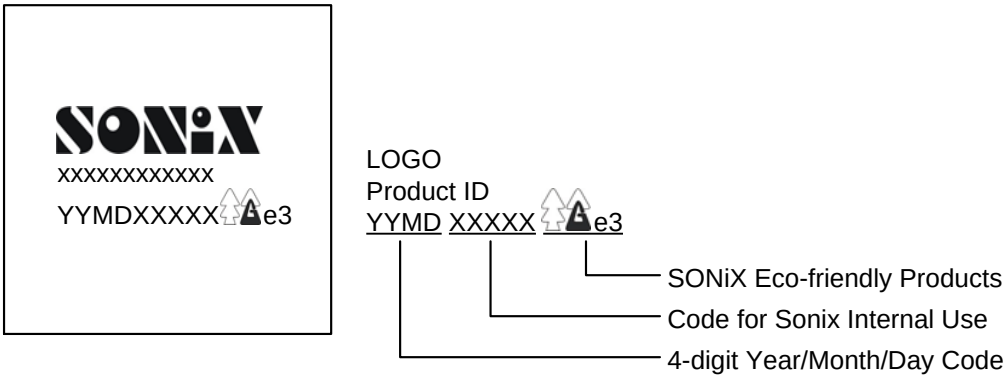


27.3 MARKING EXAMPLE

Name	ROM Type	Device	Package	Temperature	Material
SN32F299FG	Flash memory	299	LQFP	-40℃~85℃	Green Package
SN32F298FG	Flash memory	299	LQFP	-40℃~85℃	Green Package
SN32F297FG	Flash memory	299	LQFP	-40℃~85℃	Green Package
SN32F299W	Flash memory	299	Wafer	-40℃~85℃	-
SN32F299H	Flash memory	299	Dice	-40℃~85℃	-

27.4 DATECODE SYSTEM

The figure below is an example of the marking. Contents such as the product ID or symbol may vary according to different packages.



SONIX reserves the right to make change without further notice to any products herein to improve reliability, function or design. SONIX does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others. SONIX products are not designed, intended, or authorized for us as components in systems intended, for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SONIX product could create a situation where personal injury or death may occur. Should Buyer purchase or use SONIX products for any such unintended or unauthorized application. Buyer shall indemnify and hold SONIX and its officers , employees, subsidiaries, affiliates and distributors harmless against all claims, cost, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use even if such claim alleges that SONIX was negligent regarding the design or manufacture of the part.

Main Office:
Address: 10F-1, NO. 36, Taiyuan Street., Chupei City, Hsinchu, Taiwan R.O.C.
Tel: 886-3-5600 888
Fax: 886-3-5600 889

Taipei Office:
Address: 15F-2, NO. 171, Song Ted Road, Taipei, Taiwan R.O.C.
Tel: 886-2-2759 1980
Fax: 886-2-2759 8180

Hong Kong Office:
Unit No.705,Level 7 Tower 1,Grand Central Plaza 138 Shatin Rural Committee Road, Shatin, New Territories, Hong Kong.
Tel: 852-2723-8086
Fax: 852-2723-9179

Technical Support by Email:
Sn8fae@sonix.com.tw